Pushing Ultra-Low-Power Digital Circuits into the Nanometer Era

UCL Université catholique de Louvain

Microelectronics Laboratory

David Bol

Ph.D public defense

December 16, 2008

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Why ultra-low power ?

<u>High-performance circuits</u>

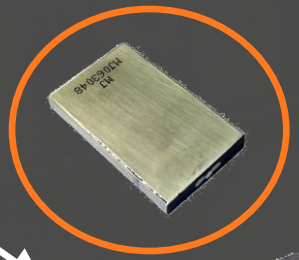
Performances: 10 GOp/s

Power < 100 W

<u>Low-power circuits</u>

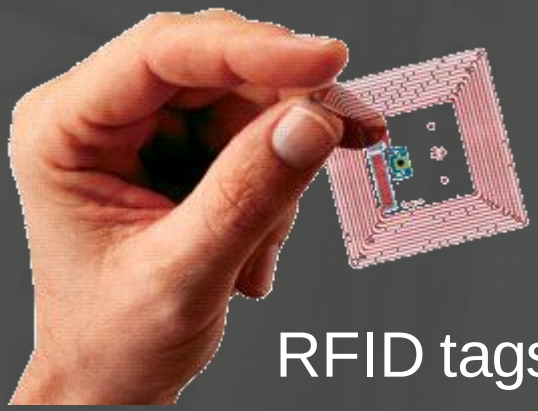
Performances: 1 GOp/s

Power < 1 W



Hearing aids

ULP digital circuits



RFID tags

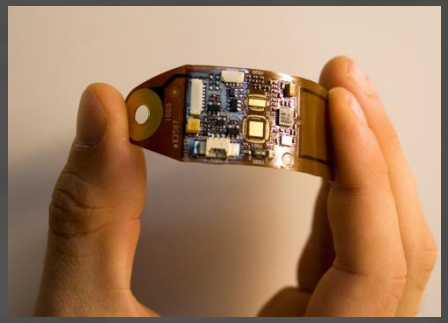
Hearing aids
and biomedical

Ultra-low-power circuits

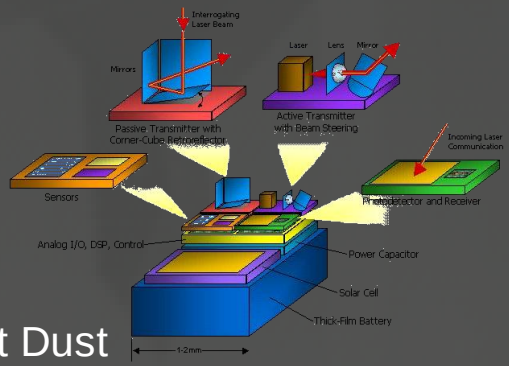
Performances: 10 k - 10 MOp/s

Power < 1µW

Wearable
electronics



Sensor
networks



Smart Dust
[Berkeley]

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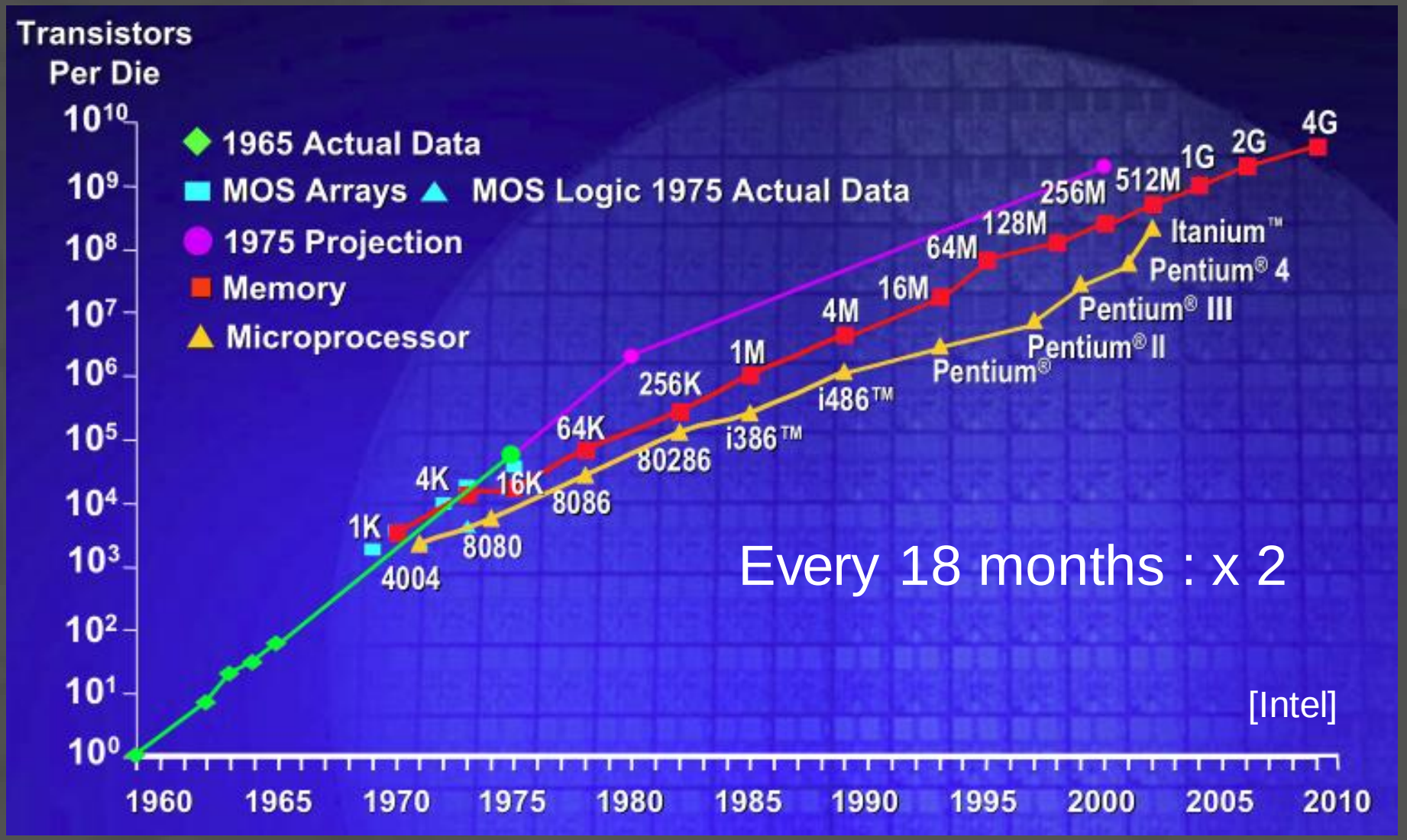
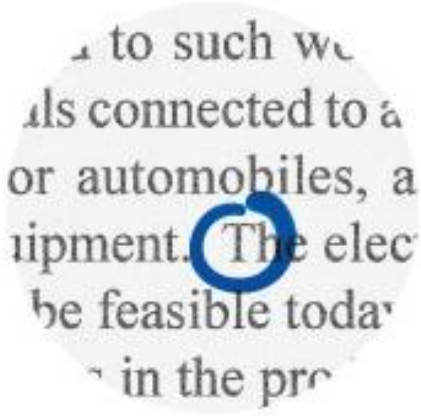
Moore's law (1965)



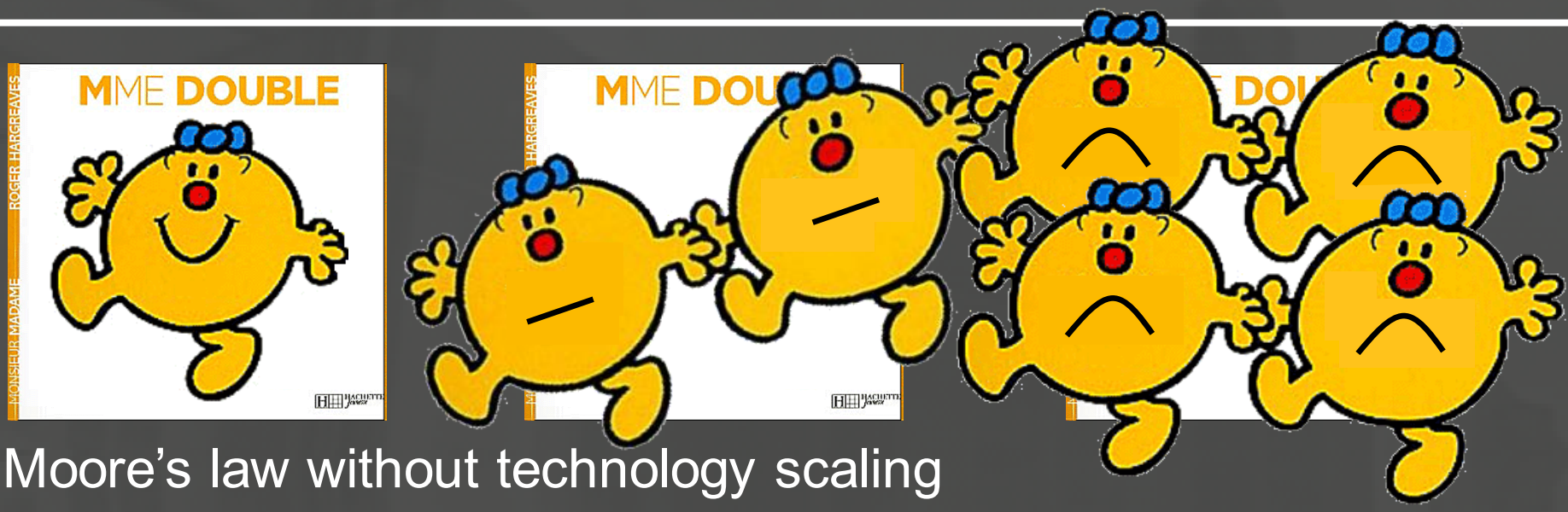
Moore's law today

Gordon Moore estimated in 2003 that the number of transistors shipped in a year had reached about 10,000,000,000,000,000,000 (10^{19}). That's about 100 times the number of ants estimated to be in the world.



The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

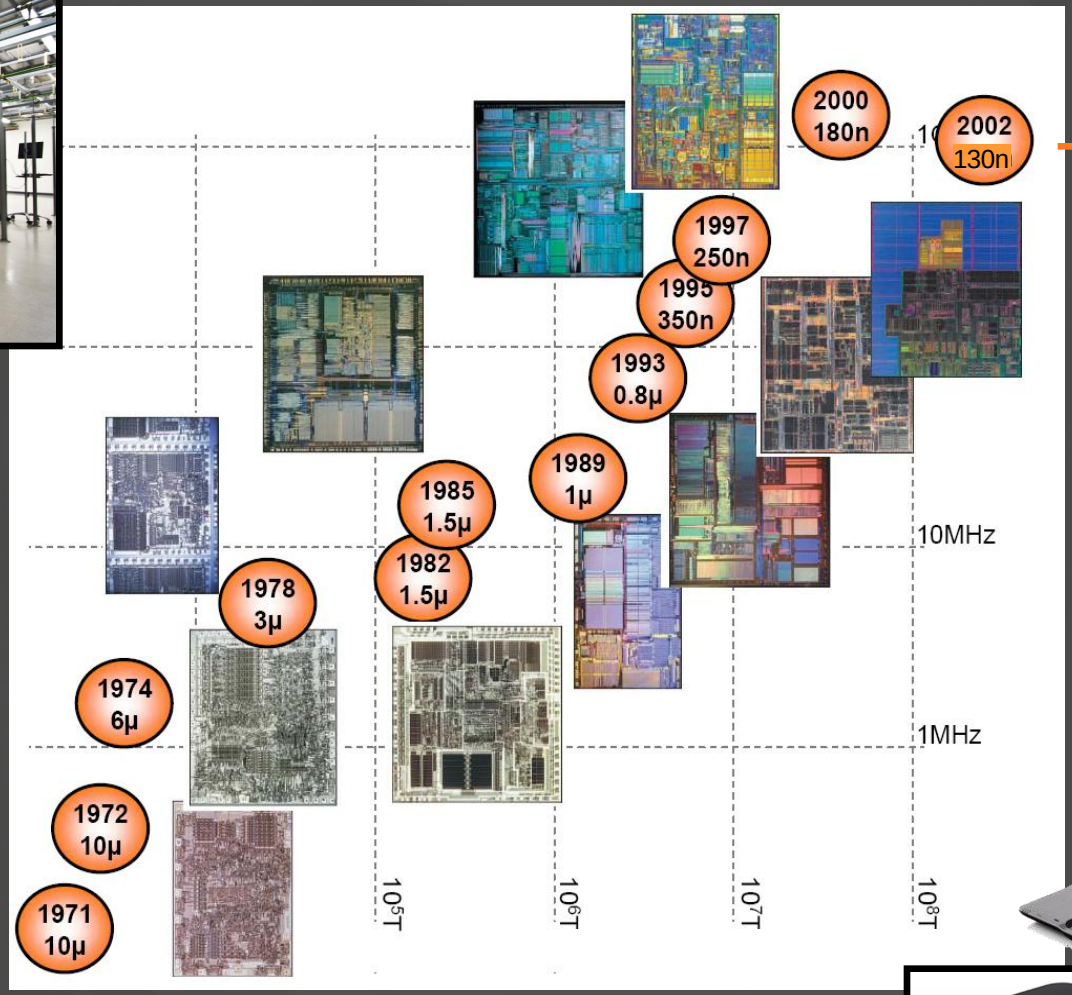
Moore’s law



Moore’s law without technology scaling

Moore’s law with technology scaling

Technology scaling



2008
45nm

100 MHz

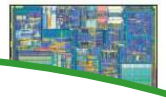
10 MHz

1 MHz

10^4 10^5 10^6 10^7

Transistor count

Technology scaling

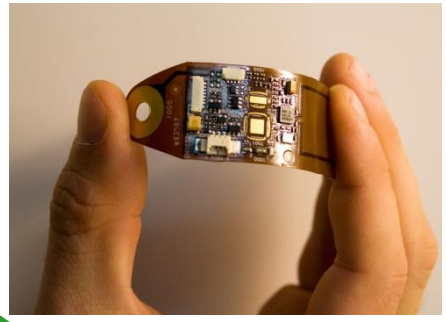


2000

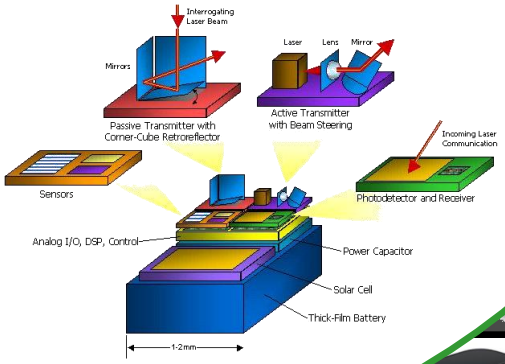
2002
130n

2008
45nm

ULP circuits

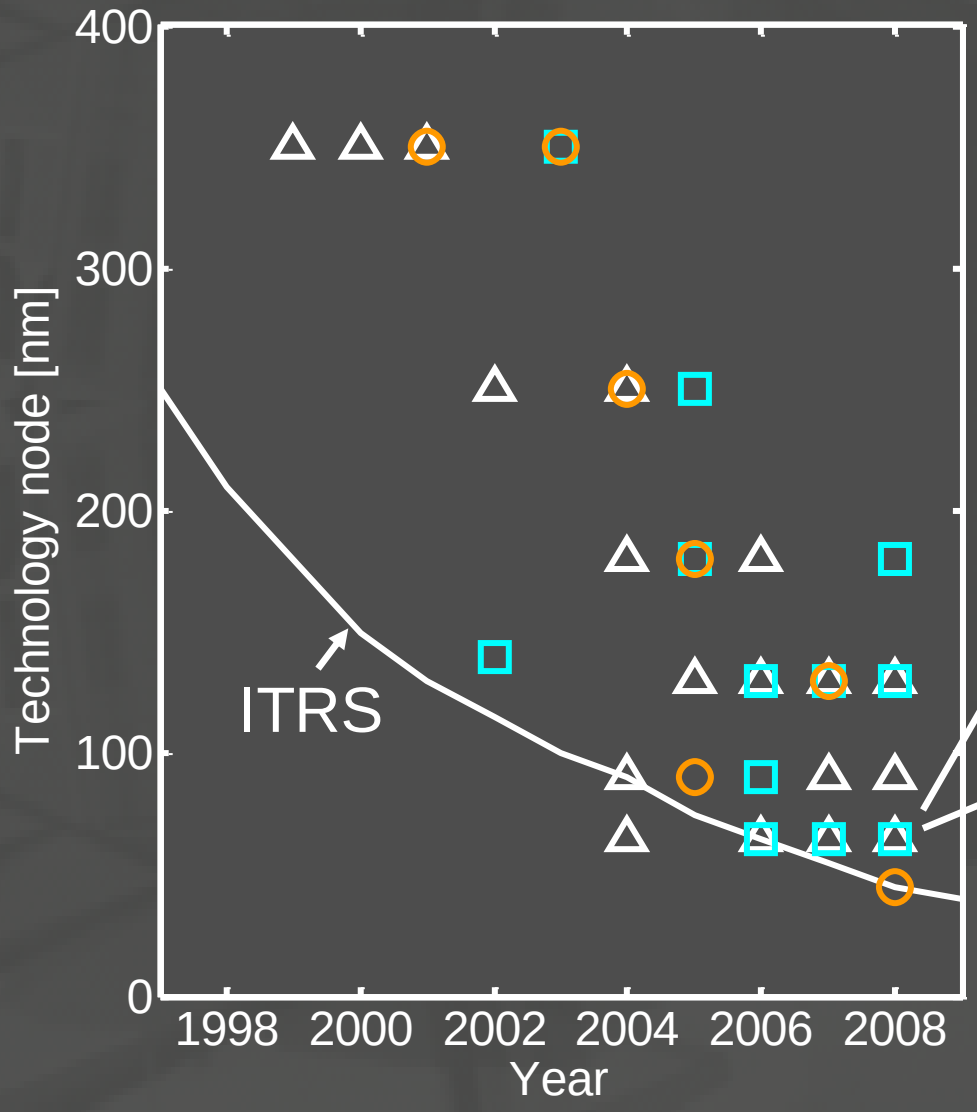


?

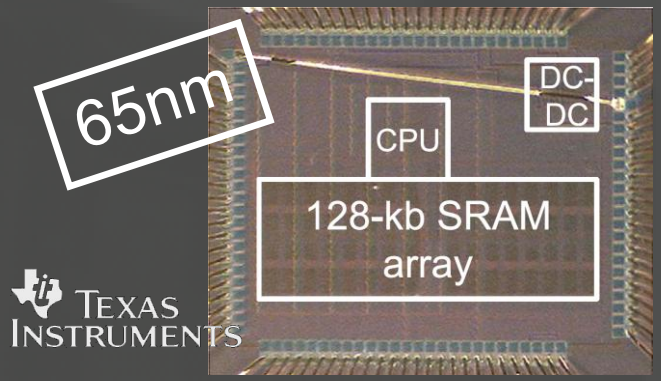


Transistor count

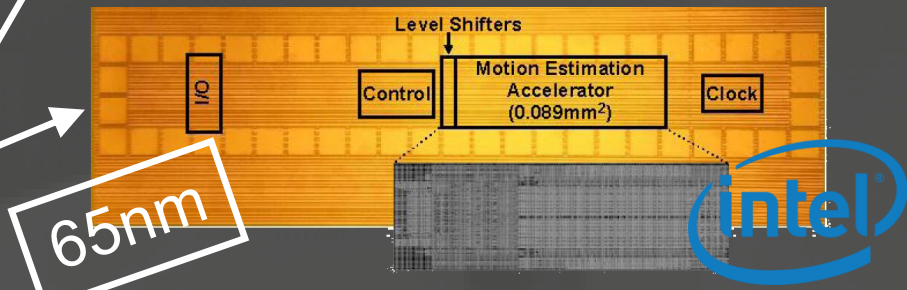
Trend in ULP digital circuits



Last chips [IEEE ISSCC'08]:



Ultra-low-power 0.3V µC for biomedical applications [Kwong]

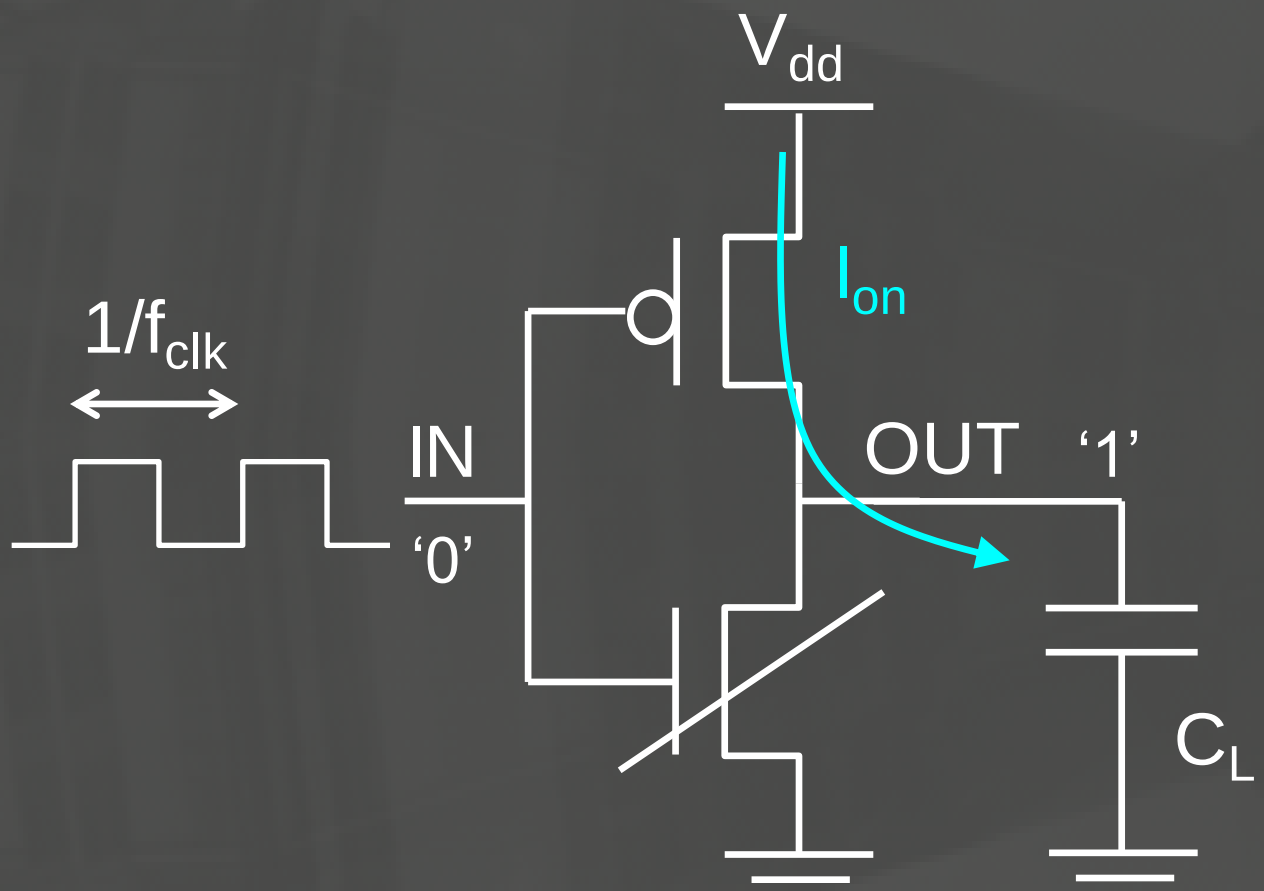


Ultra-low-power 0.32V motion estimator [Kaul]

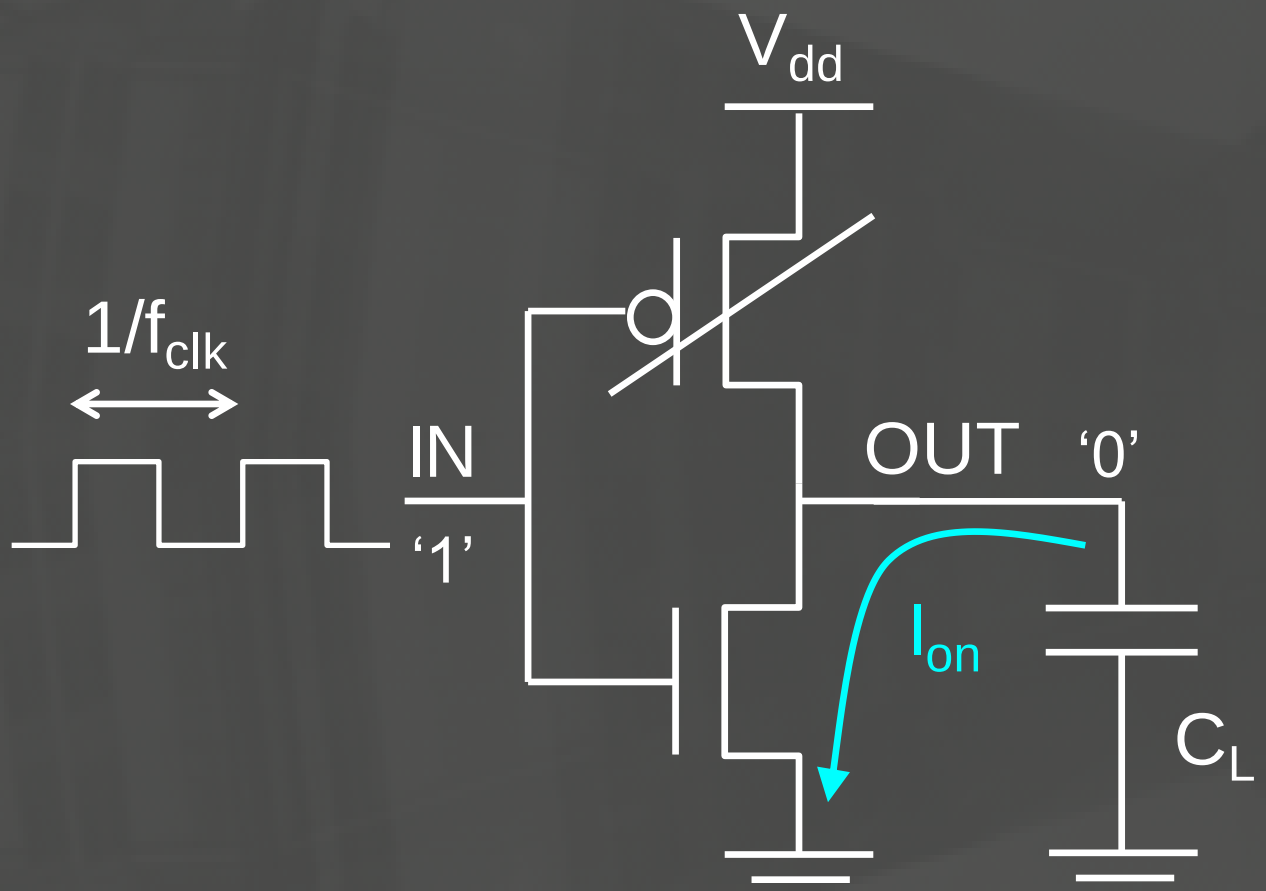
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching E_{min}
- Reducing E_{min}
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits

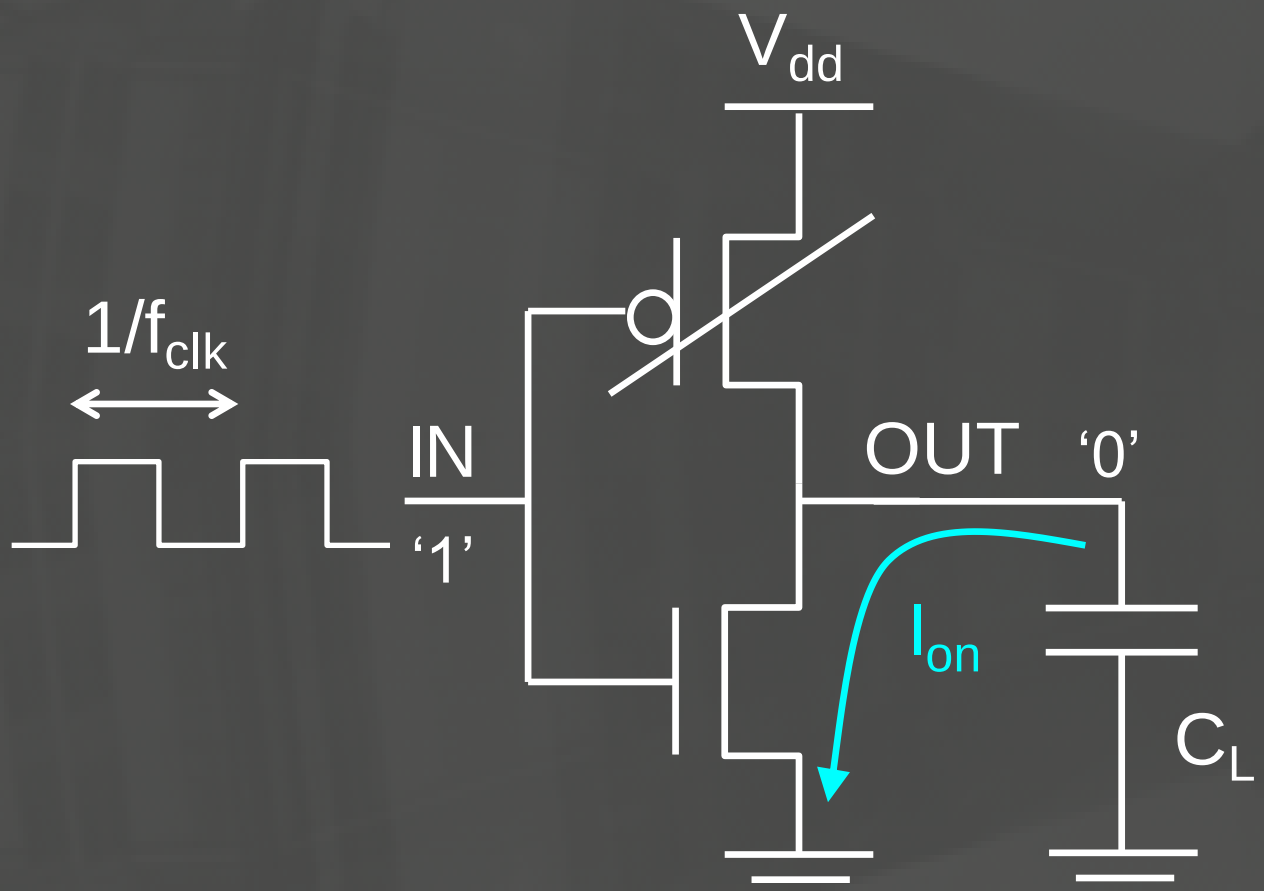
Sources of power dissipation



Sources of power dissipation

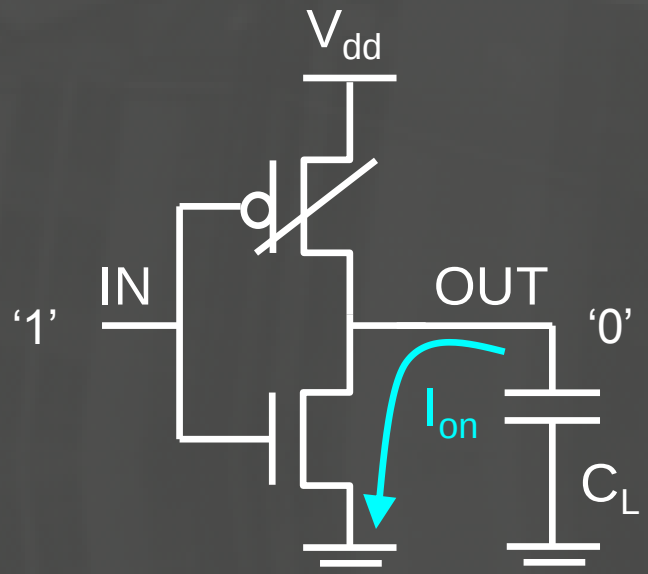


Sources of power dissipation



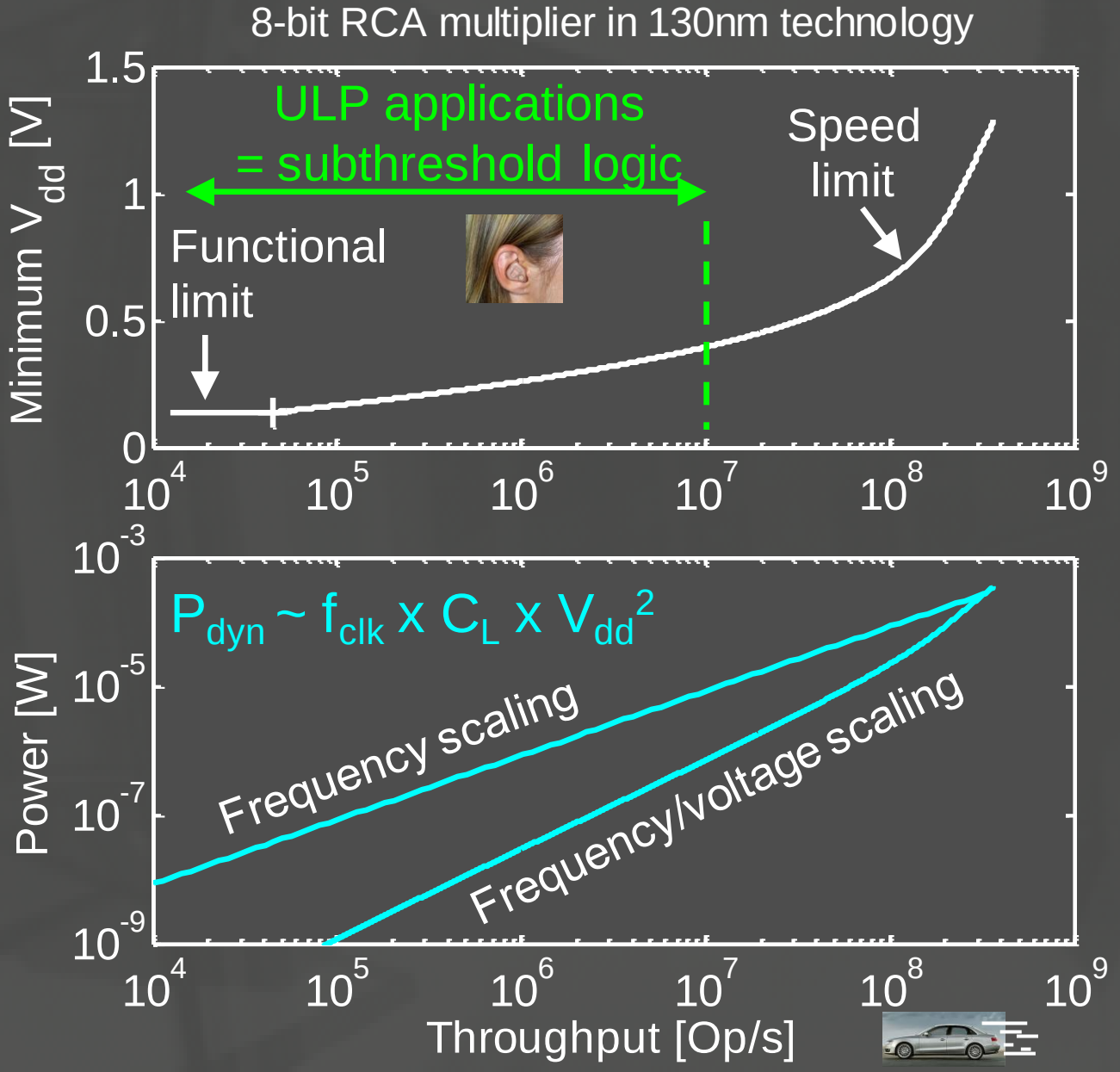
$$P_{dyn} \sim f_{clk} \times C_L \times V_{dd}^2$$

Sources of power dissipation

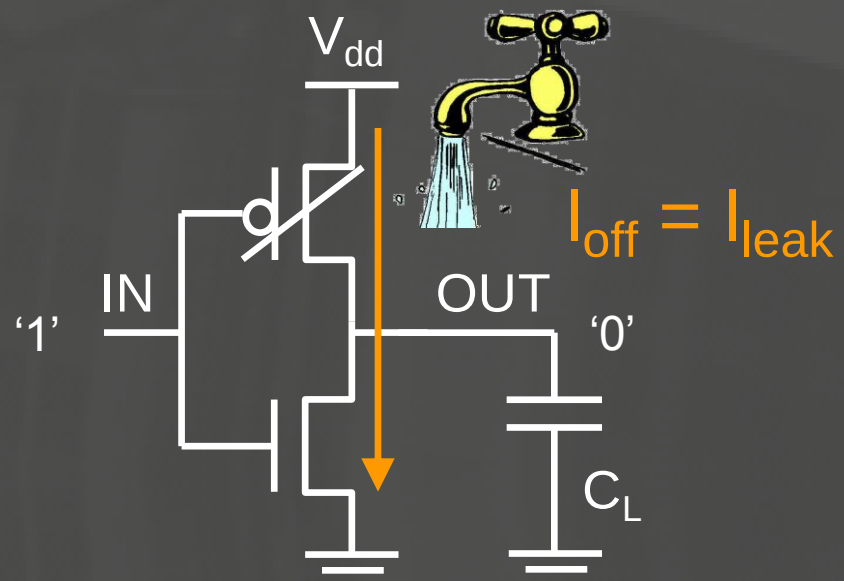


$$P_{dyn} \sim f_{clk} \times C_L \times V_{dd}^2$$

Power consumption



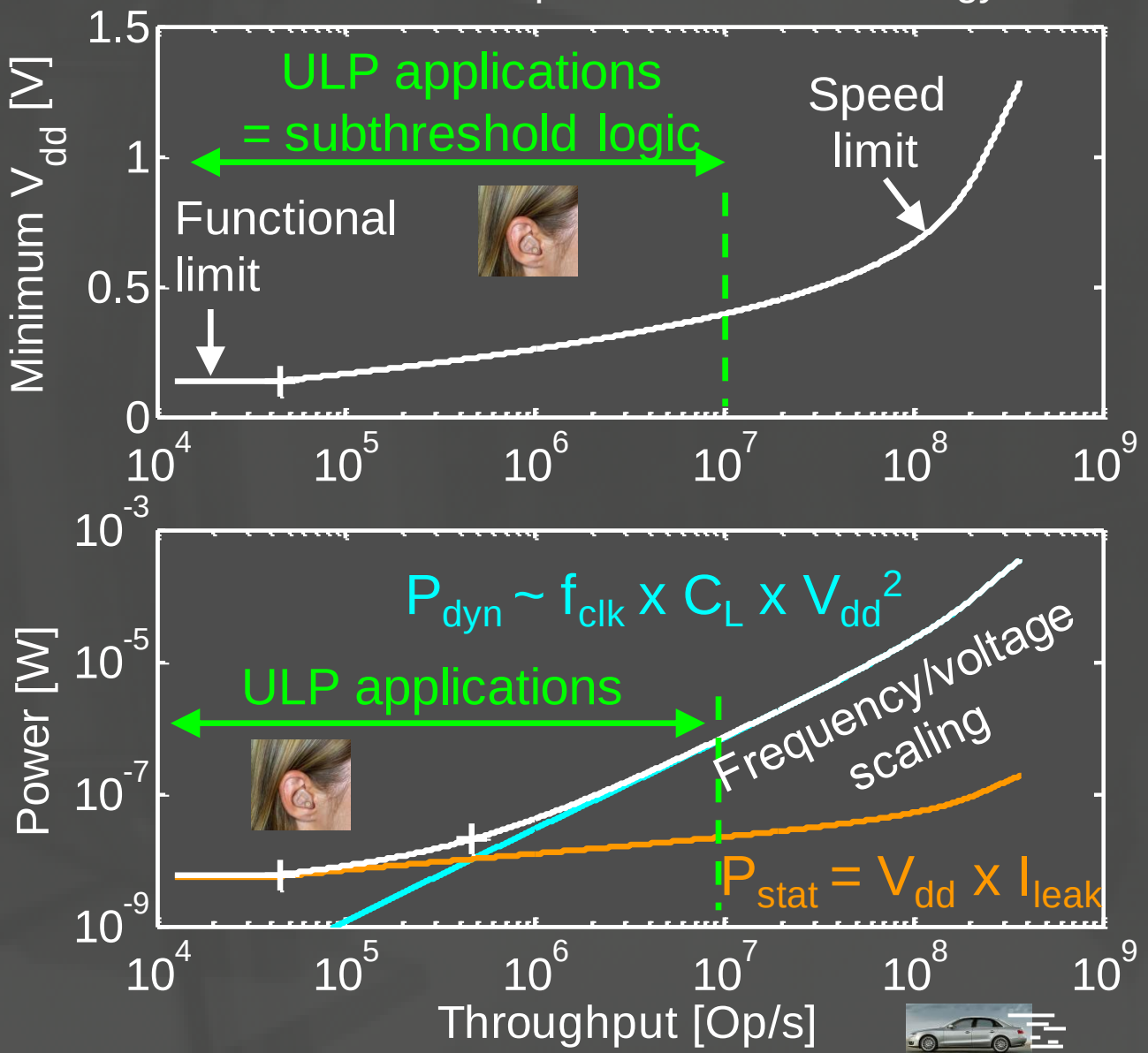
Sources of power dissipation



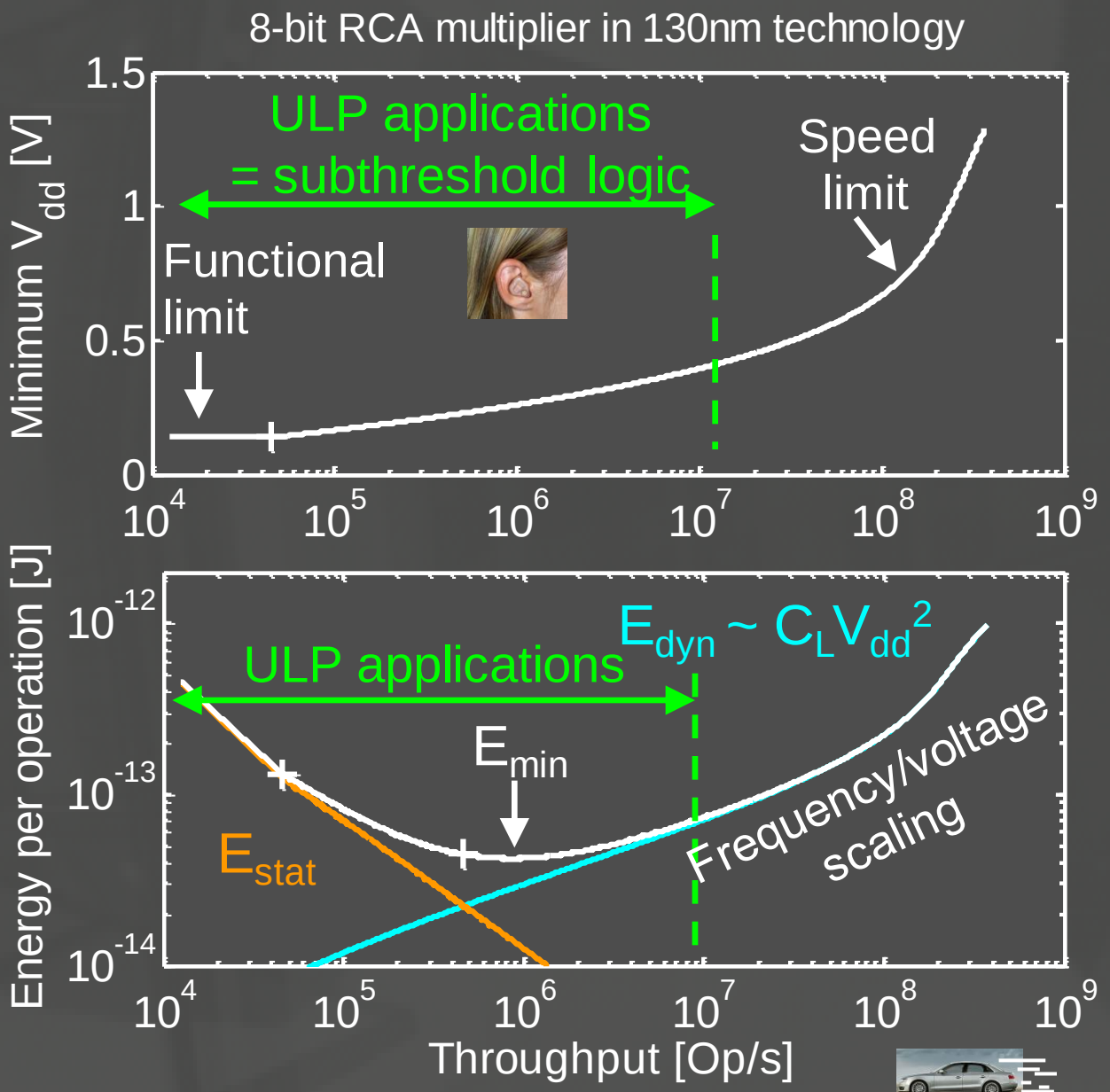
$I_{off} = I_{leak}$

$P_{stat} \sim V_{dd} \times I_{leak}$

Power consumption



Energy consumption



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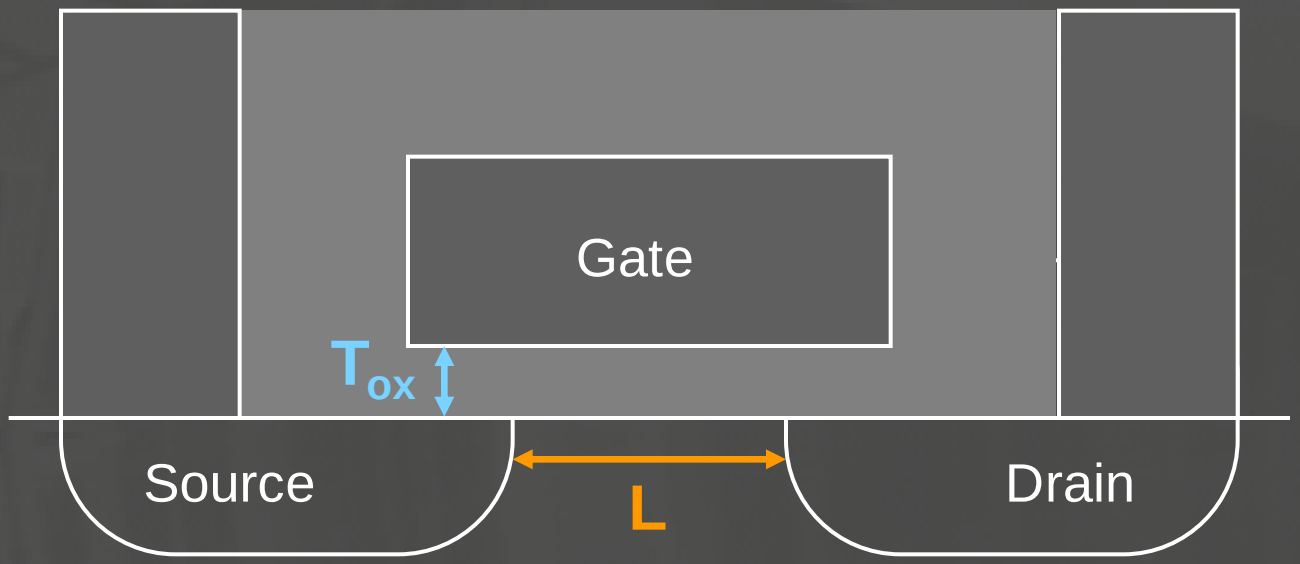
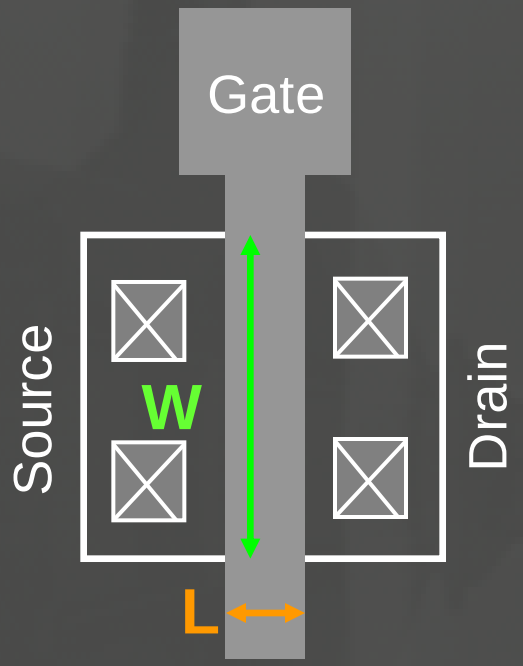
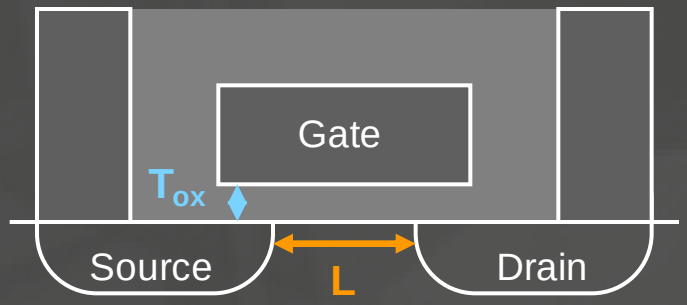
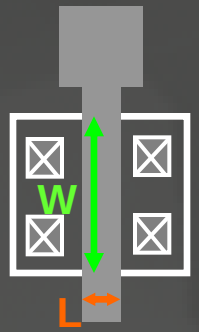
Impact of technology scaling





T_{ox}, L, W ~ 1/S





Impact of technology scaling

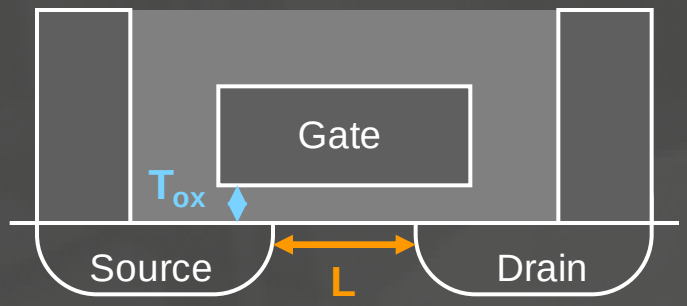
- I_{on} ↑
- C_L ↓
- I_{leak} ↑

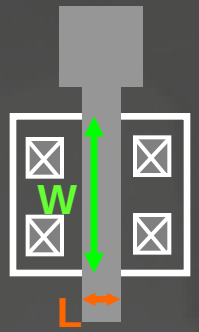
→ Speed ↑  → Reduce V_{dd} 

$E_{dyn} \sim C_L V_{dd}^2$

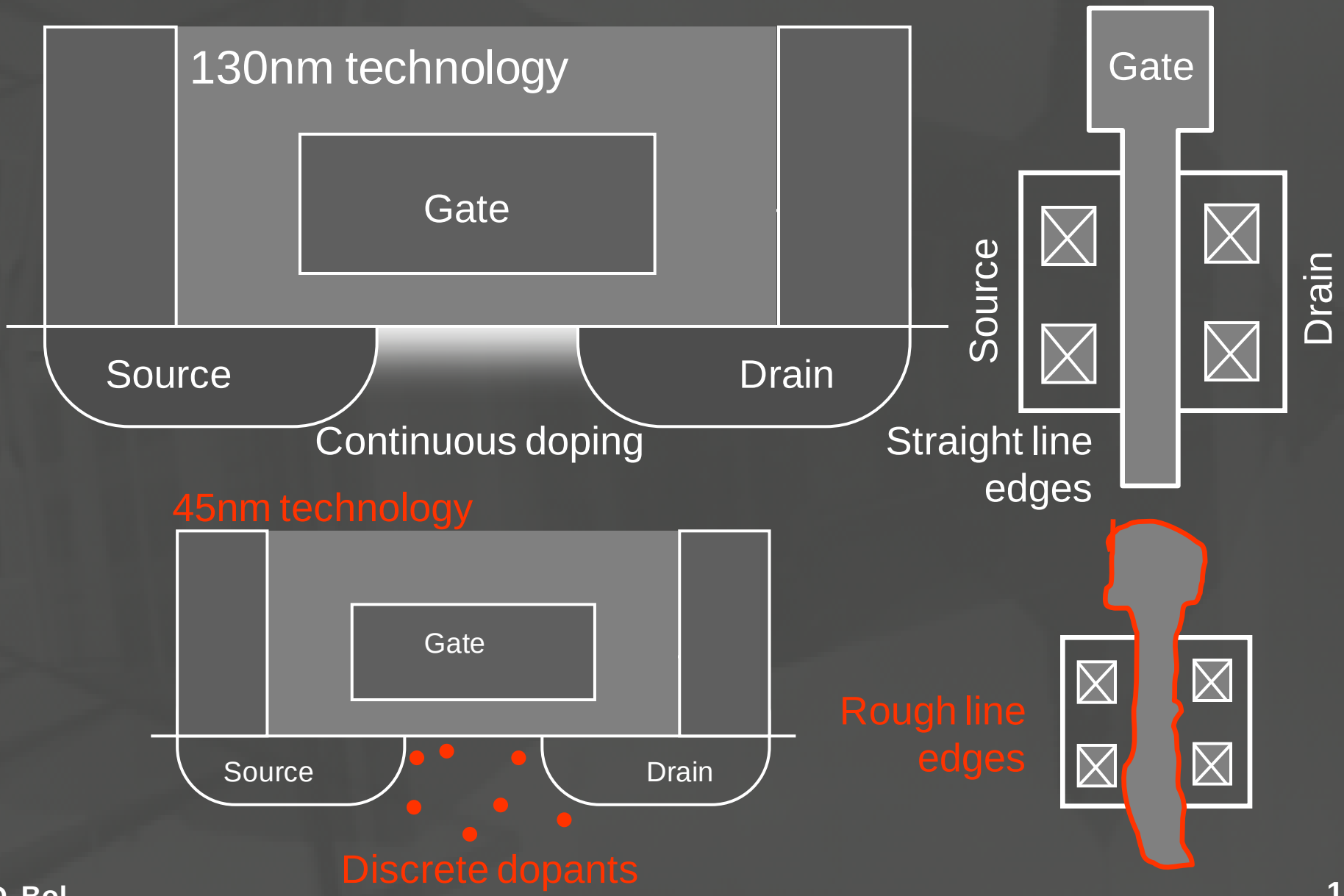
$E_{stat} \sim I_{leak} V_{dd}^2$

- Variability !

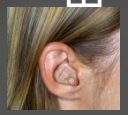




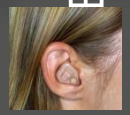
Variability



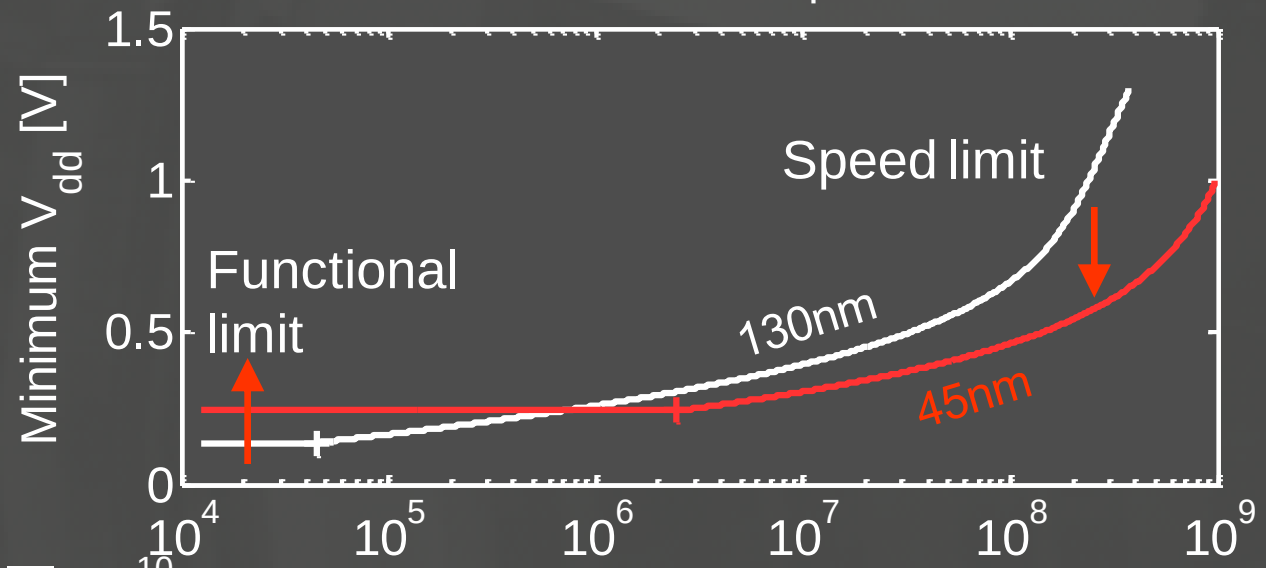
Impact of technology scaling

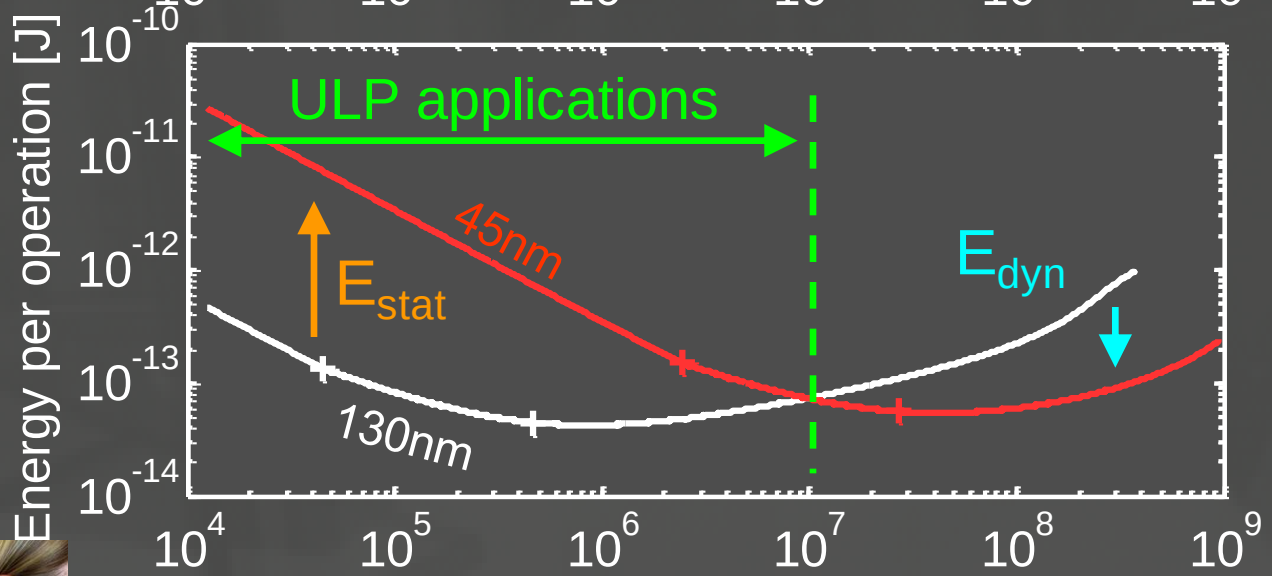


Impact of technology scaling

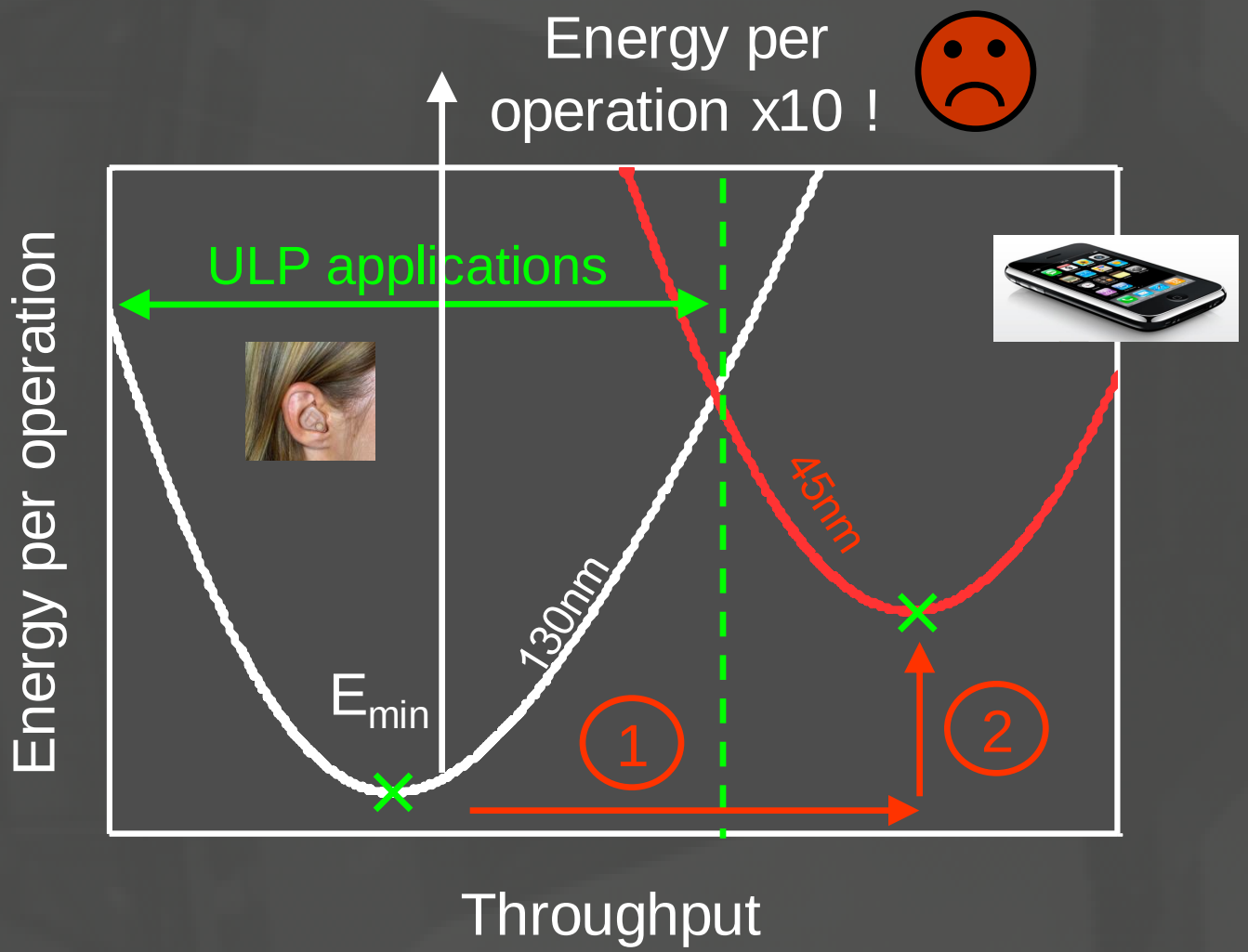


8-bit RCA multiplier

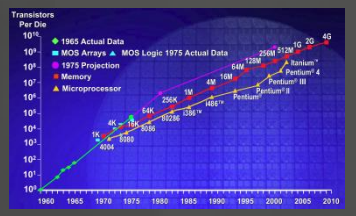




Impact of technology scaling

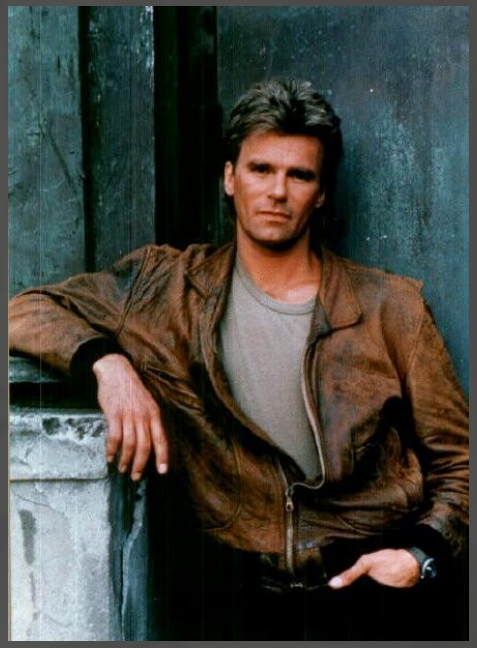


What if you have to s e ?

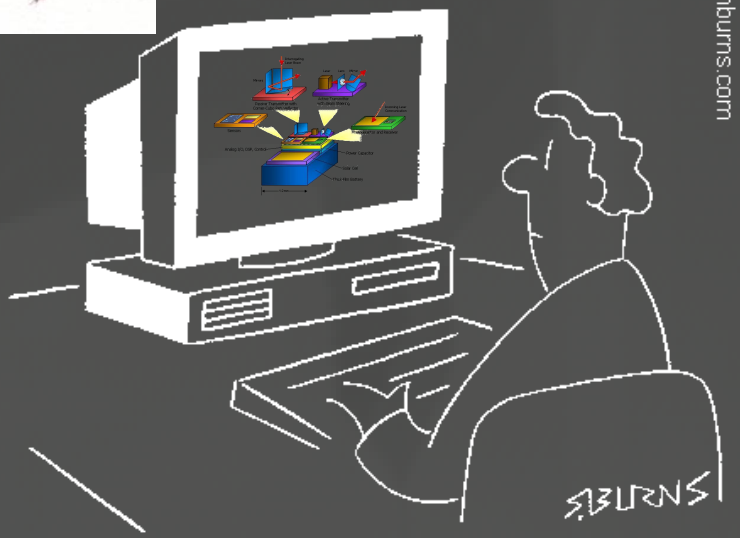


Famous Intel co-founder

Scale,
scale,
scale…



DIY



D. Bol

Outline

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- Reducing E_{min} (2)
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1 Technology versatility

45nm technology

High-Performance/ General-Purpose

- Short L_g
- Thin T_{ox}
- Low V_t
- Mid V_{dd}

→

- High I_{on}
- High I_{leak}

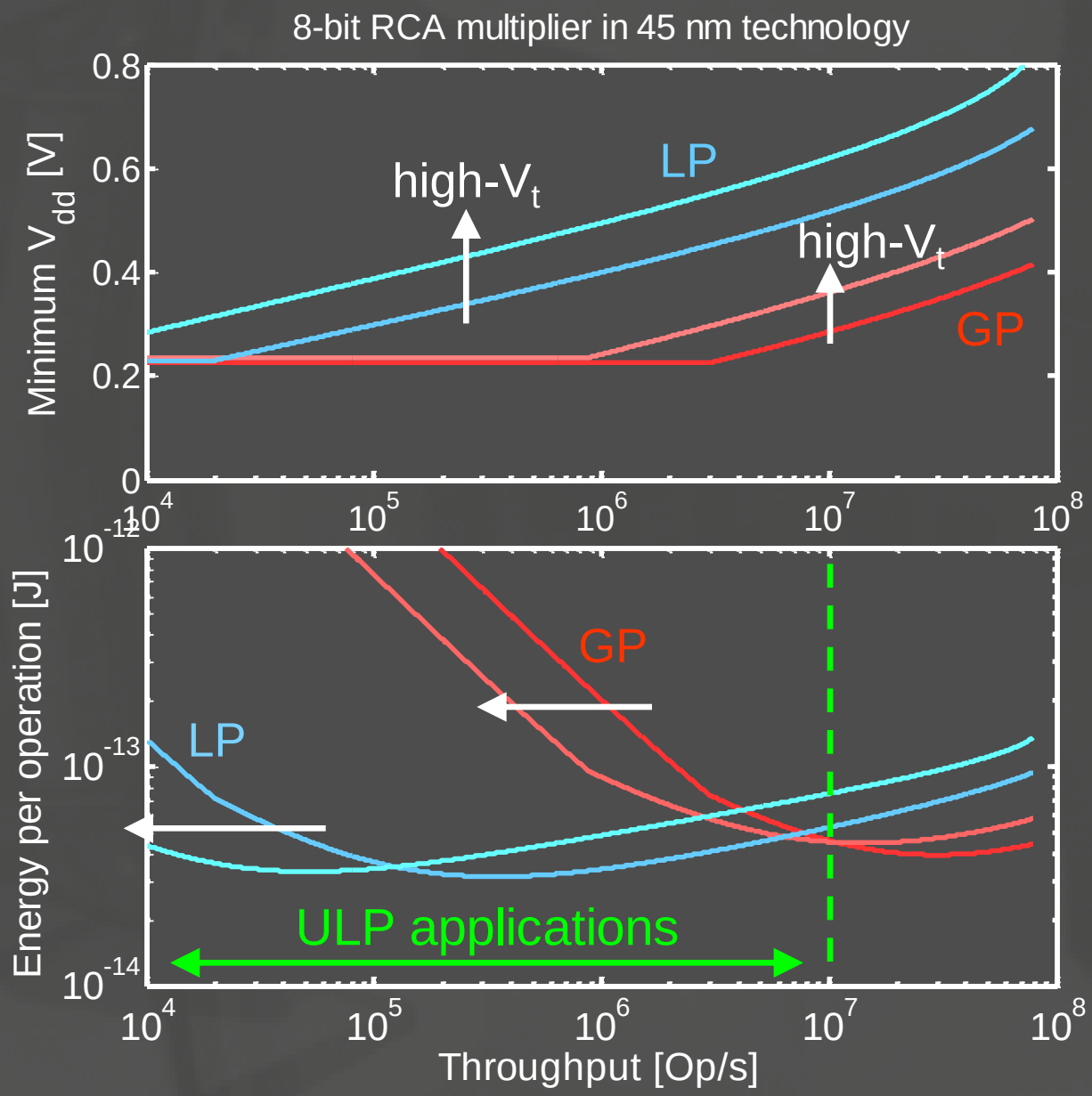
Low-Power

- Mid L_g
- Mid T_{ox}
- High V_t
- High V_{dd}

→

- Low I_{on}
- Low I_{leak}

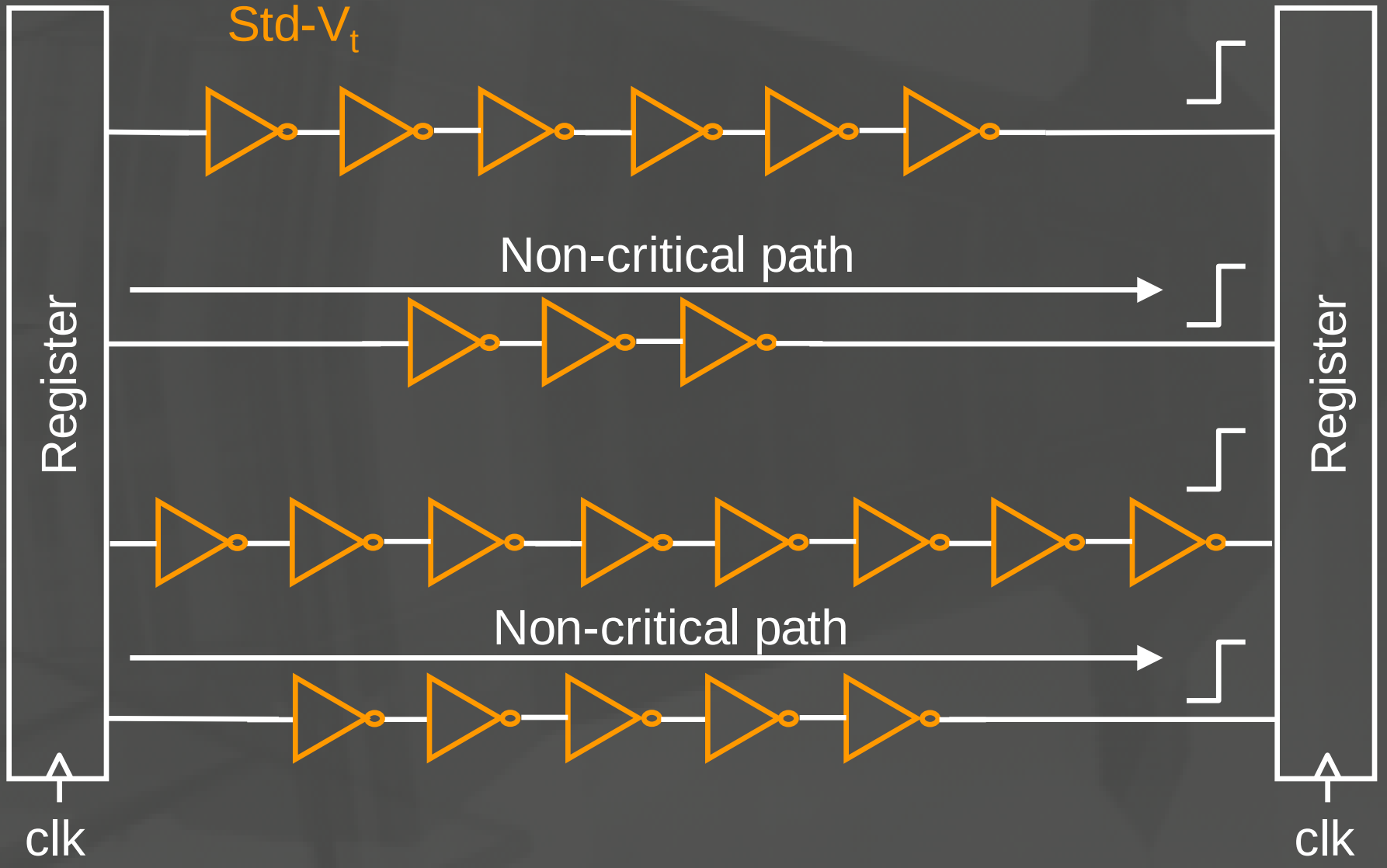
Technology selection



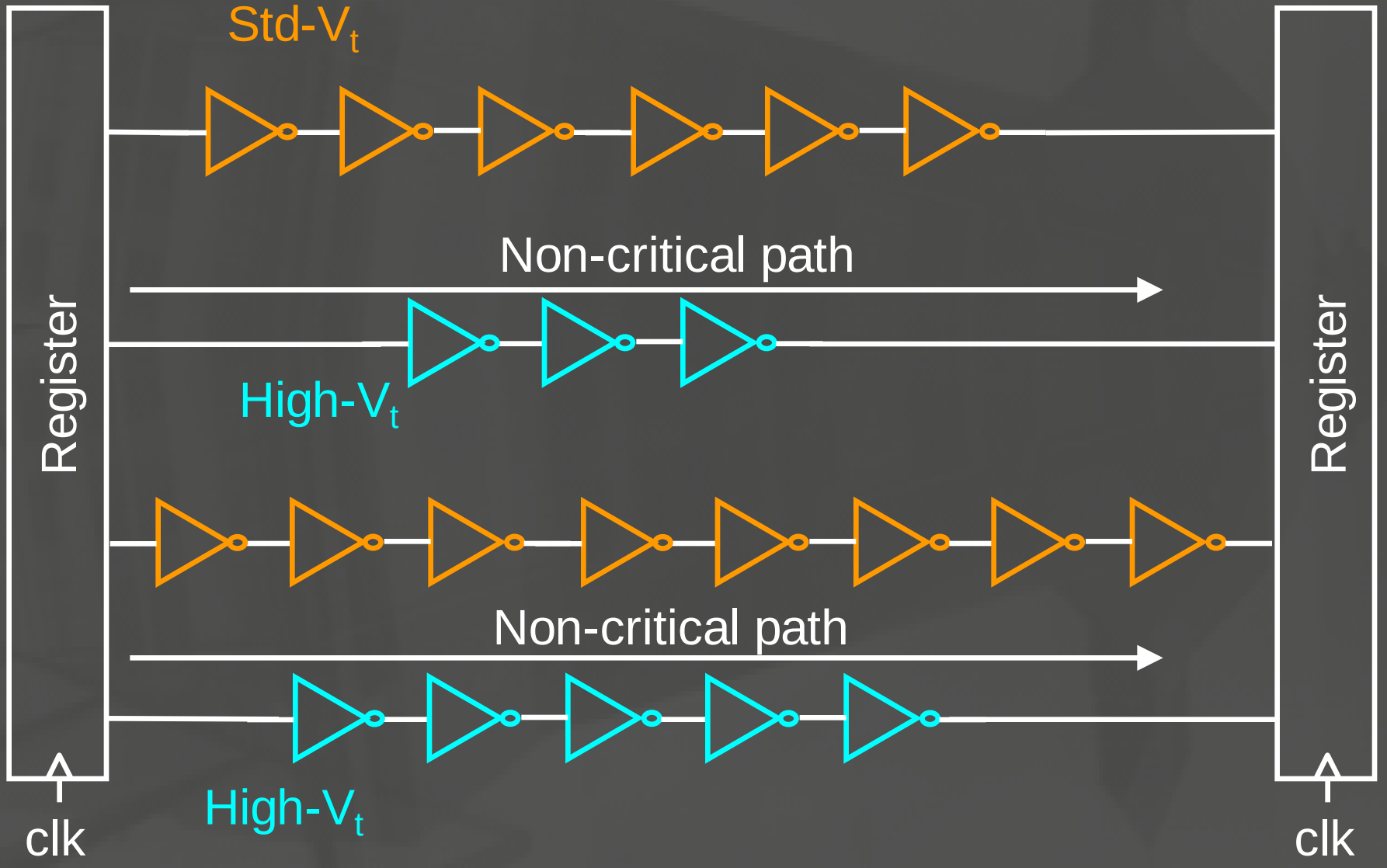
General-Purpose

Low-Power

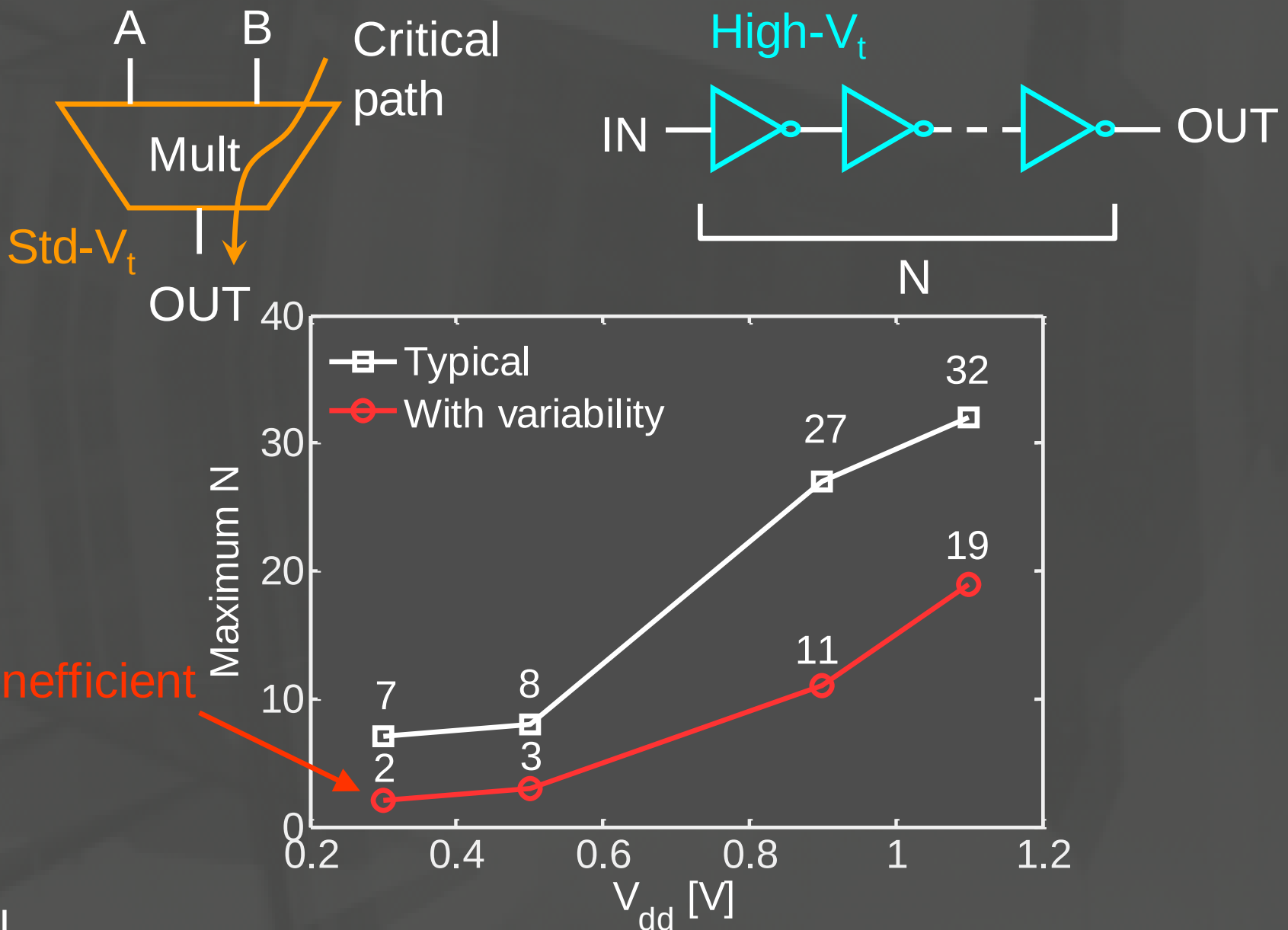
Dual-V_t assignement



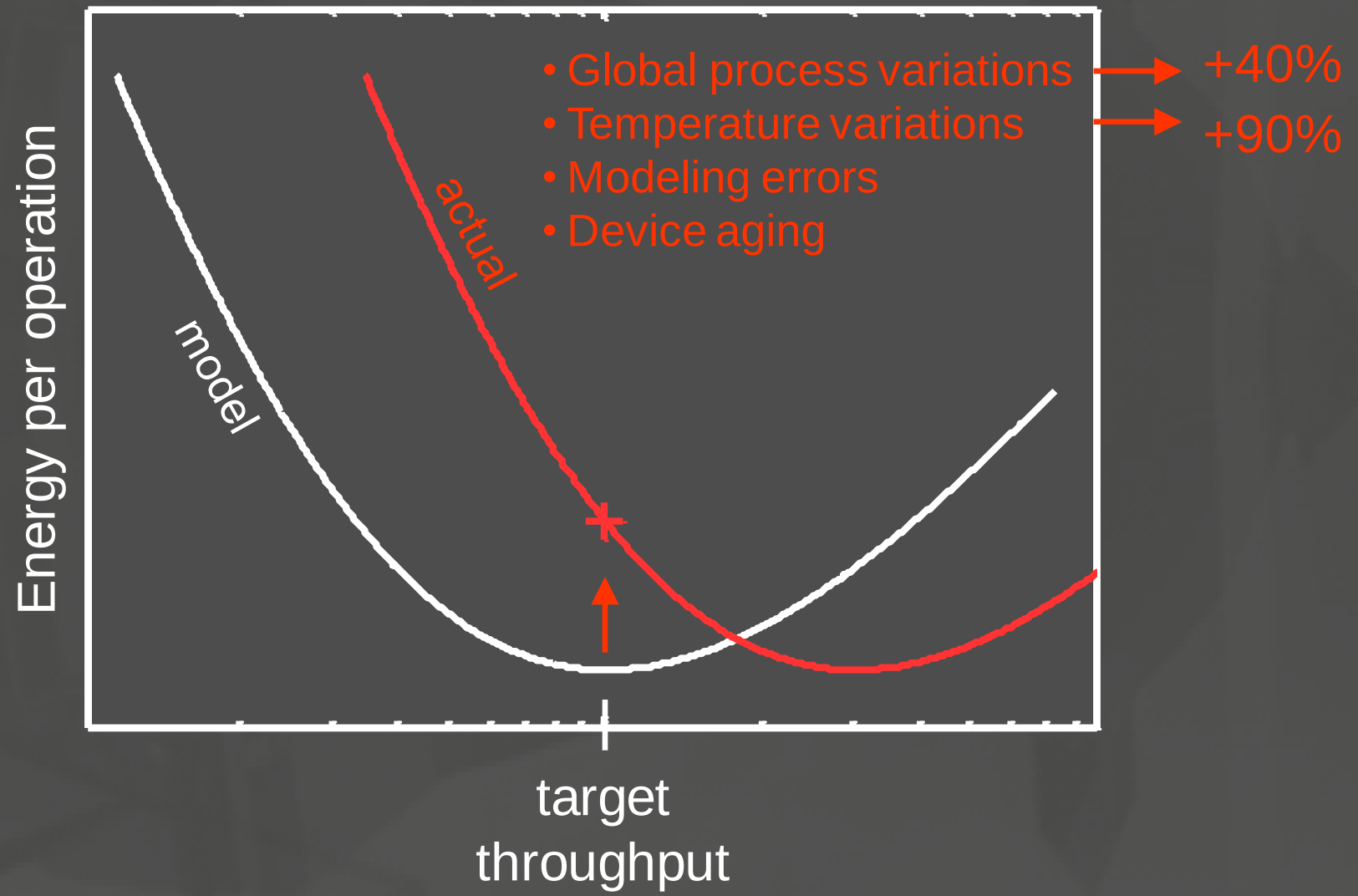
Dual-V_t assignement



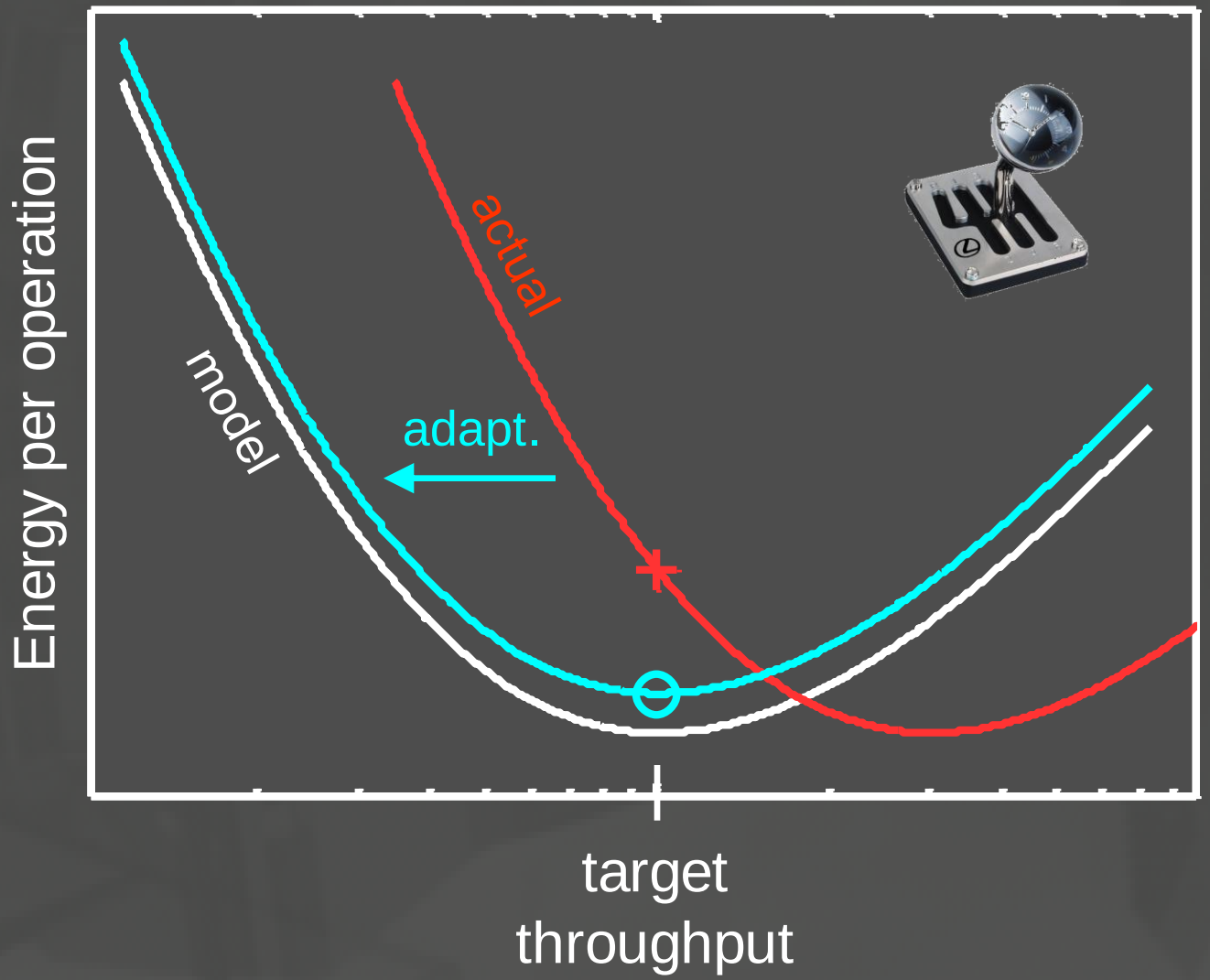
Dual-V_t assignement



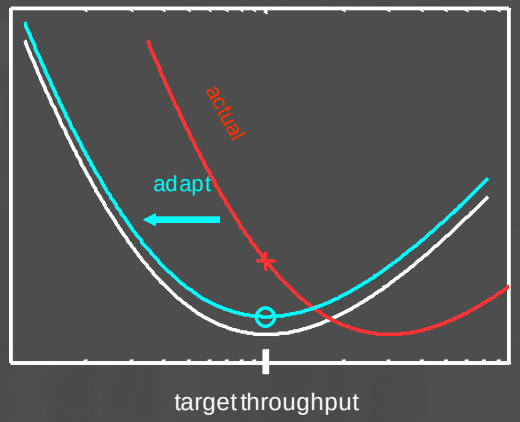
Circuit adaptation

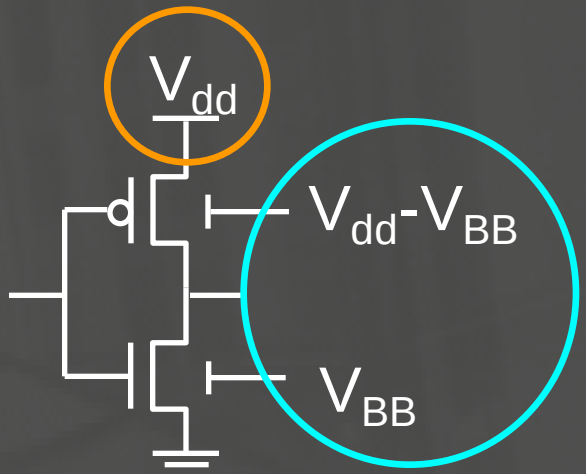


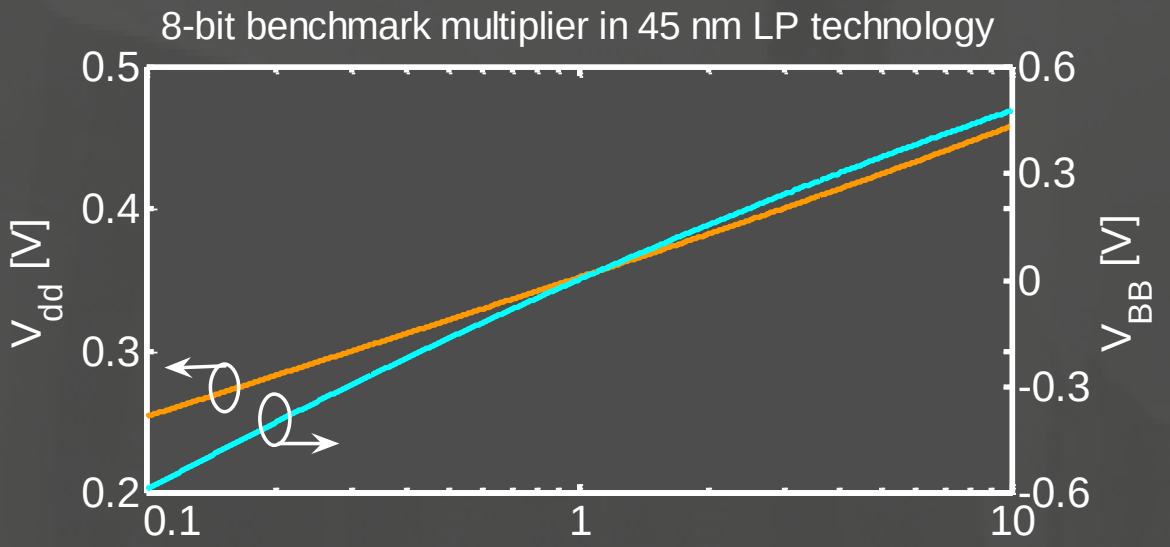
Circuit adaptation

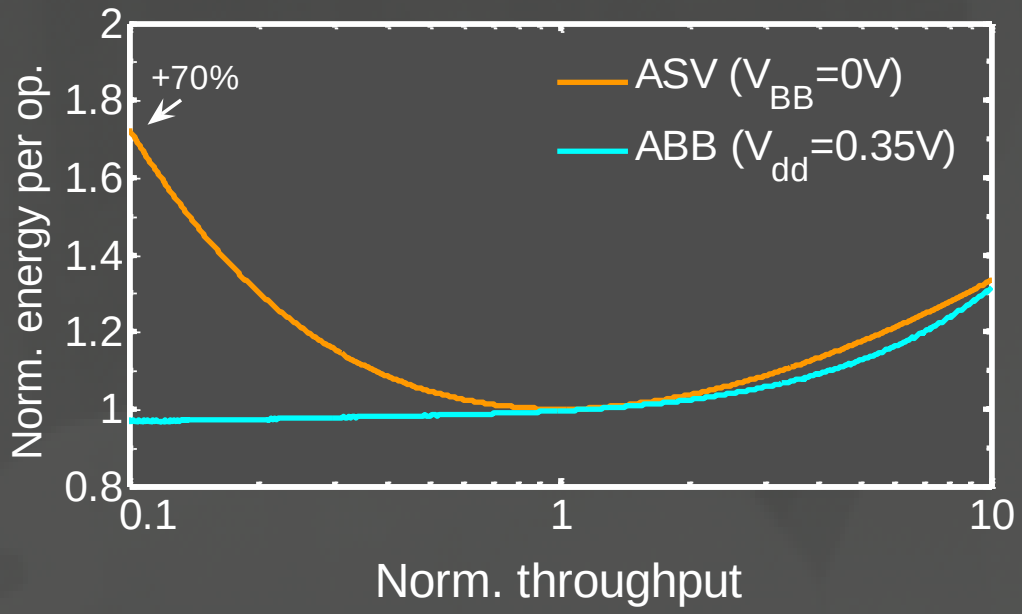


Circuit adaptation

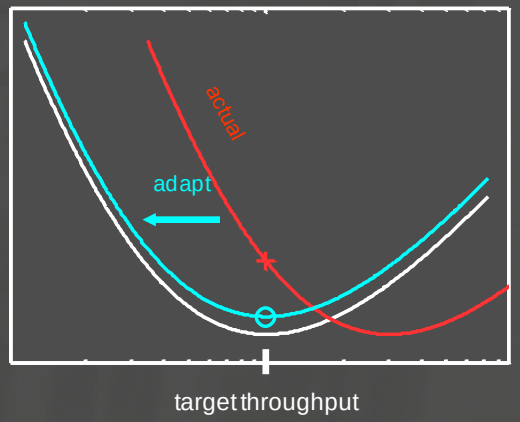


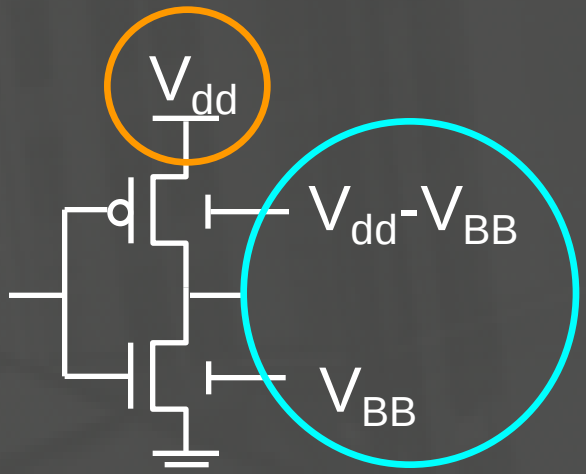


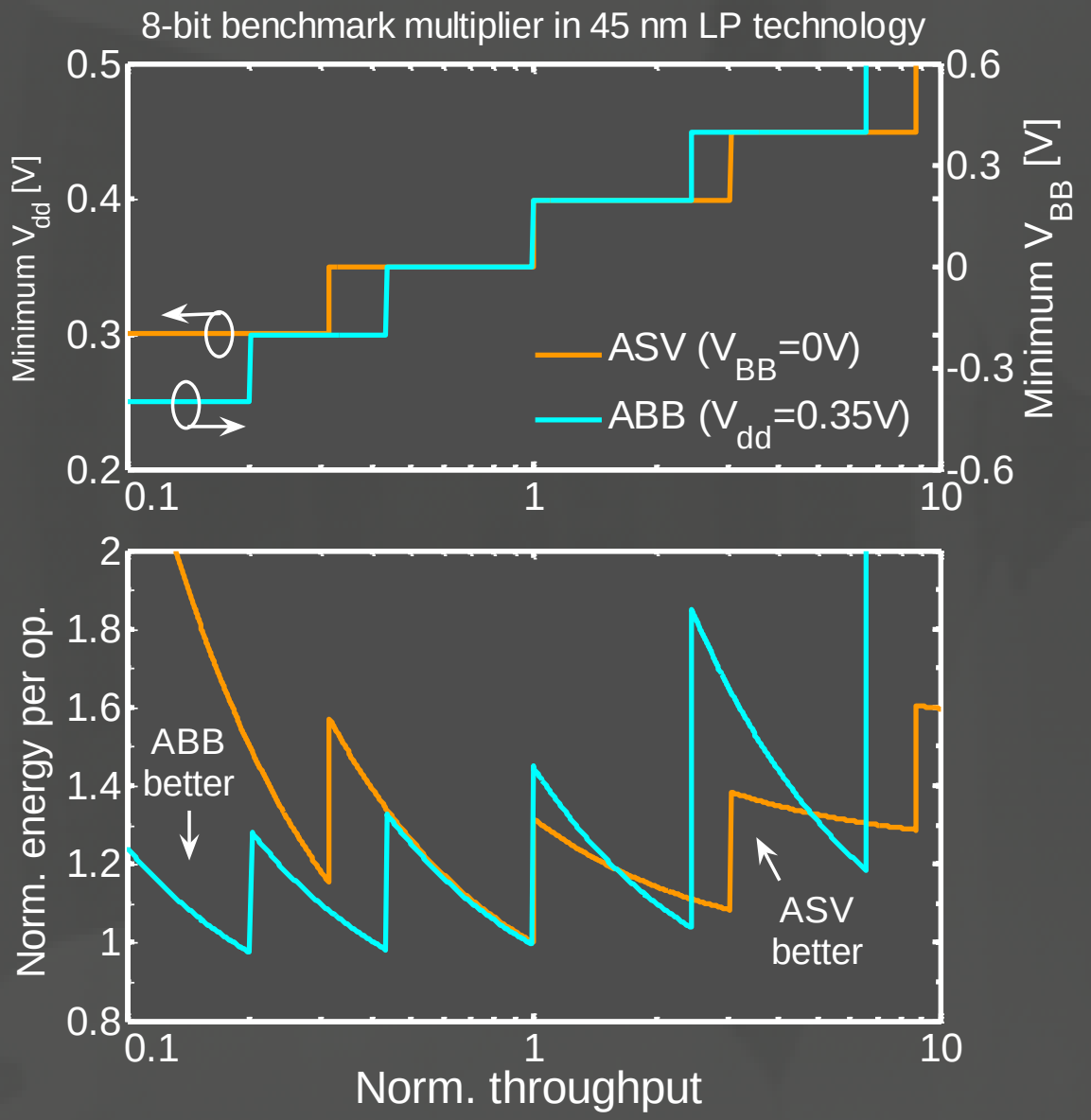




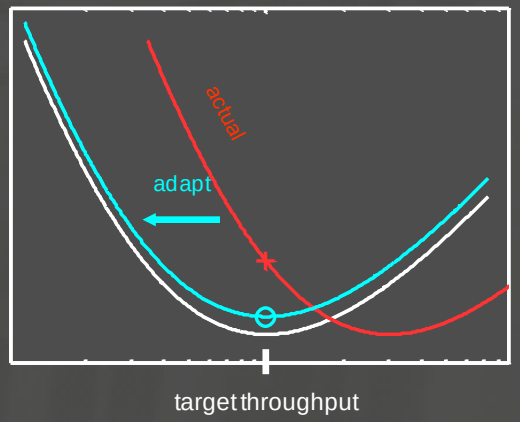
Circuit adaptation

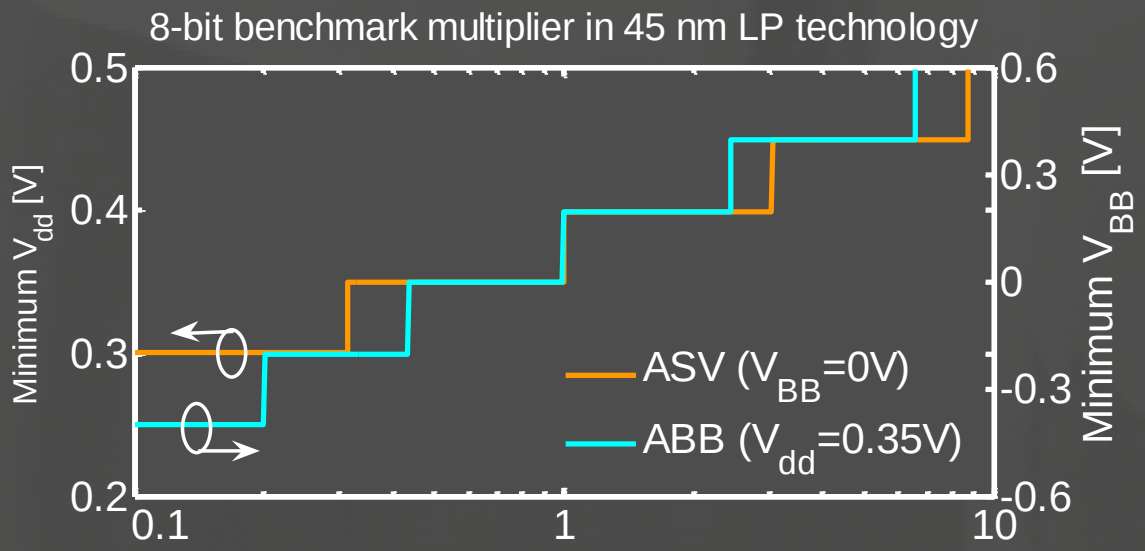






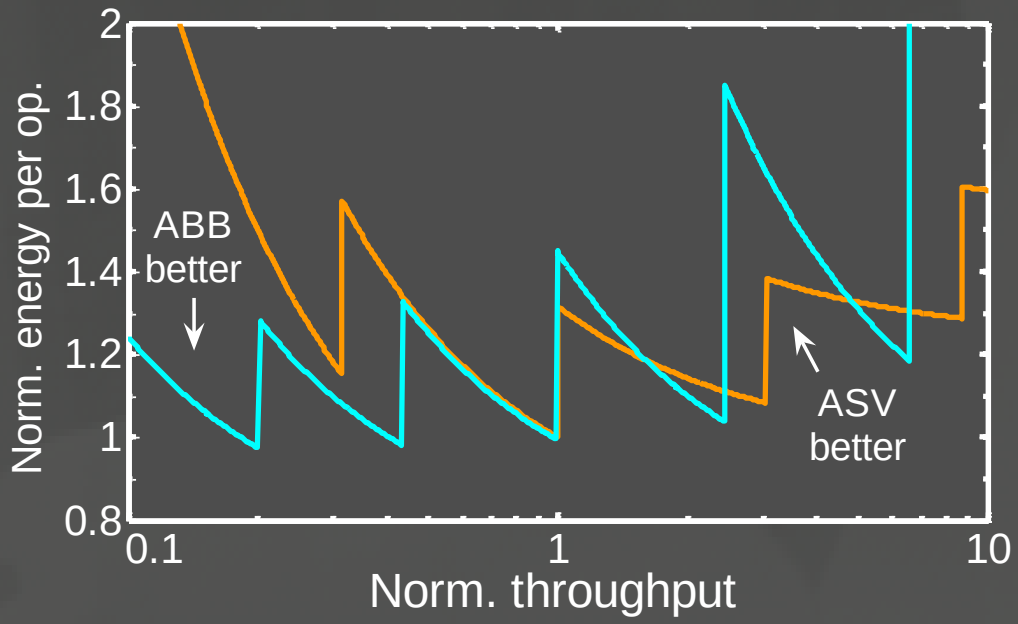
Circuit adaptation





Reverse body bias is fine in 45 nm LP technology

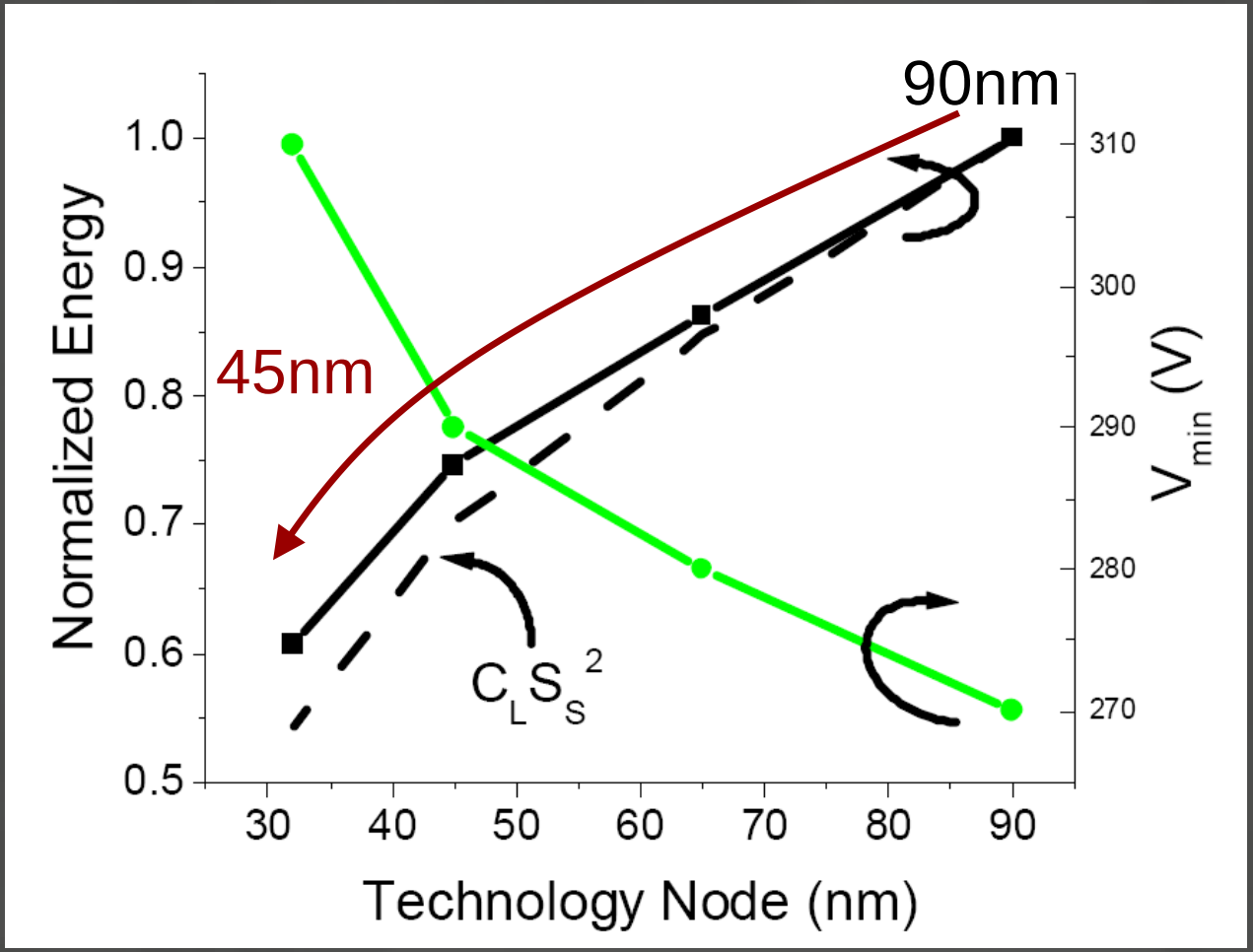
Problem in 45 nm GP!
What at 32 nm?



Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching E_{min} (1)
- Reducing E_{min} (2)
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits

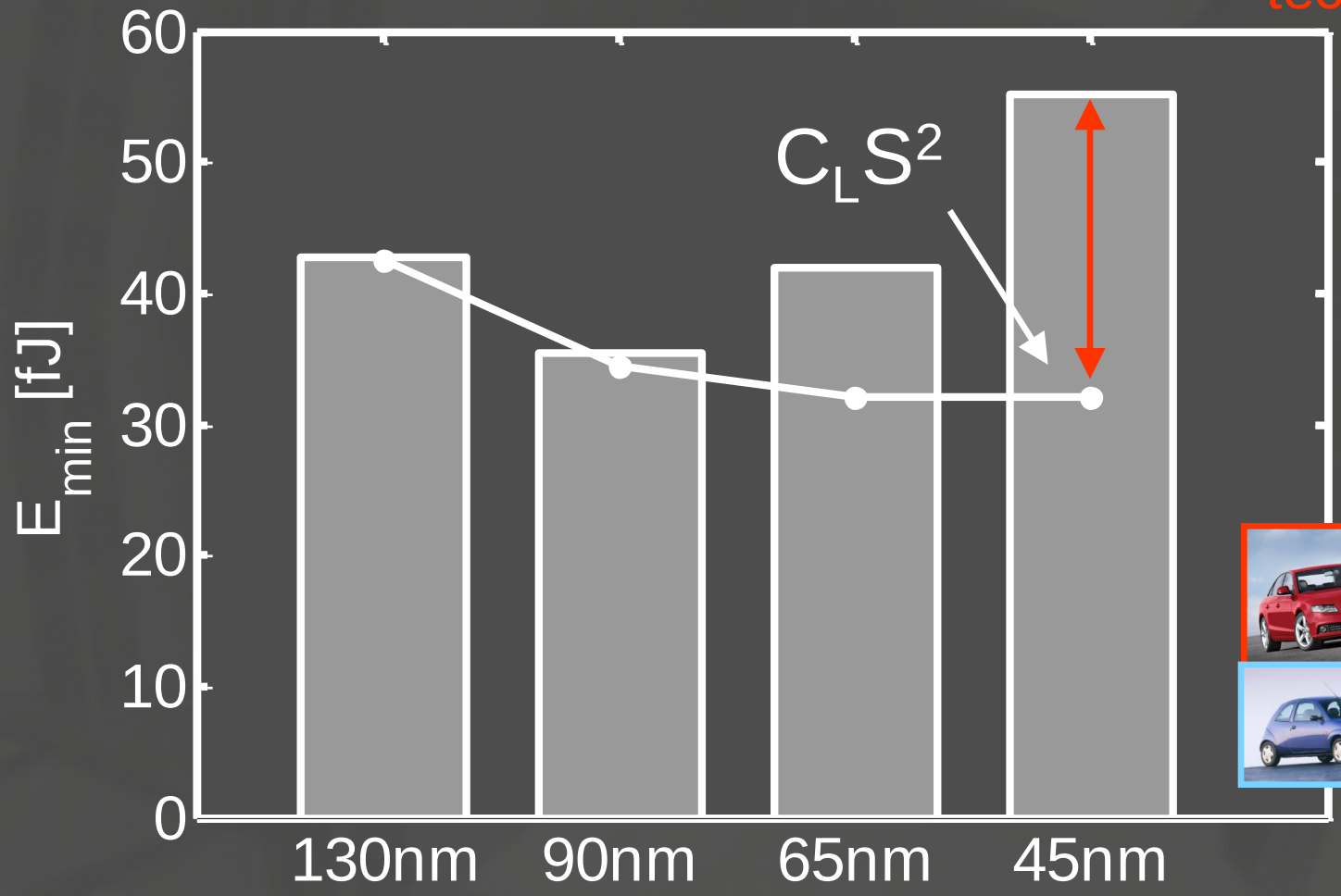
E_{min} modeling



[Hanson, IEEE TED, pp. 175-185, 2008]

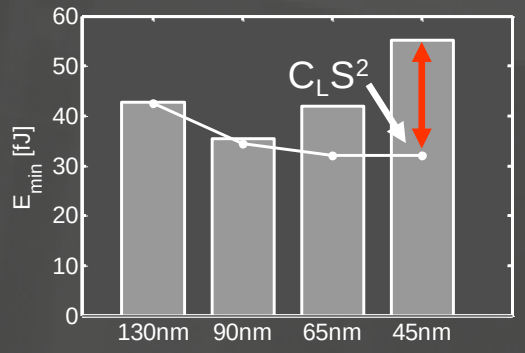
Evolution of E_{min}

New effects in nanometer technologies



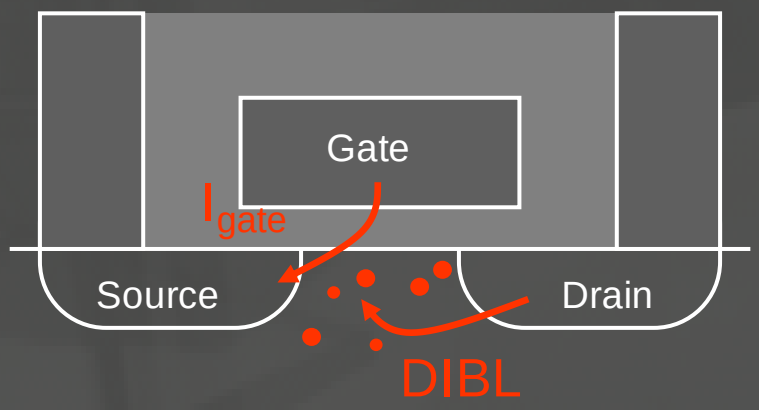
In all flavors

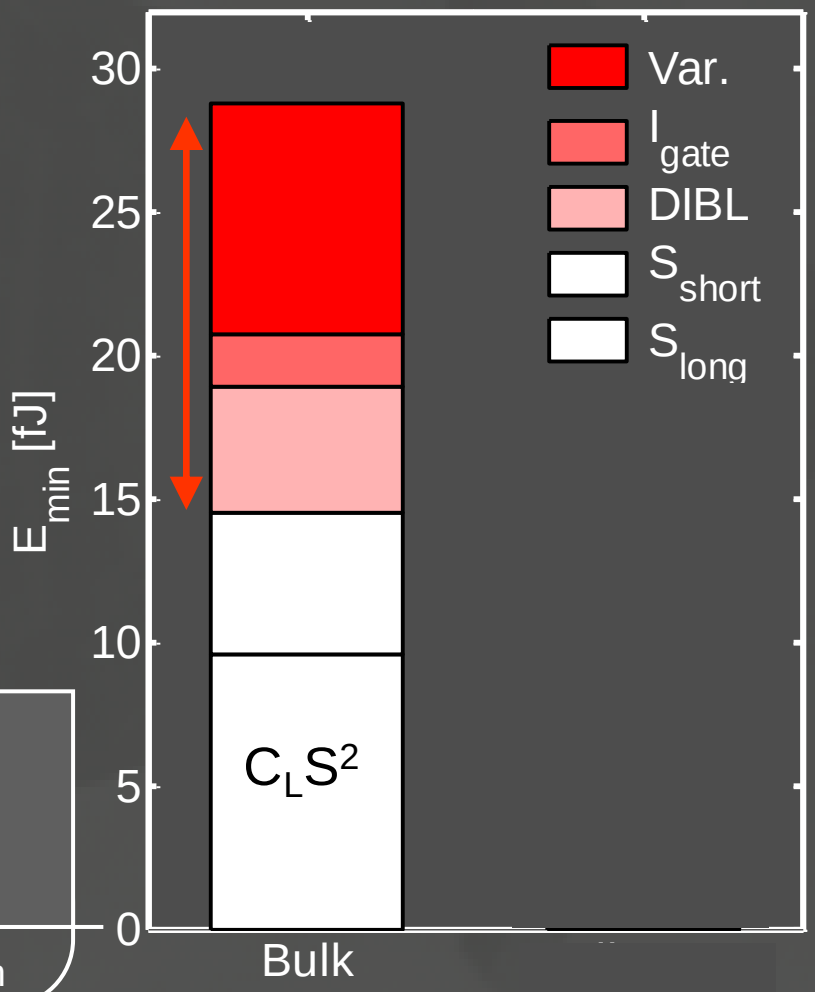
New effects in nanometer technologies



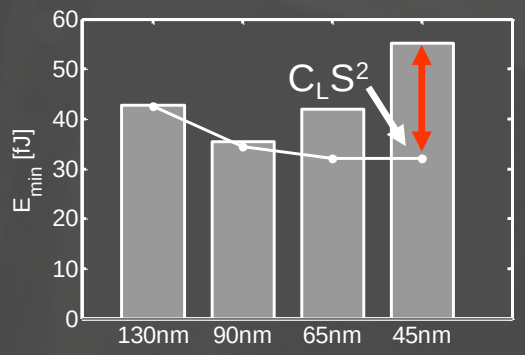
New effects:

- Bad short-channel S
- Drain-induced barrier lowering
- Gate leakage
- Variability





New effects in nanometer technologies



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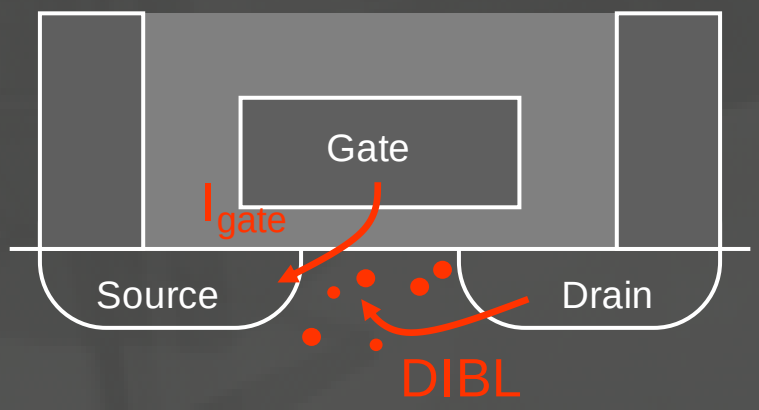
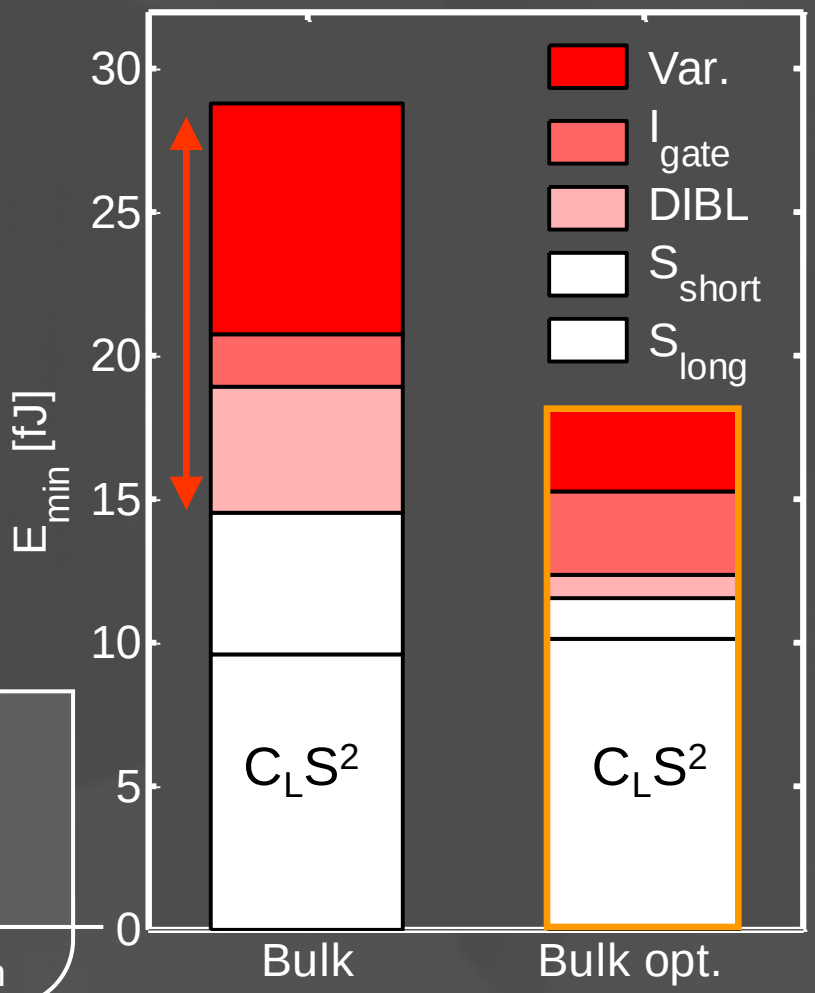
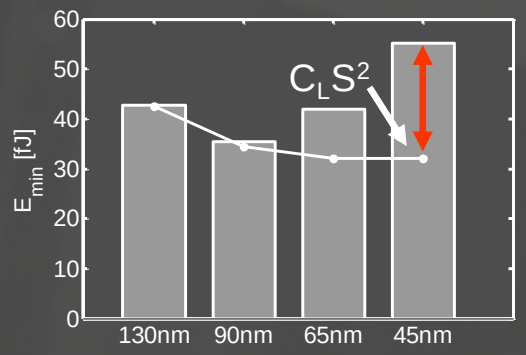


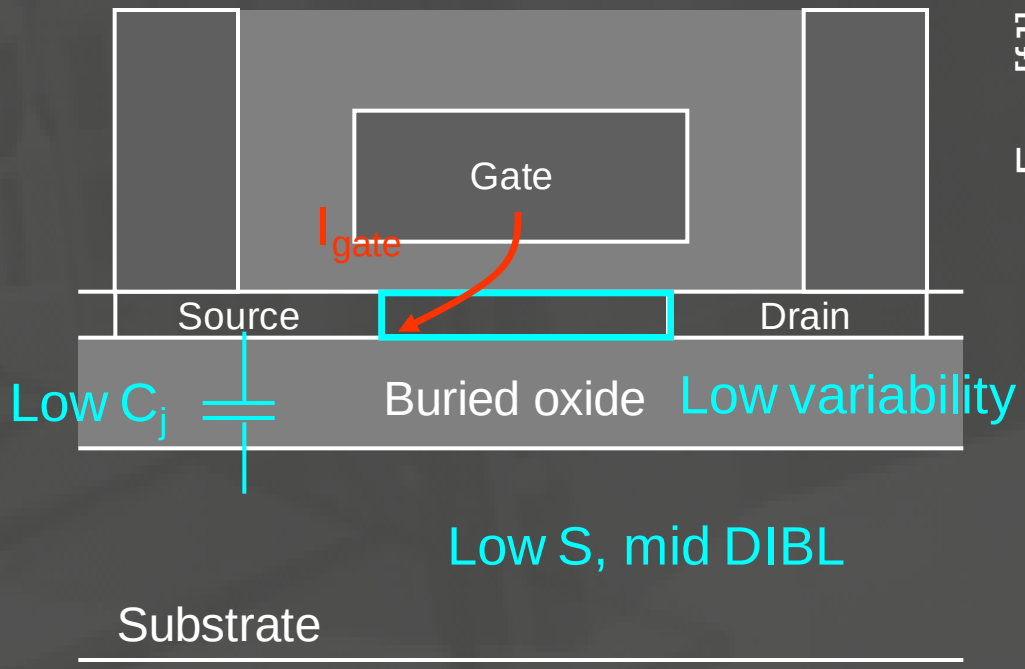


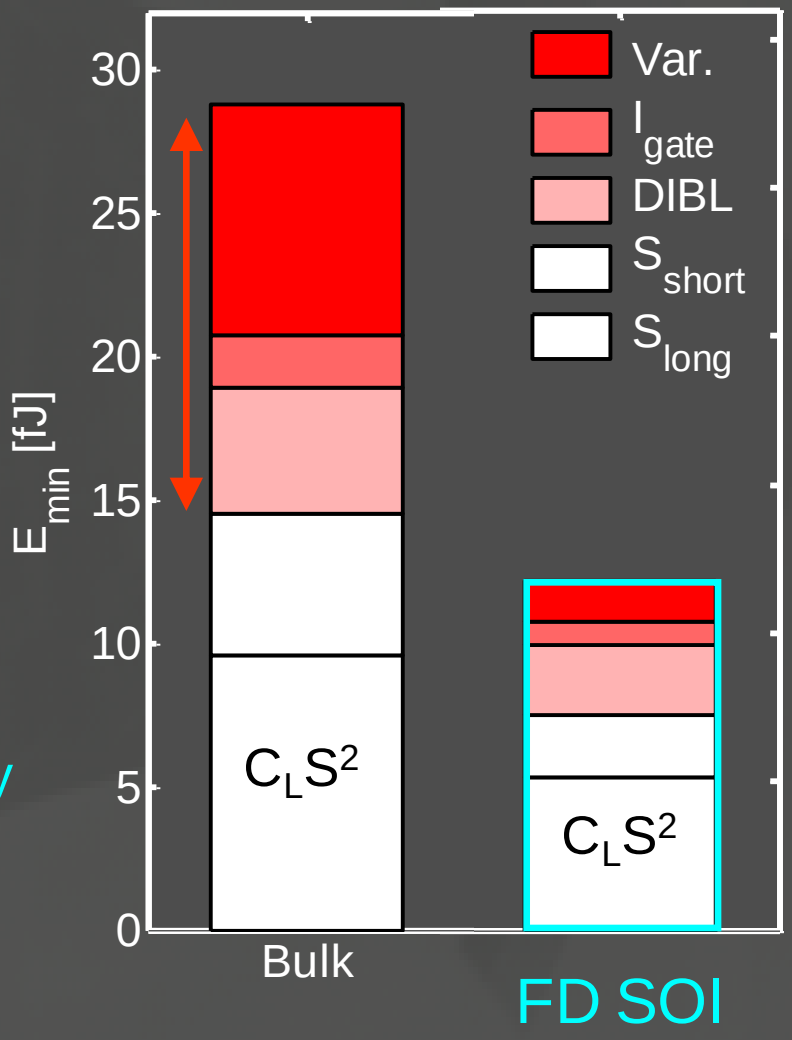
Low V_t + long L_g

Fully-depleted SOI technology

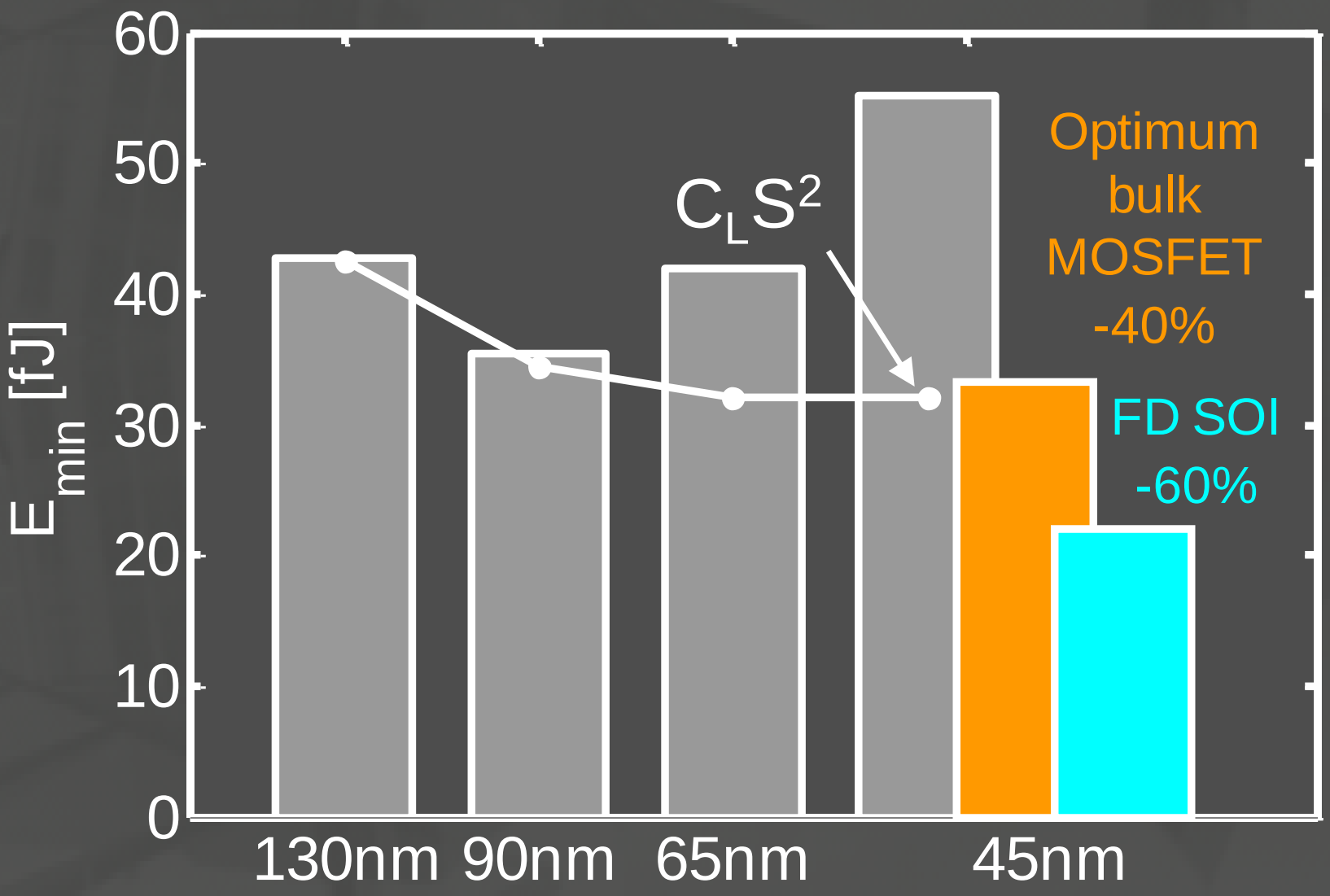


Undoped channel





Evolution of E_{min}



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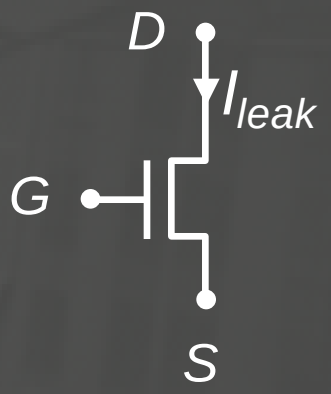
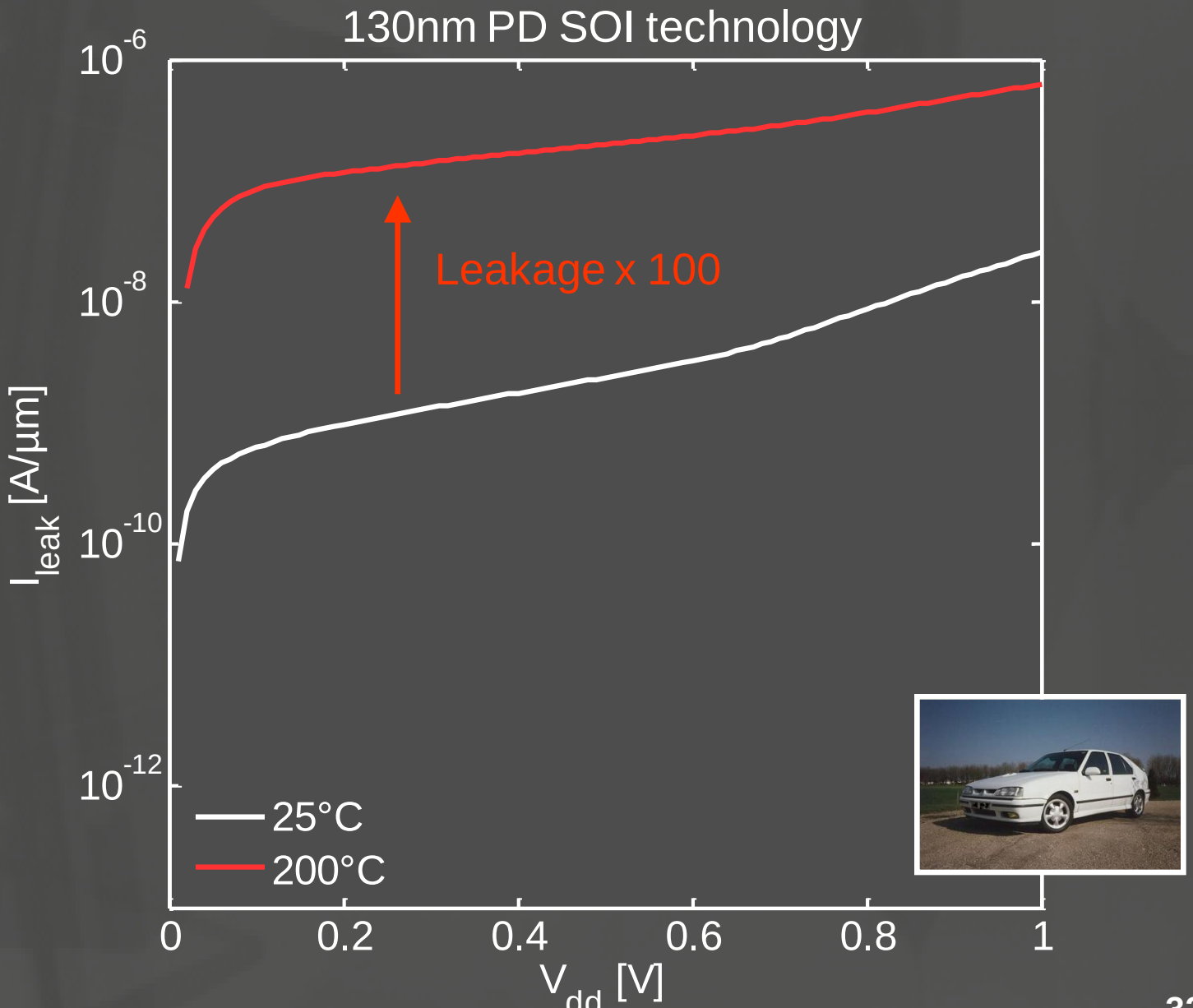
High-temperature operation

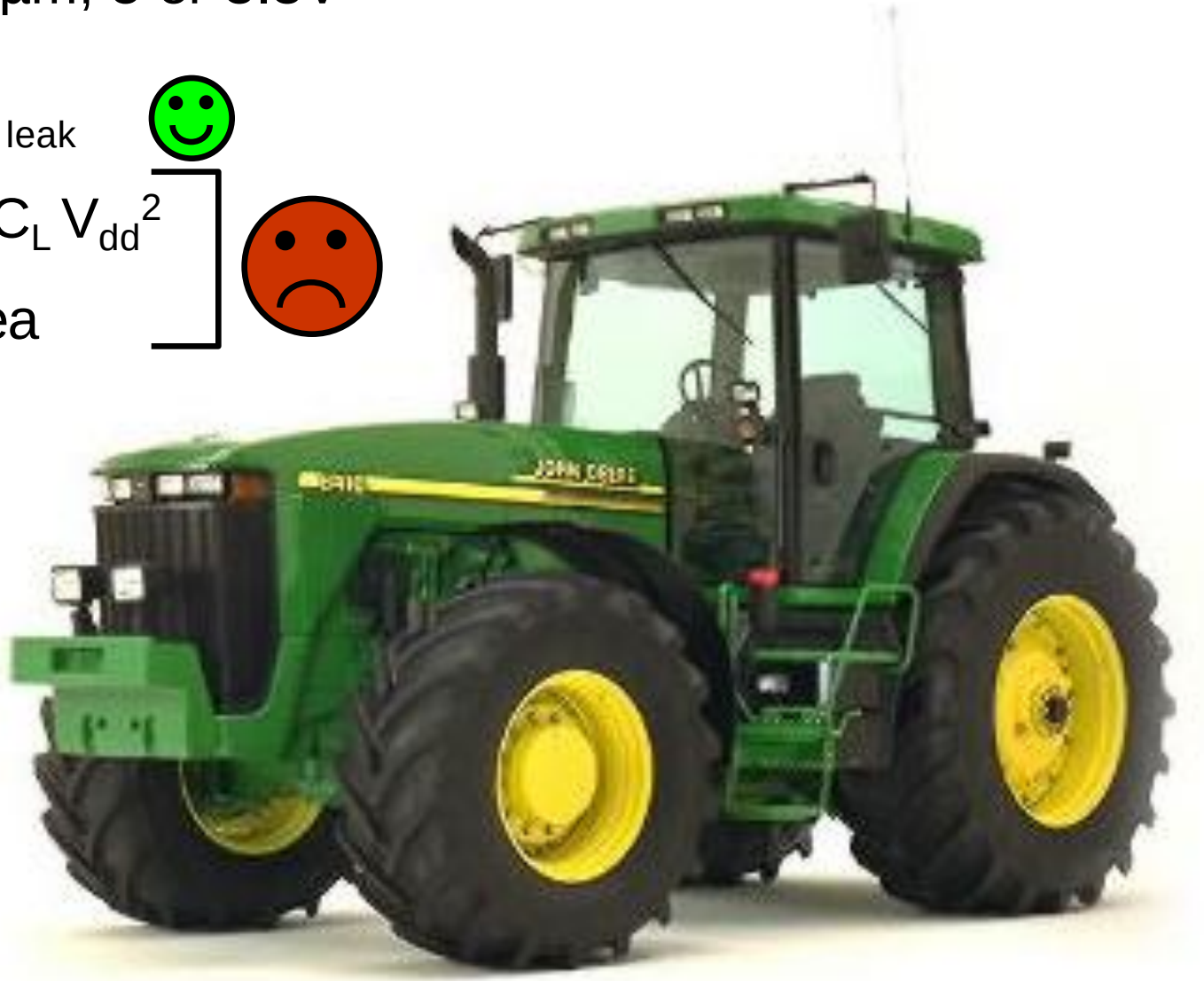




Low-leakage SOI technology

1 or 0.5 µm, 5 or 3.3V

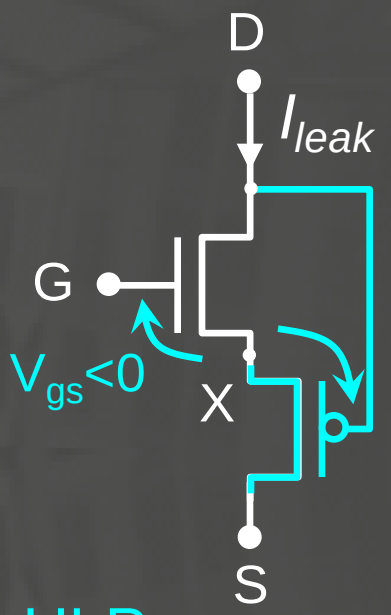
- $E_{stat} \sim I_{leak}$
- $E_{dyn} \sim C_L V_{dd}^2$
- Die area



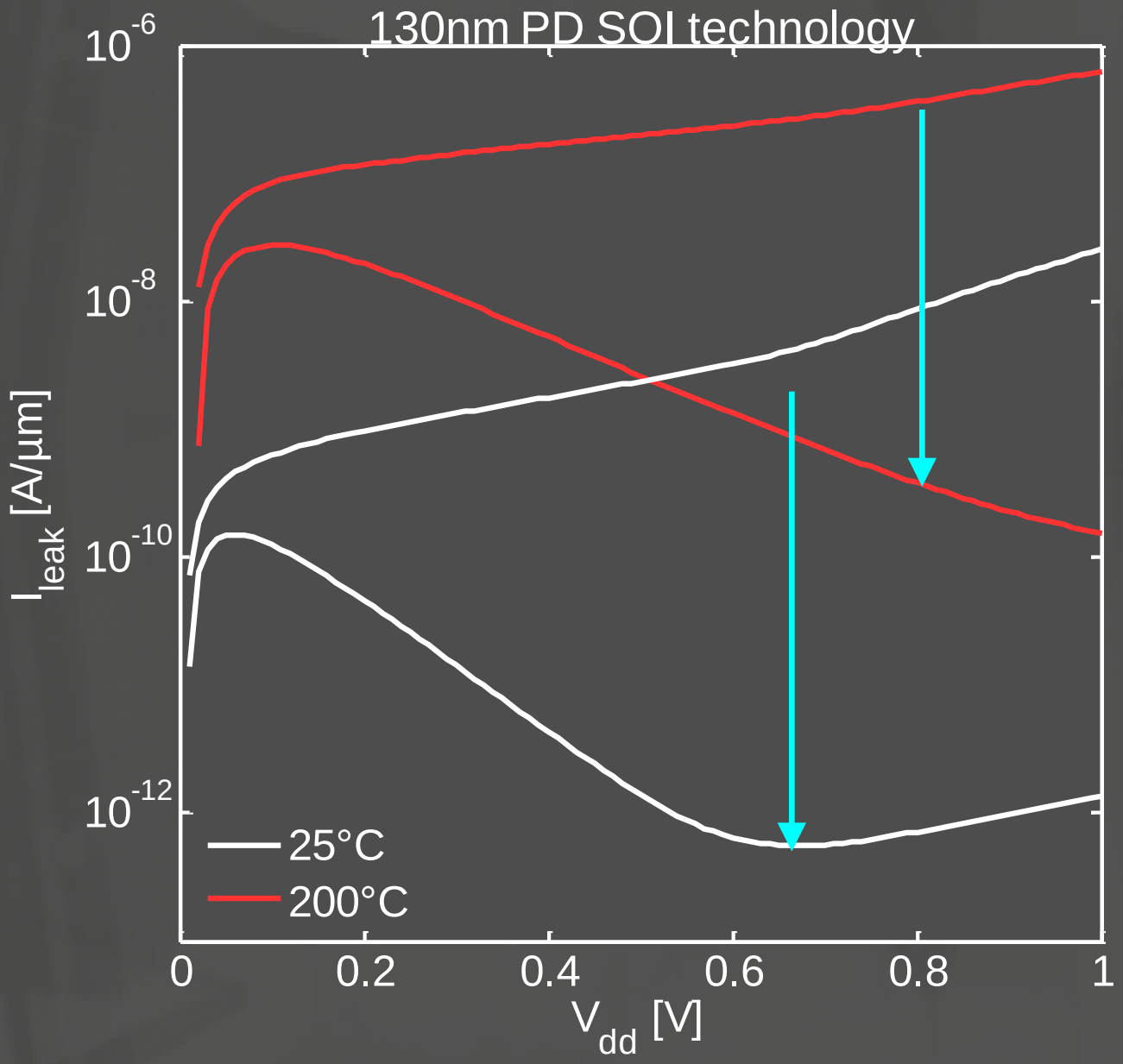
Standard SOI technology

0.13 µm, 1 V

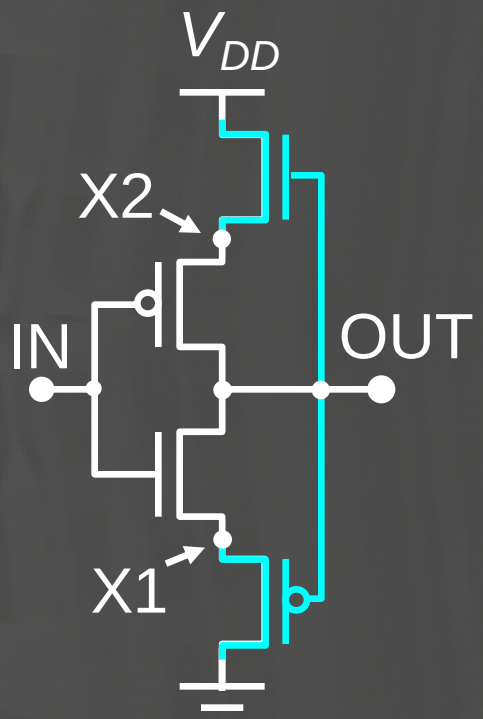
High-temperature operation



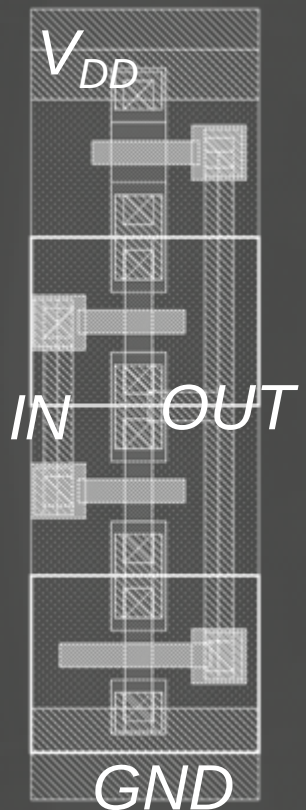
ULP transistor



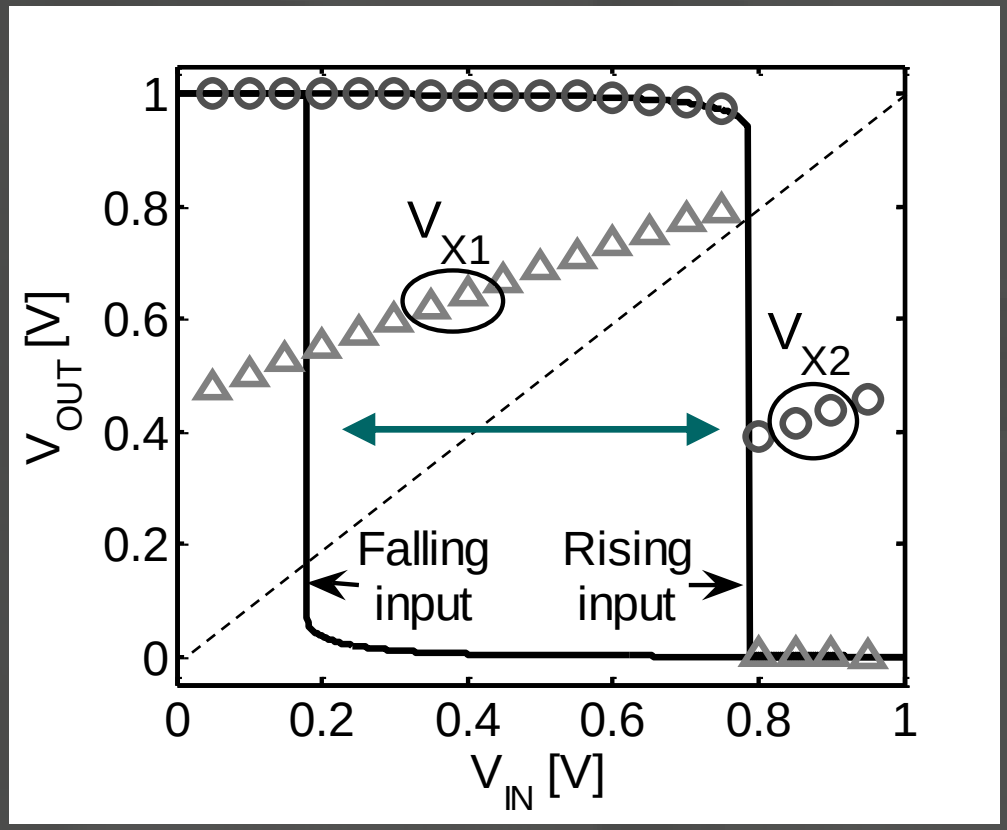
ULP logic style



ULP logic style



Layout in SOI



Hysteresis

ULP logic style

Inverter type	Process $[\mu m]$	Area $[\mu m^2]$	T_{del} $[ns]$	P_{stat} $[nW]$	P_{inst} @ 1 MHz $[nW]$
ULP	0.13	5.4	34.6	0.031	0.81
CMOS	0.13	2.6	0.072	26.8	36.4
CMOS	0.13	2.6	0.31	6.8	8.4
CMOS	1	320	510	0.98	$52.6^{\dagger}$

ULP logic style at 200°C:

- 1000x P_{stat} reduction
- Long delay → max ~ 1 MOp/s

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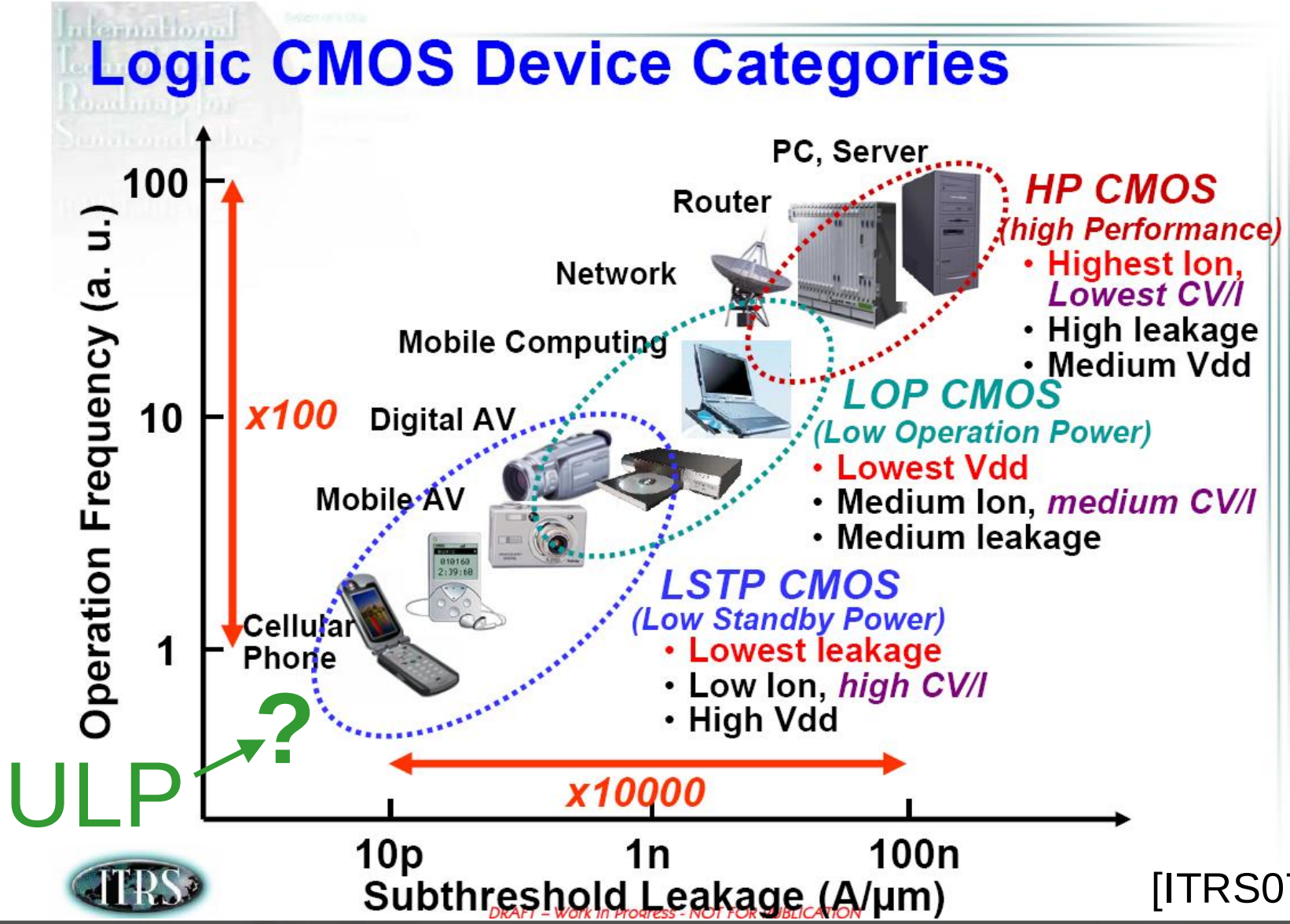
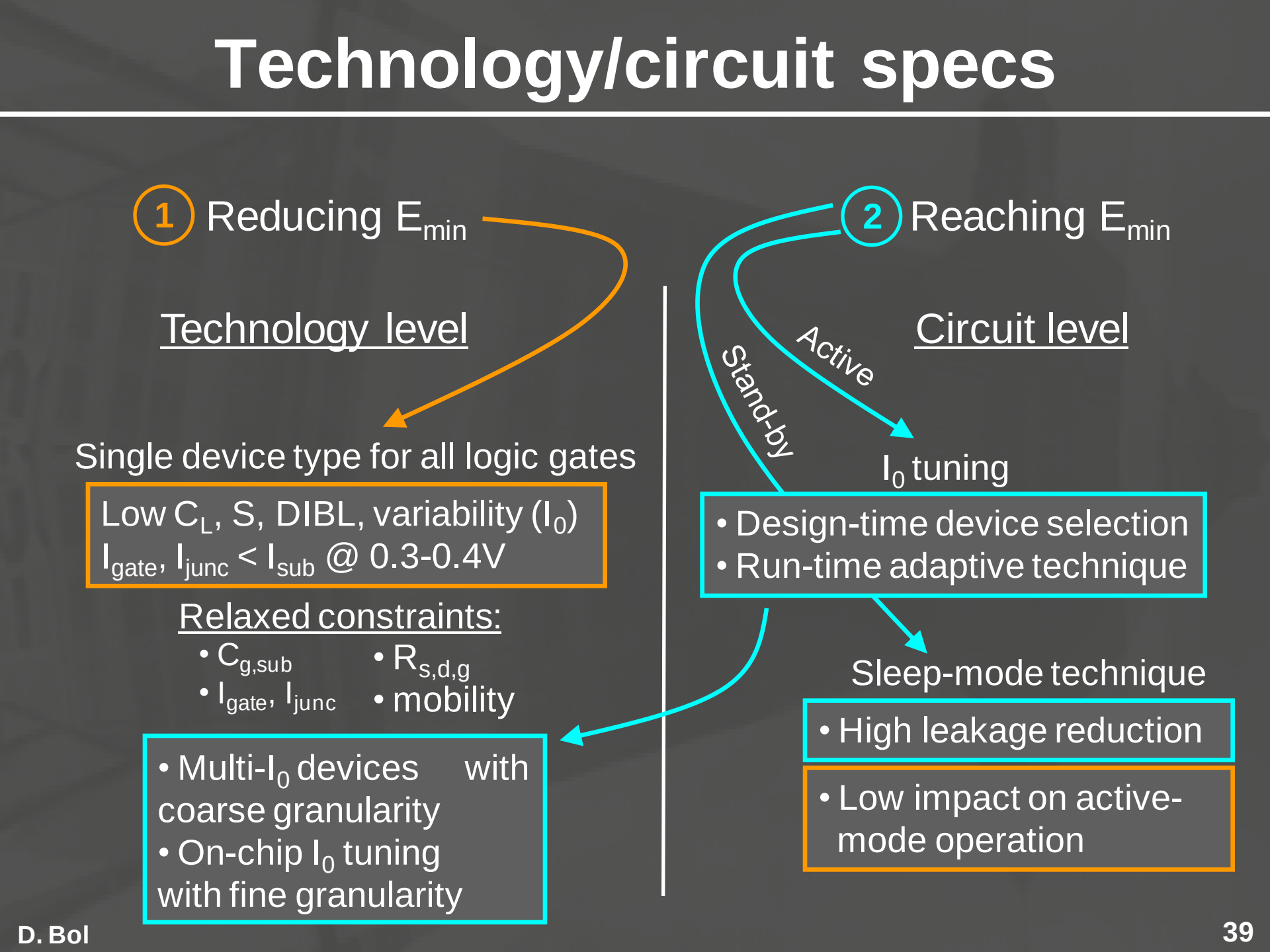
ITRS recommendations

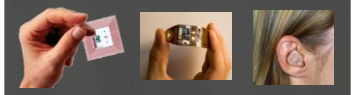


[ITRS07]

Technology/circuit specs



Technology/circuit roadmap

Applications \ Node	130 / 90 nm	65 / 45 nm	32 / 22 nm
High-temperature ULP industrial applications 	ULP logic style • PD SOI • *(FD SOI)* @ GP flavor	Reliability issues	Reliability issues
Standard ULP applications 	Subthreshold logic • Bulk *(+ adapt. RBB)* • *(FD SOI)* @ GP flavor	Subthreshold logic • Bulk + adapt. RBB • FD SOI @ LP flavor	Economical issues
ULP mode in LP applications 	Performance issues	Subthreshold logic • Bulk opt. + adapt. RBB • FD SOI @ HP/GP flavor	Subthreshold logic • FD SOI + UTBOX/DG + adapt. dual-BG bias @ dedicated flavor

Architectural techniques (//, pipe) for meeting throughput constraint

Thank you!

Any questions ?

Acknowledgements:

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Energy consumption