Digital Substrate Noise Reduction by Low-Power Circuit Operation and SOI Technology

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Abstract
Progress of integrated circuit technology allows integration of analog and digital circuits on the same chip. This co-integration yields higher performances and reliability, while reducing power consumption, but also raises new challenges for circuit designers. The substrate noise generated by the switching digital part has detrimental effects on the analog part. In this contribution, a wide-band characterization of the so-called "digital substrate noise" is realized, in bulk and in SOI technology. The impact of low-power circuit operation mode on the digital substrate noise is investigated. A comparison of bulk and SOI technology with regard to the digital substrate noise level is also realized.

1. INTRODUCTION

In recent years, rapid progress of integrated circuit technology has enabled the co-integration of analog front-end and digital baseband processing circuits of communication systems onto the same chip. Such mixed-signal Systems-on-Chip (SoCs) allow more functionality, higher performance, lower power and higher reliability than non-integrated solutions, where at least two chips are needed, one for digital and one for the analog part. Moreover, thanks to CMOS technology scaling and its associated increasing integration level, SoCs have become the way to achieve cost effectiveness for demanding applications such as home entertainment and graphics, mobile consumer devices, networking and storage equipment.

Such a rising integration level of mixed-signal integrated circuits (ICs) raises new issues for circuit designers. One of these issues is the substrate noise generated by switching digital circuits, called Digital Substrate Noise (DSN), which may degrade the behaviour of close analog circuits [1]. DSN issues become more and more important with IC evolution as:

- digital parts get more noisy due to increasing complexity and clock frequencies ;
- digital and analog parts get closer ;
- analog parts get more sensitive because of V_{dd} scaling for power concern issues.

In general, regardless of the impact of DSN on the victim, substrate noise can be decomposed in three different mechanisms: noise generation, injection into the substrate and propagation [2]. Improvement in the reduction of any of these three mechanisms, or in all of them, will lead to a reduction of the DSN and in a relaxation of the design requirements. Typically, guard rings and overdesigned structures are adopted to limit the effect of substrate noise, thereby reducing the advantages of the introduction of new technologies. It is thus a major issue for the semiconductor industry to find area-efficient design/technology solutions to reduce the impact of substrate noise in mixed-signal ICs.

In this work, we experimentally study two directions for reducing DSN in low-voltage mixed-signal SoCs: low-power operation and Silicon-on-Insulator (SOI) technology. Indeed, SOI CMOS has already proved its better performance over bulk CMOS technology in terms of gain, better scalability, isolation and crosstalk [3]. Furthermore, SOI can be also combined with high-resistivity substrates (HR-SOI) in order to attain less losses and better RF performances. However, to the authors' knowledge, no comparison in terms of digital substrate noise has been made between SOI and bulk CMOS technologies, or at least between comparable CMOS technologies and dimensions. We thus compare experimental DSN characterizations of CMOS circuits lying on SOI and bulk substrates.

This contribution is organized as follows. In Section 2, the main mechanisms of DSN are briefly presented. We then introduce the experimental setup in Section 3. Reduction of DSN by low-power operation in bulk technology is adressed in Section 4 and the reduction of DSN by migration to SOI technology is finally presented in Section 5.

2. DIGITAL SUBSTRATE NOISE MECHANISMS

Three mechanisms must be taken into account while studying DSN: the noise generation, the injection and propagation through the substrate. The performance degradation on the victim circuit is beyond the scope of this contribution

There are two main sources generating DSN [4], which are the same for bulk and SOI technology. The first source is the switching activity of the source and drain of the transistors. The second source of DSN is noise coupling from the supply rails to the substrate. This noise is due to parasitic inductances and resistors in the supply circuit and bondwires, coupled to the current spikes generated by switching gates. Inductances in power-supply lines coupled with the capacitance between ground and power can also create ringing on supply lines, which couples to the substrate.

While studying the injection and propagation mechanisms, differences must be made between bulk and SOI technology. In SOI, both noise sources are coupled capacitively to the HR-Si substrate through the buried oxide, whereas in bulk the drain switching current is more effectively injected into the substrate through source/drain junctions. This difference in injection mechanisms can be seen in Figure 1. The noise propagates then through the substrate, which can be modeled by resistors for the bulk substrate or by capacitor-resistor lumped element model for HR-Si substrate [2][3].

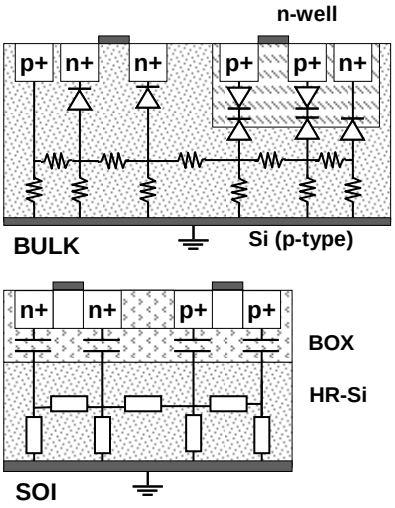

Fig. 1. Digital noise generation and injection in bulk (top) and SOI (bottom) technologies

3. EXPERIMENTAL SETUP

Two circuits have been fabricated to characterize DSN. The first one is fabricated using the 0.13µm bulk technology while the second uses the 0.13µm SOI technology, both from STMicroelectronics. This is the only difference between these two circuits, and the layout of the circuit has been reported directly from one technology to the other.

The circuit is compound of a digital part generating DSN and a tap to probe DSN, as shown in Figure 2. The digital part is composed of inverter trees. Some control signals permit to choose how many inverter trees actually switch. The probing system is compound of a 200x150 µm N+-doped active zone located 1100 µm away from the inverter trees and connected to a coplanar RF pad.

The input signal of the inverter trees is a clock signal generated by an external pulse generator, injected through an RF pad. The supply current is measured using the DC voltage source. The spectral content of the noise is measured using a wide-band spectrum analyzer. All connections cables are the same for bulk and SOI circuit measurements.

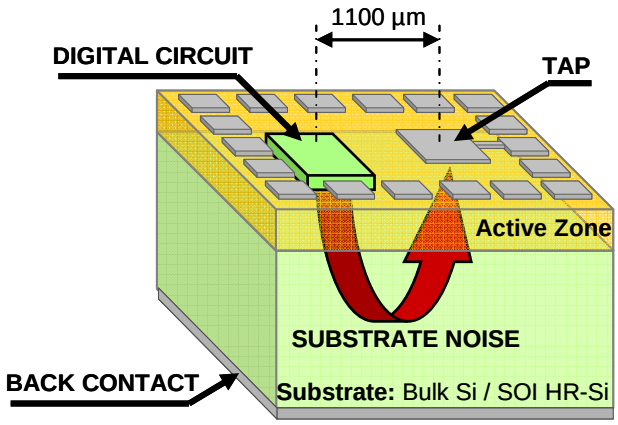

Fig. 2. On-chip experimental setup

Figure 3 shows results of a measurement for the bulk circuit, using an input clock frequency of 225 MHz, a power supply of 1.2V and with 8 inverter trees switching. In the remainder of this contribution, we mainly use frequency envelope of the noise to present results, as it allows easier comparison between several noise levels.

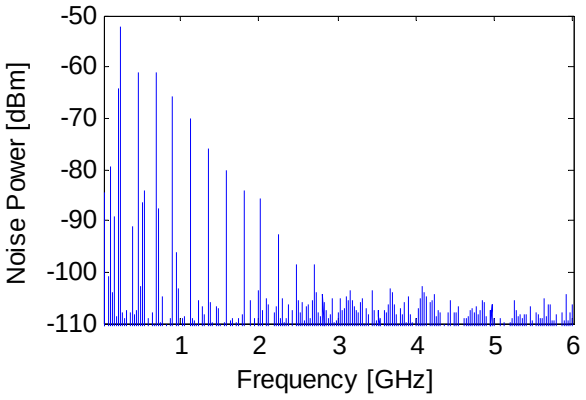

Fig. 3. Frequency spectrum of the measured DSN in bulk Si (clock frequency = 225MHz, V_{dd} = 1.2V, 8 inverter trees)

4. DSN REDUCTION IN BULK TECHNOLOGY

In this section, we investigate the impact of power consumption reduction on DSN, using measurement results for the bulk circuit. We focus on dynamic consumption reduction techniques often used in digital design: frequency, supply voltage and activity factor reduction [5].

4.1. DSN vs. clock frequency

Figure 4 shows DSN level for 8 switching inverter trees, at 1.2V and for different input frequencies. Figure 4.a shows absolute noise level in dBm. Results show that reducing the input signal frequency, and thus the dynamic power consumption, by a factor of 3 allows a reduction greater than 10 dBm in the noise level. Moreover, the envelope of the

frequency response seems independent of the clock input frequency.

Figure 4.b presents normalized DSN measurement with regard to the total power consumption of the digital circuit, for the same circuit configuration. This graph shows closer envelope curves, although the fitting between the curves is not perfect. One can thus conclude that there is a relation between power consumption and DSN, and that this relation is close from a linear one [4].

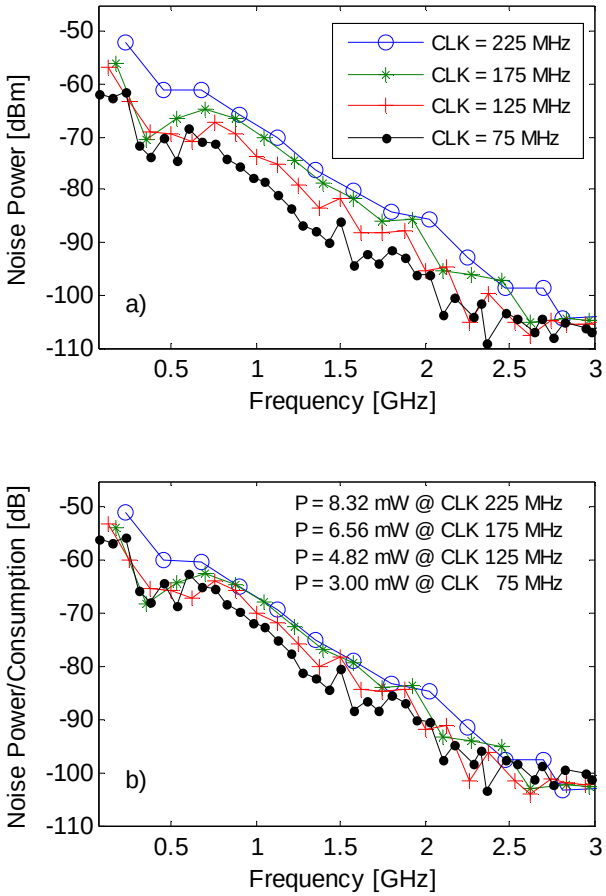

Fig. 4. Frequency envelope of measured DSN vs. CLK frequency: (a) absolute and (b) normalized to power consumption (V_{dd} = 1.2 V, 8 inverter trees, bulk Si)

4.2. DSN vs. voltage supply

Figure 5 shows DSN level for 8 switching inverter trees, with an input signal clock frequency of 225 MHz and several supply voltages. Figure 5.a shows absolute noise level in dBm. Results show that reducing the supply voltage from 1.4V to 0.8V allows a noise level reduction from 10 to 30 dBm, depending on the noise frequency.

Second graph in Figure 5 presents DSN measurements with the same circuit configuration, while noise power is normalized with regard to the total consumption of the digital circuit. The noise level for the different supply voltages is close for the first harmonic, which seems to confirm that the noise level is proportional to the injected supply power. At higher frequencies however, an increasing discrepancy can be shown between the different curves. This discrepancy could arise from steeper signal edges for switching inverter while using higher supply voltage. These steeper edges would in turn create more DSN at higher frequencies, compared with soft edges of inverter trees working at lower supply voltage.

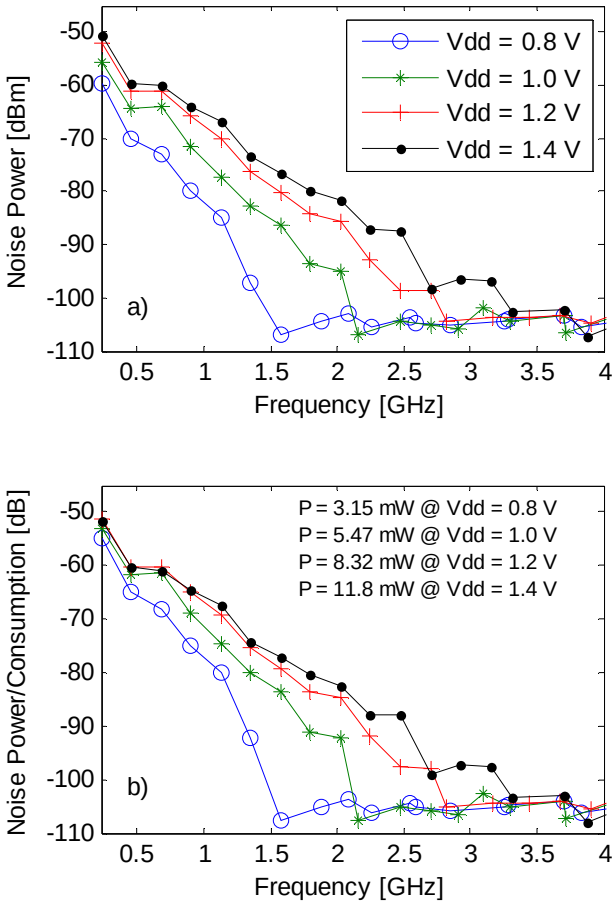

Fig. 5. Frequency envelope of measured DSN vs. V_{dd}: (a) absolute and (b) normalized to power consumption (CLK frequency = 225 MHz, 8 inverter trees, bulk Si)

4.3. DSN vs. activity factor

Figure 6 shows DSN level for a supply voltage of 1.2V and an input signal clock frequency of 225 MHz, while the number of inverter trees switching goes from 1 to 16. It allows us to simulate the impact on DSN of using activity factor reduction technique, like clock or data gating. Figure 6.a shows absolute noise level in dBm. Results show that reducing the activity factor by a factor of 16 allows a DSN level reduction of almost 20 dBm.

Figure 6.b presents DSN measurements with the same circuit configuration, while noise power is normalized with regard to the total consumption of the digital circuit. As for the DSN vs. clock frequency analysis, normalized curves are closer than the ones for absolute DSN level. The re-

maining difference between the curves could be explained here by an higher injection surface of the source/drain switching noise when more inverter trees are switching.

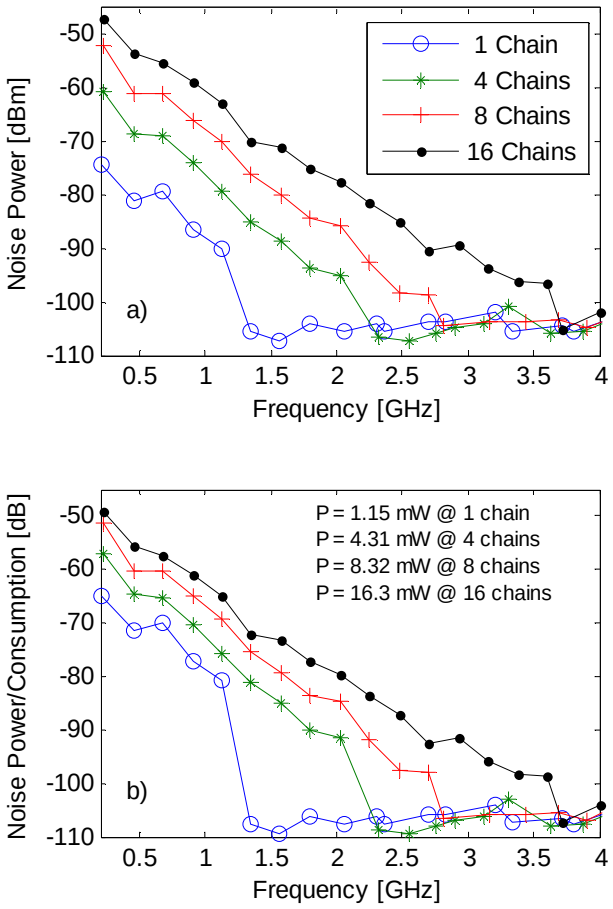

Fig. 6. Frequency envelope of measured DSN vs. number of inverter trees: (a) absolute and (b) normalized to power consumption (CLK frequency = 225 MHz, V_{dd} = 1.2 V, bulk Si)

5. DSN REDUCTION BY USING SOI TECHNOLOGY

As explained in Section 2, DSN injection and propagation mechanisms are different in bulk and SOI technology. In this section, we investigate the impact on DSN of using SOI technology rather than bulk. We first focus on the noise injected by the external environment through the backside contact, then on the noise generated by switching of digital I/O pads, and finally on the noise produced by the switching digital circuit

5.1. Substrate backside injected noise reduction

In this paragraph we study the impact of using SOI technology on the noise injected in the circuit by the backside contact. It is due to noise on the DC supply voltage, which is contacted to the backside of the chip. Three measurements are made to characterize the backside noise. In Figure 7.a, the measured substrate noise when the RF output probe is not placed on the circuit pad is shown. This characterizes the noise picked up by the probe wire and the spectrum analyzer itself. Figure 7.b and c show measured substrate noise when the RF output probe is placed on the pad for bulk and SOI circuit respectively. Only the backside contact is contacted to the chuck of the prober. The input clock signal and the supply sources are disconnected. The increase in the noise level between these two kinds of measurement can thus only come from parasitic environmental noise, picked up by the chuck and injected through the backside contact. While in SOI technology the noise level is the same for measure with or without RF output probe contact, the bulk measurement shows an increase in noise level. SOI seems thus to be more robust against undesired backside injected noise.

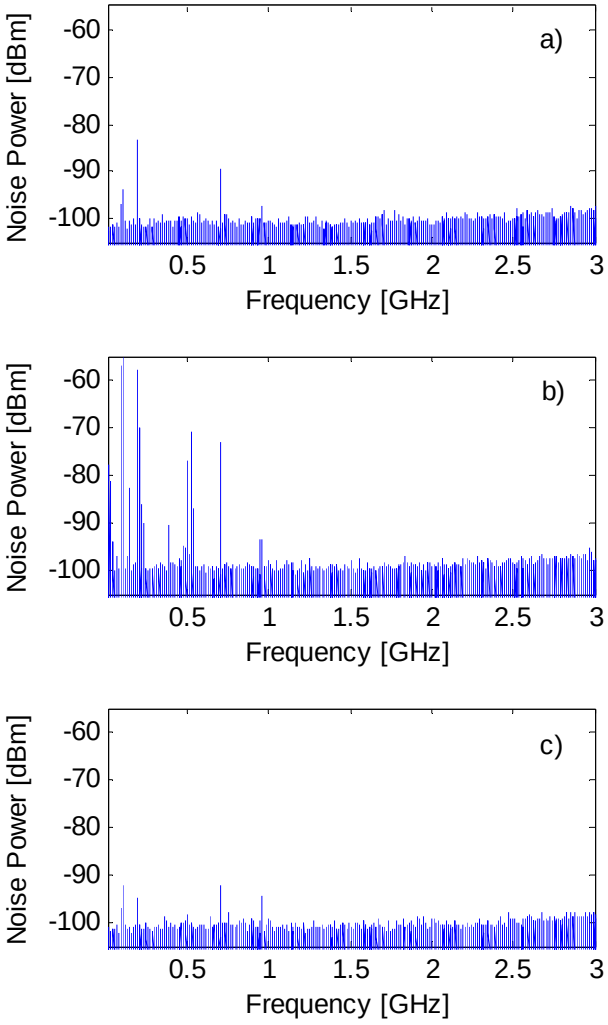

Fig. 7. Frequency spectrum of measurement noise-floor: (a) no probe contact, probe contact (b) to bulk Si circuit and (c) to SOI circuit

5.2. I/O pad injected noise reduction

To focus on the noise injected by a switching I/O pad, we inject a 225 MHz input clock signal on the RF input pad of the circuit, keeping the supply sources disconnected. Results are shown in Figure 8. For the SOI circuit, the noise level stays the same than in Figure 7.c. The switching input pad injects thus no noise through the substrate to the analog victim. On the other hand, measurement of the bulk circuit shows the appearance of noise at 225, 675 and 1125 MHz, which are the frequencies of the odd harmonics of the input signal. The robustness of the SOI regarding the I/O pad injected noise is of practical interest, because digital circuit can have several digital pads switching at the same time.

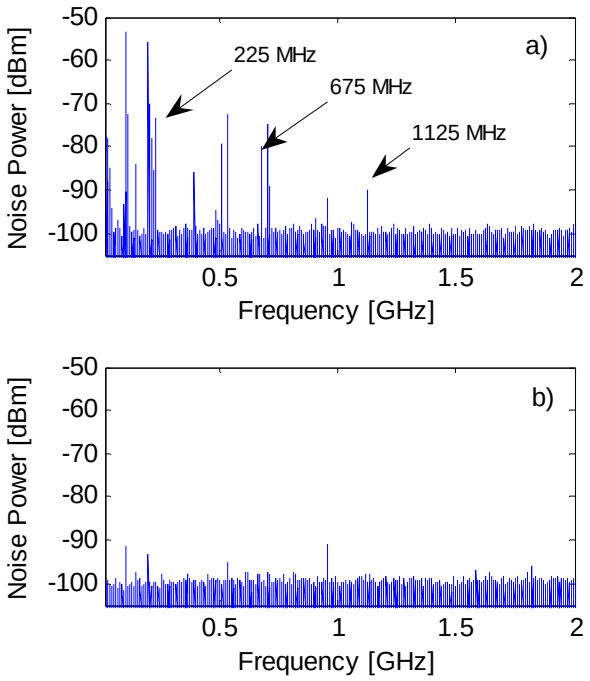

Fig. 8. Frequency spectrum of the measured substrate noise from the switching clock input pad (a) in bulk Si and (b) SOI at (CLK frequency = 225 MHz)

5.3. DSN reduction

In this paragraph, we study the impact of using SOI technology on the noise generated by the digital circuit. Figure 9 shows the DSN measurement for the SOI circuit, with 8 switching inverter trees, a supply voltage of 1.2 V and an input clock frequency of 225 MHz. Similarly to the bulk results from section 4.1, the DSN frequency response is not dependent on the clock frequency. However, DSN presents a quite different frequency response in SOI than in bulk. At low frequency, SOI and bulk have the same kind of response, with the SOI DSN level decreasing faster with increasing frequency. At higher frequency, the SOI DSN presents a kind of pass-band filter shape, which is not present for the bulk circuit. We have shown in our previous work that this second part of the frequency response is due to ringing on supply rail, due to parasitic capacitances and inductances on the supply rails [6].

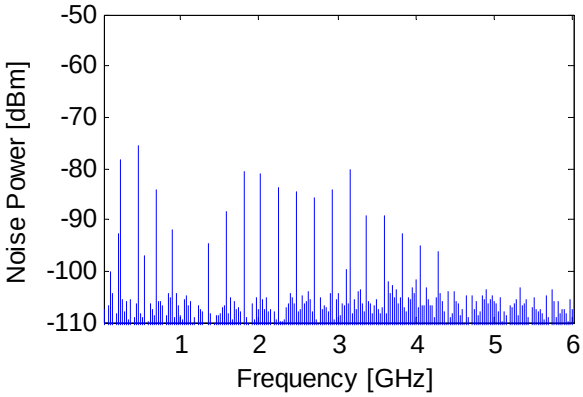

Fig. 9. Frequency spectrum of the measured DSN in SOI (clock frequency = 225MHz, V_{dd} = 1.2V, 8 inverter trees)

Figure 10 shows comparison of bulk and SOI measurements, for two different supply voltages. For the 1.2V supply voltage, up to 1 GHz the SOI technology allows an important reduction of DSN. At higher frequency, the noise due to ringing on supply rail becomes dominant, and the bulk circuit shows a lower DSN level. This conclusion is in agreement with results of studies on the supply noise showing that special attention should be paid to supply rail for SOI technology, due to lower intrinsic decoupling capacitances [7]. At lower power supply (0.8V), as for the bulk, high frequency noise generation decrease. The ringing supply noise tends thus to be negligible. The SOI technology presents then better DSN results than bulk for frequency up to 2 GHz, and similar DSN level for upper frequency.

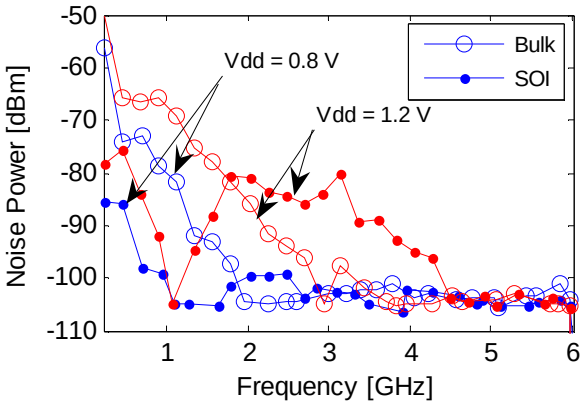

Fig. 10. Comparison of the frequency envelope of measured DSN (clock frequency = 225 MHz, 8 inverter trees)

Finally, Figure 11 shows power consumption of the two circuits for two supply voltages and several input frequencies. As expected, one can establish a linear relation between input frequency and power consumption. This figure also shows that power consumption values are quiet similar

for the two circuits, the SOI one consuming slightly less than the bulk one. This is a confirmation that the difference between DSN in these two technologies is due to difference in DSN mechanisms, and not to a difference in consumption.

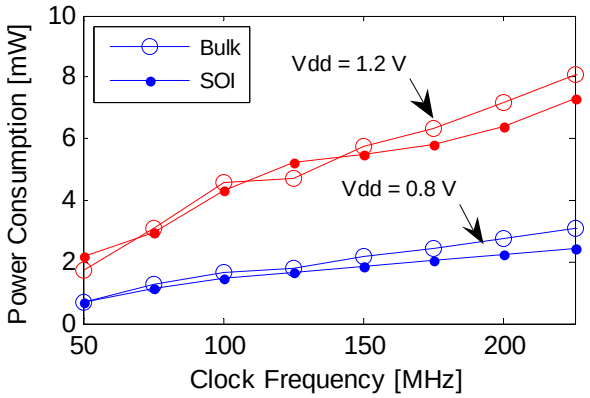

Fig. 11. Comparison of the power consumption vs. clock frequency

6. CONCLUSION

In this contribution, a wide-band characterization of the digital substrate noise in bulk and in SOI technology is realized. The impact of using low-power operating mode is studied, showing that reducing the dynamic consumption of the digital part of a circuit allows reducing DSN. A comparison between bulk and SOI technology is also realized, showing better robustness of SOI against the backside contact injected noise and the noise injected by switching digital I/O pads. Regarding to the DSN, a special attention should be paid to the supply circuit when using SOI technology. It is also shown that SOI in combination with low-power circuit operation achieves the lowest DSN level for a given circuit.

ACKNOWLEDGMENTS

This work has been partially funded by The Institute for the Promotion of Innovation by Science and Technology in Flanders (IWT-Flanders) - project SBO no: 040114 - and by the European Commission FP6 Framework Programme through the Integrated Project PULLNANO. D. Bol and D. Flandre are research fellow and honorary senior research associate of the Fonds National de la Recherche Scientifique, respectively. R. Ambroise is with UCL thanks to a grant from the Fonds pour la formation à la Recherche dans l'Industrie et l'Agriculture. Authors would like to thanks Pascal Simon for his support with measurement setup, and STMicroelectronics for the fabrication of the SOI circuit.

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