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Ultra-Low-Voltage Design of Nanometer CMOS Circuits for Low-Power Heterogeneous Embedded Systems

FETCH 2010

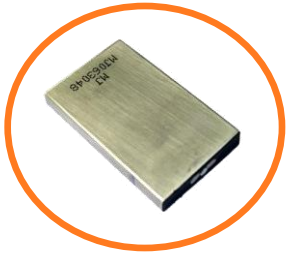
David Bol

Microelectronics Laboratory

January 12th, 2010

Heterogeneous embedded systems

- Heterogeneous embedded systems integrate:
  - Logic (custom + microprocessors)
  - Memories (eSRAM/eDRAM/Flash)
  - Analog (PLL, regulators, ADC/DAC, sensors)
  - RF (mixers, LNA, PA)
- Common constraint → low power



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Ultra-low-voltage operation

- Low-voltage V_{dd}=0.6-1.5V

  MOSFETs in strong inversion (superthreshold)

- **Ultra-low-voltage $V_{dd} \leq 0.5V$**

  MOSFETs in weak/moderate inversion

  = sub-/near-threshold

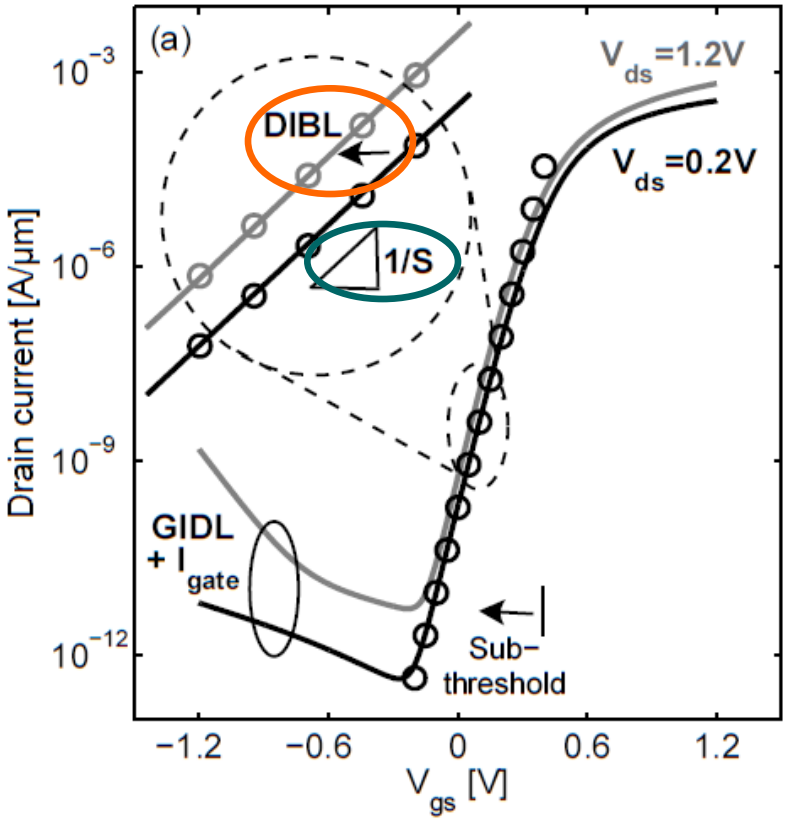
- Interests of ultra-low-voltage operation:
  - Logic: reduces Energy per operation (E_{op})
  - Memories: reduces leakage power (P_{leak})
  - Analog: improved behavior

Subthreshold operation

$$I_{sub} = I_0 \times 10^{\frac{V_{gs} + \eta V_{ds}}{S}} \times \left(1 - e^{\frac{-V_{ds}}{U_{th}}}\right)$$

3 technological parameters:

- I_0 reference current
  ~ $\mu \times W/L_{eff} \times e^{(-Vt+-\sigma)/S}$
- S subthreshold swing [mV/dec]
- η DIBL factor [mV/V]

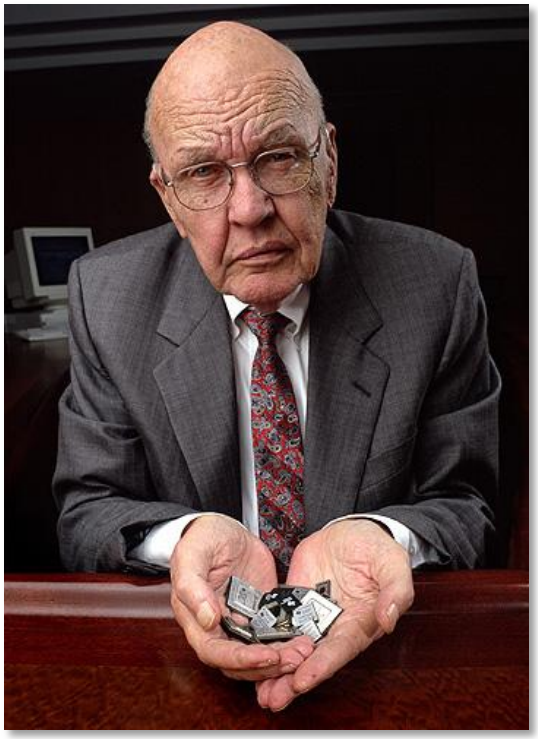


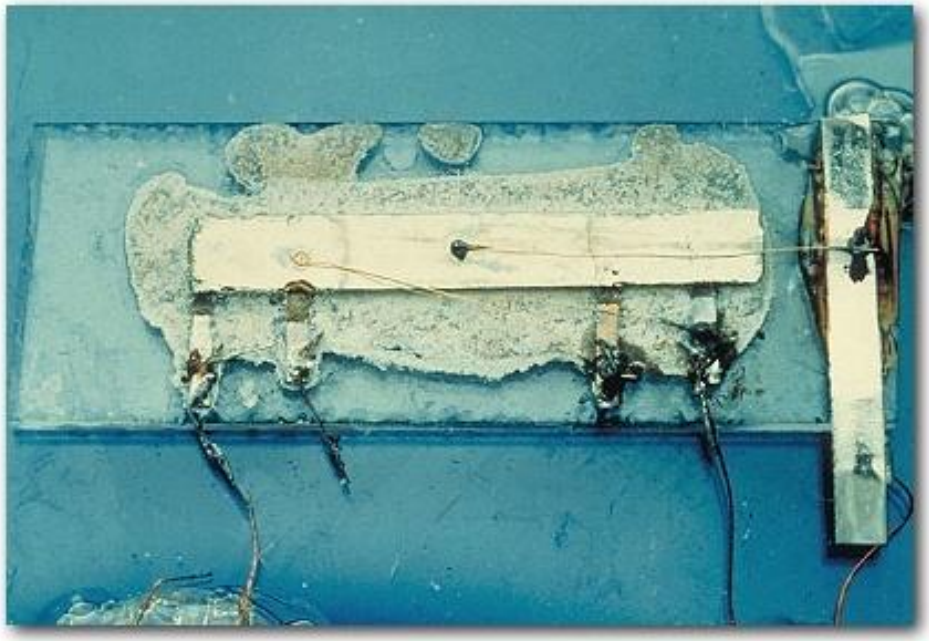
Outline

- Motivation
- **Background: CMOS technology scaling**
- Ultra-low-voltage logic
- Ultra-low-voltage SRAM
- Low-voltage co-integration with analog/RF

The start of microelectronics

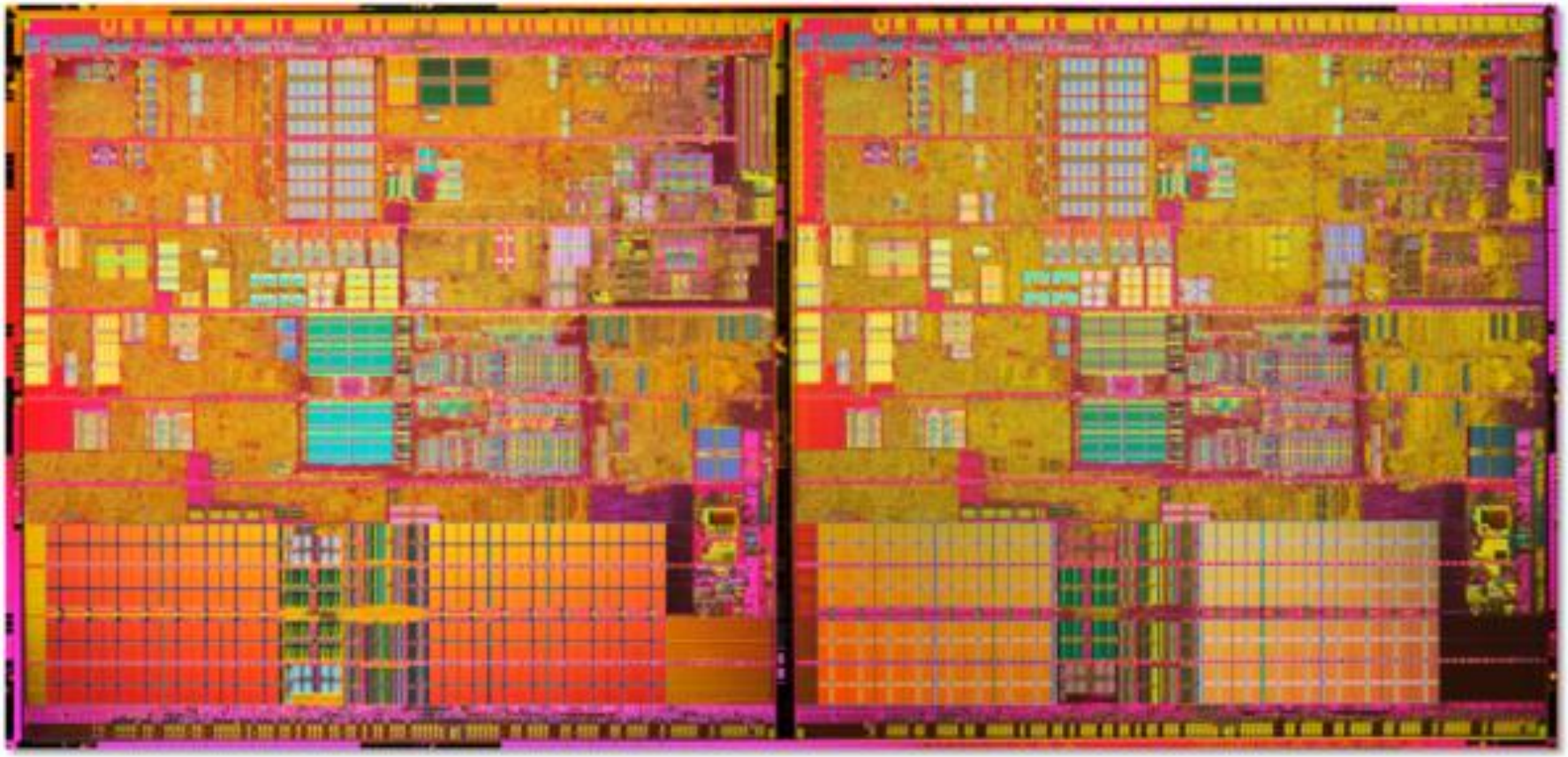
1958: Jack Kilby (Texas Instruments)
invents the integrated circuit





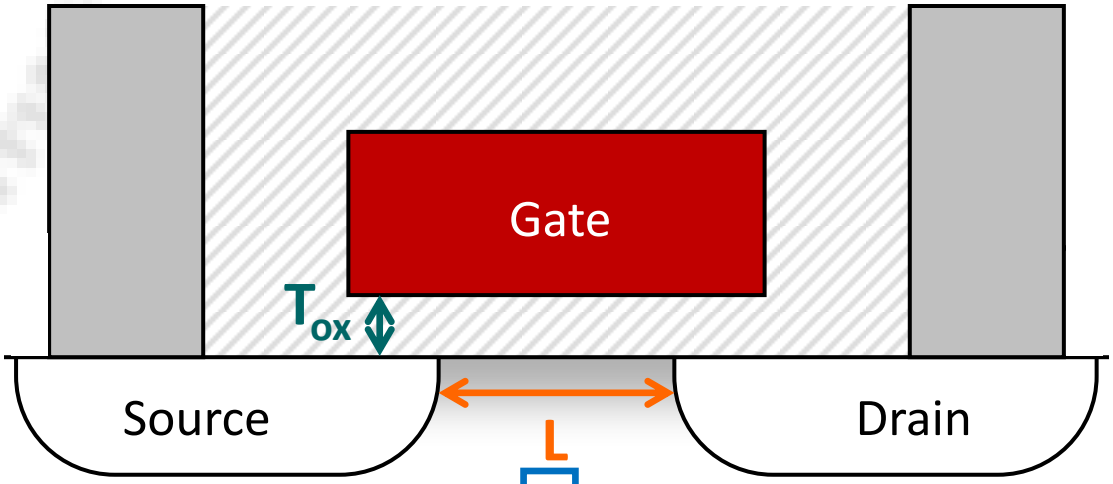
Oscillator prototype
(1 transistor + resistances + capacitors)

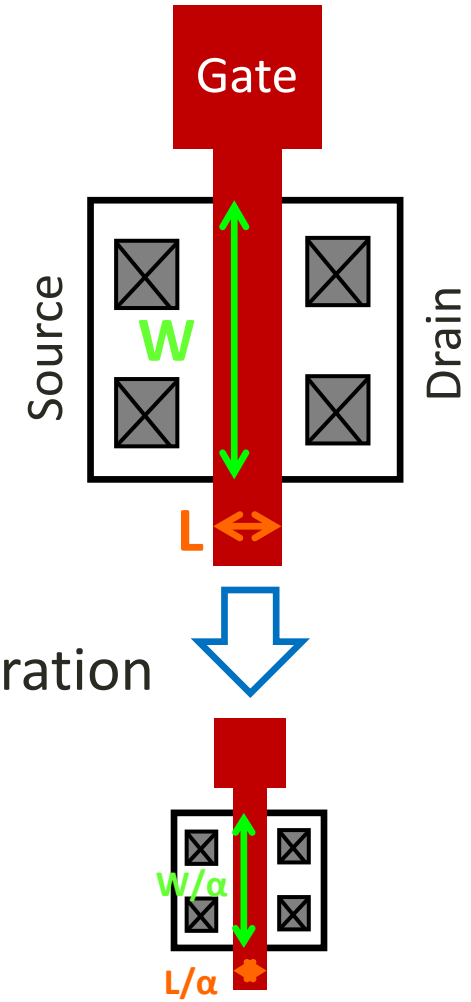
Today's nanoelectronics



Multi-core processor
> 1 billion transistors

CMOS technology scaling





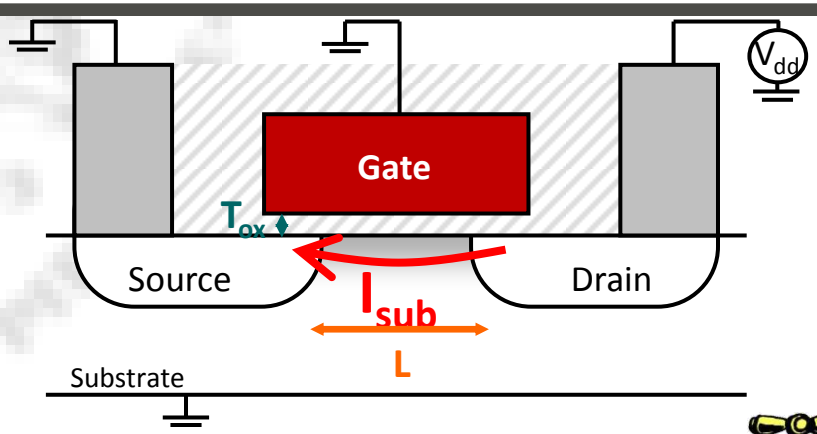
α = √2 / generation

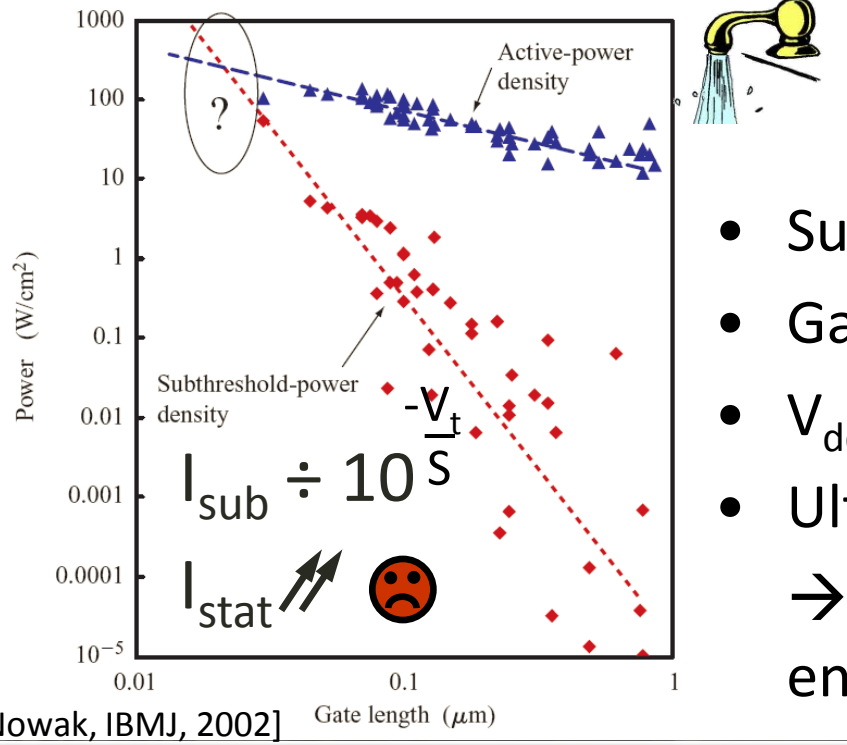
All physical dimensions T_{ox}, L, W ~ 1/α

All voltages V_{dd}, V_t ~ 1/α (constant-field scaling)

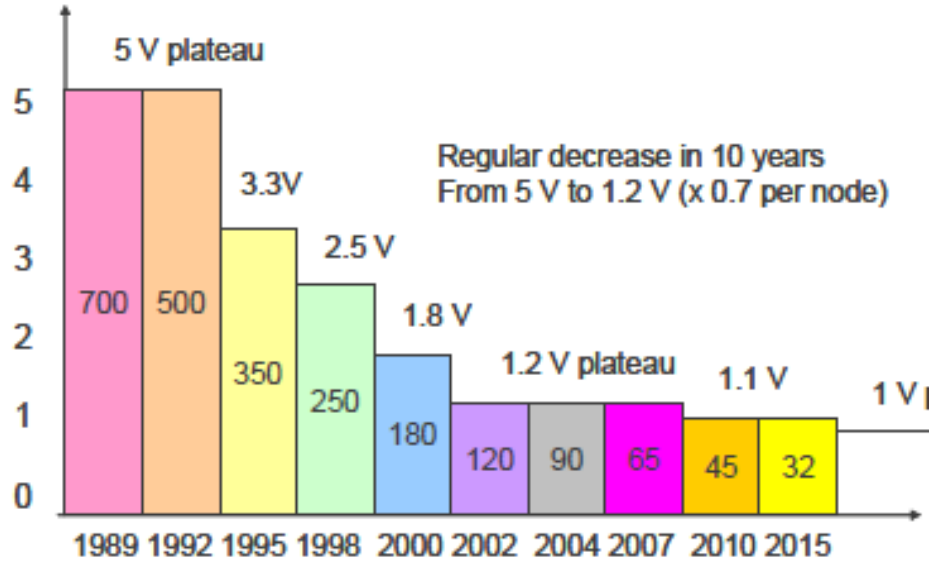
→ Area ~ $1/\alpha^2$, speed ~ α, E_{op} ~ $1/\alpha^3$ [Dennard, IEEE JSSC, 1974]

Nanometer limitations on scaling





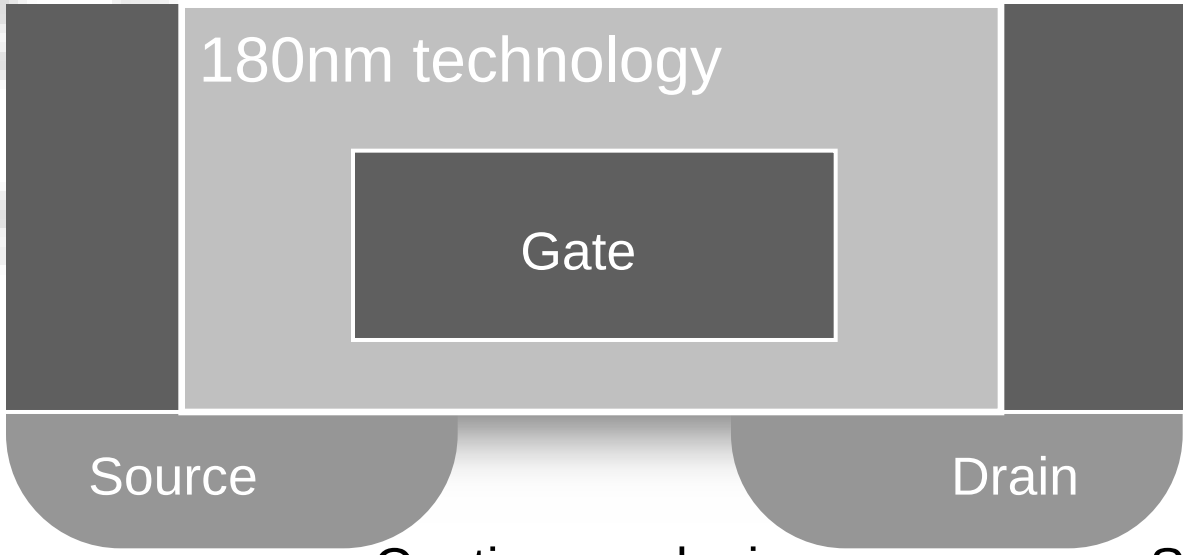
[Nowak, IBMJ, 2002]



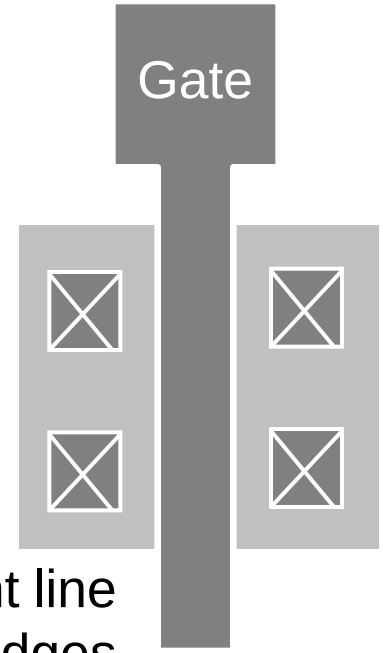
- Subthreshold leakage prevents V_t scaling
- Gate leakage prevents T_{ox} scaling
- V_{dd} is no longer scaled for speed concern
- Ultra-low-voltage operation

  → sacrificing something for improving energy efficiency

Local Variability

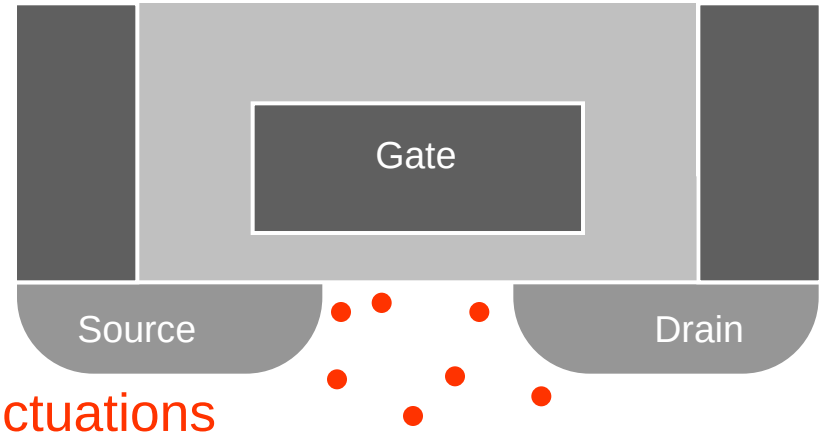


Continuous doping

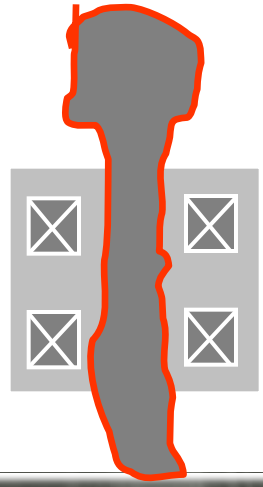


Straight line edges

45nm technology

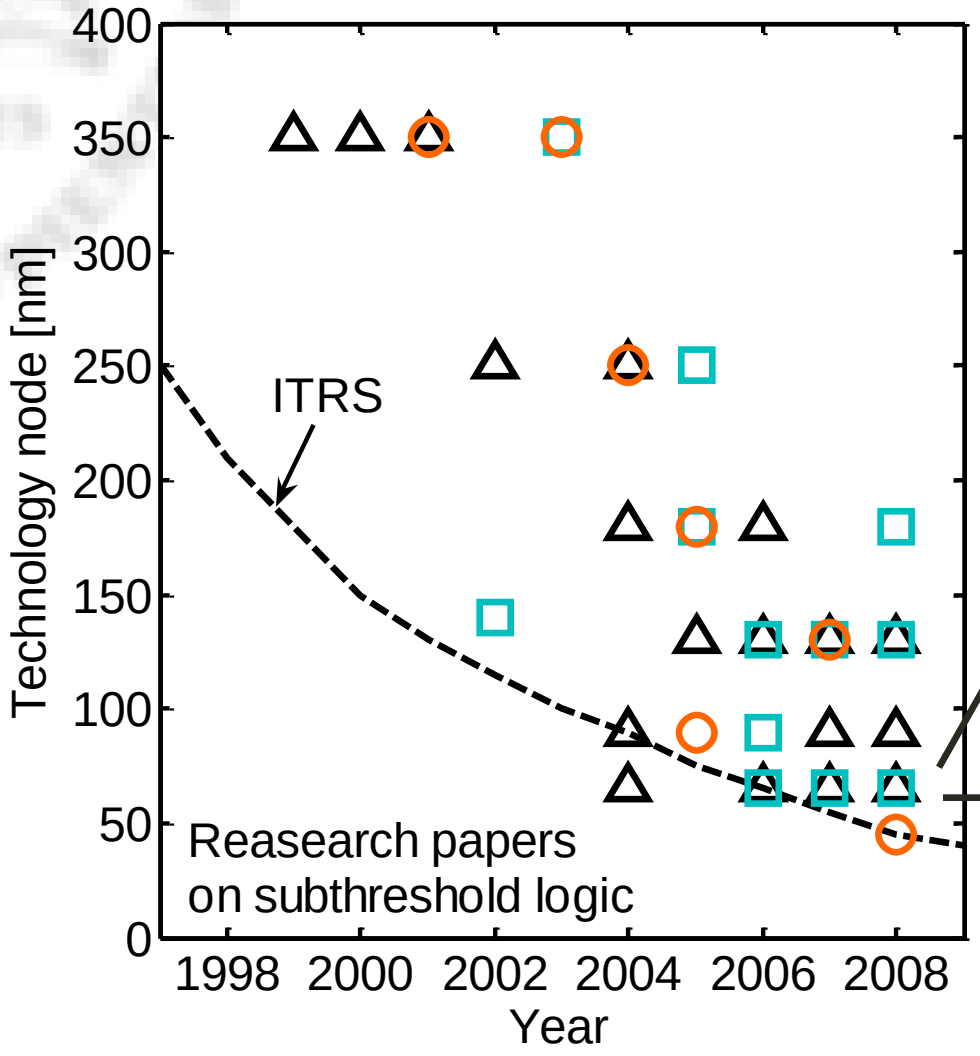


Random dopant fluctuations



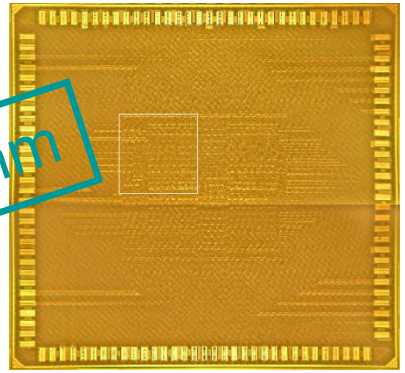
Rough line edges

Ultra-low-voltage trend



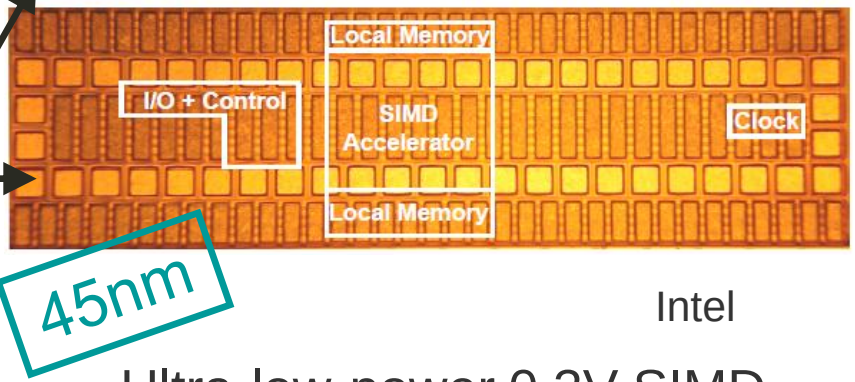
[D. Bol, IEEE Trans. VLSI, vol. 17(11), 2009]

Last chips [IEEE ISSCC'09]:



T.U. Eindhoven / NXP Semicond.

Ultra-Low-Energy/Frame 0.4V JPEG coprocessor [Pu]



Intel

Ultra-low-power 0.3V SIMD processing accelerator [Kaul]

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- **Ultra-low-voltage logic**
  - **What is the minimum V_{dd} for my circuit?**
  - Impact of technology scaling and solutions
  - Specific design issues
  - FD SOI technology
- Ultra-low-voltage SRAM
- Low-voltage co-integration with analog/RF

What is the minimum V_{dd} ?

- Absolute limit (Shannon):

  Minimum $E_{bit} = k_B T \ln(2)$

  $= q_{min} \times V_{min}$

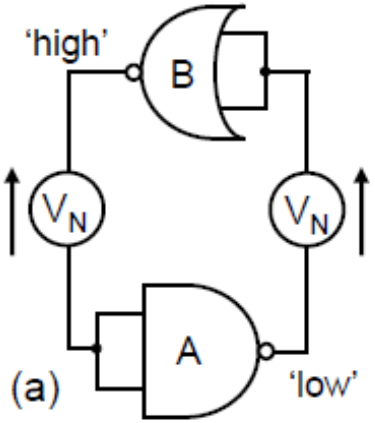
  $V_{min} \sim 18mV$ (q=e)

- Speed limit : increasing logic delay → application dependent

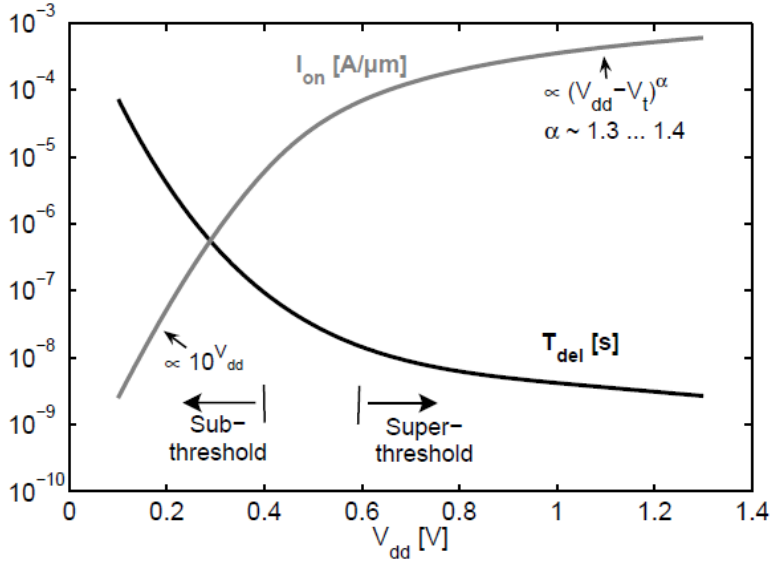
- Functional limit:

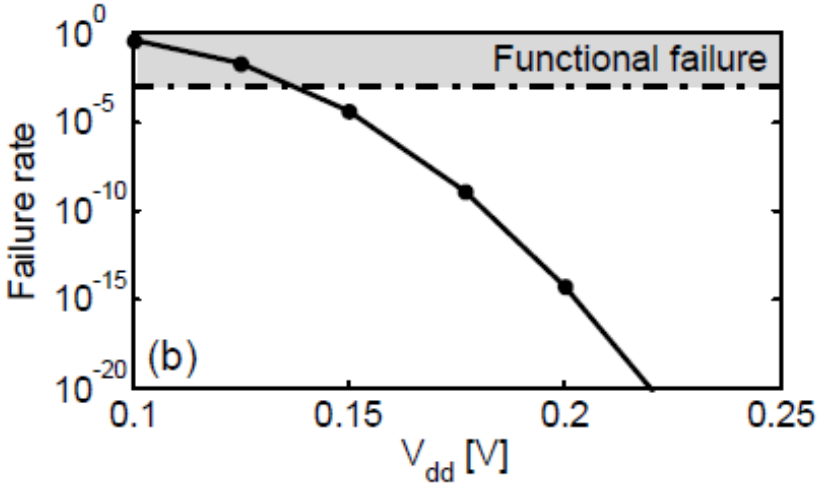
  degrading logic levels

[D. Bol, Ph.D, UCL, 2008]

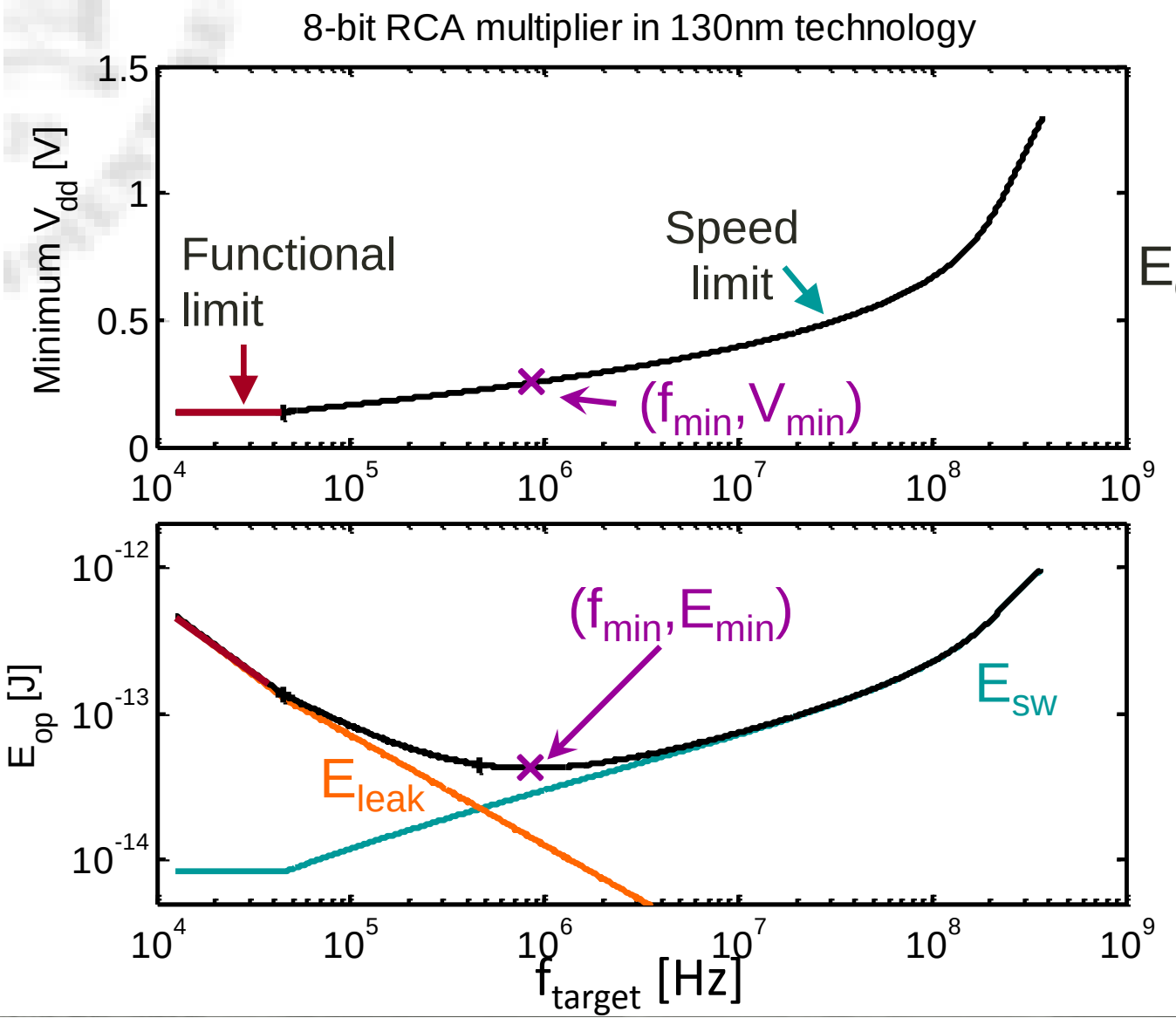


0.13µm CMOS technology





What is the minimum V_{dd} ?



$$E_{op} = \int_{0}^{T_{op}} P_{tot}\, dt$$

$$E_{op} = \tfrac{1}{2} N_{sw} C_L V_{dd}^2 + V_{dd} \times I_{leak} \times T_{op}$$

E_{leak}

- Scaling below V_{min} is not useful
- E_{min} at one particular target frequency !

[D. Bol, IEEE ICCD, 2008]

Outline

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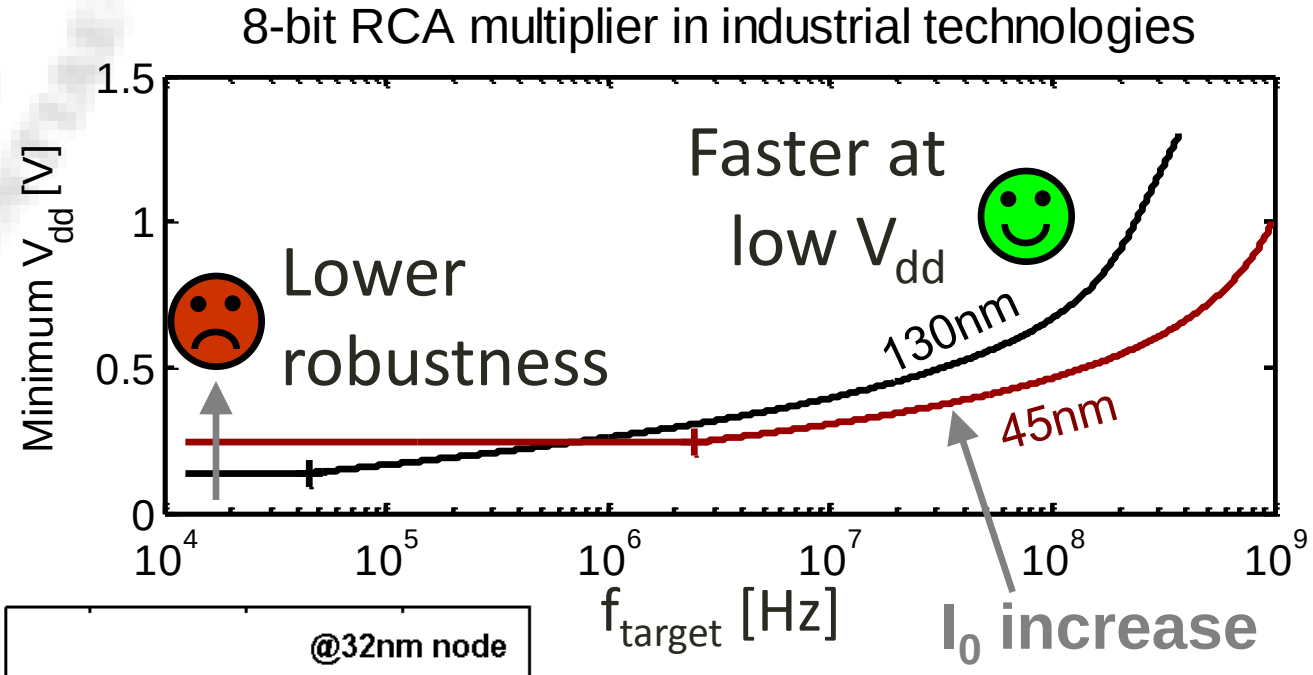
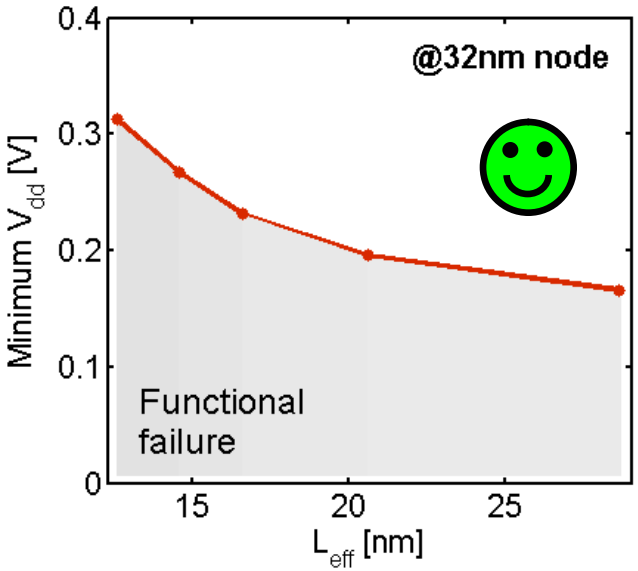
- Background: CMOS technology scaling
- **Ultra-low-voltage logic**
  - What is the minimum V_{dd} for my circuit?
  - **Impact of technology scaling and solutions**
  - Specific design issues
  - FD SOI technology
- Ultra-low-voltage SRAM
- Low-voltage co-integration with analog/RF

Impact of CMOS technology scaling



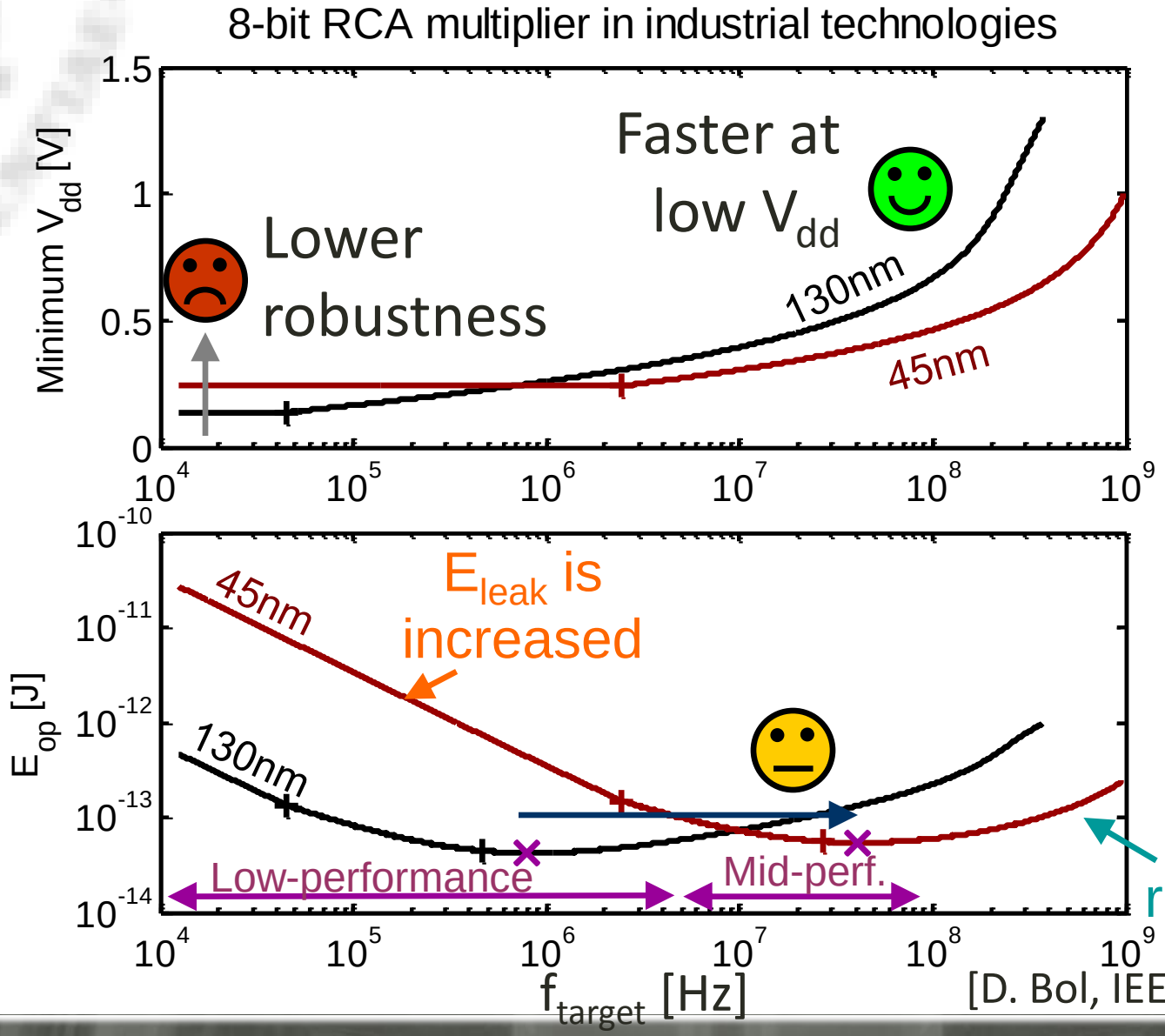
- T=25°C
- MC Spice simulations
- Foundry BSIM compact models
- GP bulk
- Std-V_t devices
- Min. L
- Constant W/L



- Logic gates with limited stack height
- Channel length upsize:
  lower DIBL and RDF variability

[D. Bol, IEEE Trans. VLSI, vol. 17(11), 2009]

Impact of CMOS technology scaling



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- Constant W/L

[D. Bol, IEEE Trans. VLSI, 2009]

Technology flavors

Commercial 45nm technology :

GP flavor

T_{ox} = 1.2 nm

Min. L_g = 35 nm

Std V_t = 0.41V

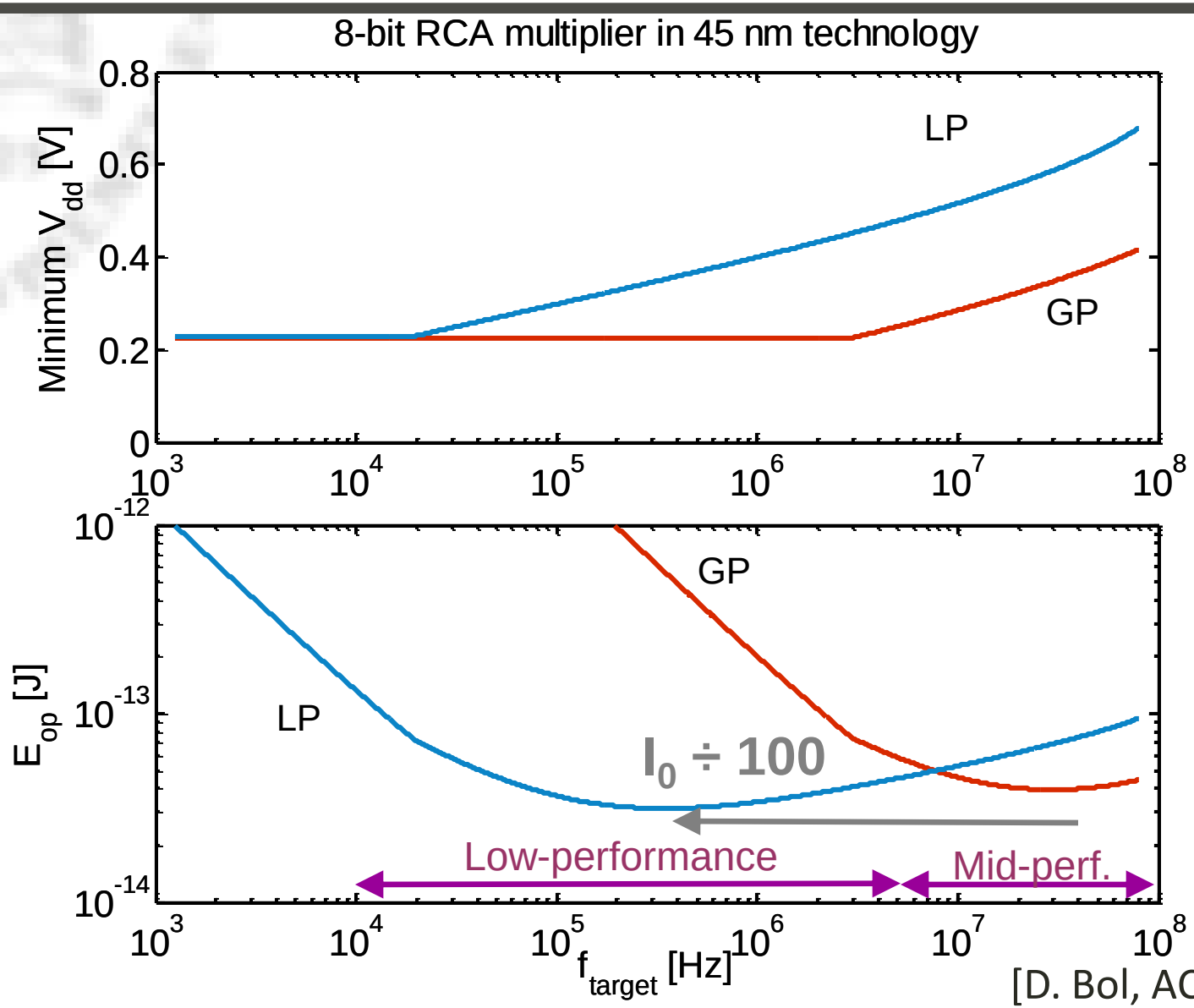
LP flavor

T_{ox} = 1.7 nm

Min. L_g = 42 nm

Std V_t = 0.55V

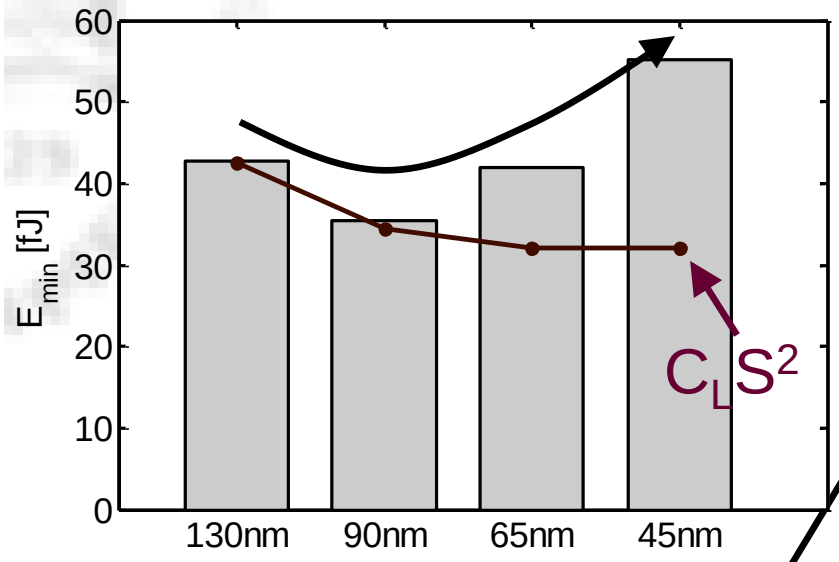
Technology flavor selection



- T=25°C
- MC Spice simulations
- Foundry BSIM4 compact models
- Min. L
- Constant W/L

[D. Bol, ACM/IEEE ISLPED, 2009]

Energy consumption



Due to increased:

- S
- Gate leakage
- DIBL
- Variability (RDF)

[D. Bol, ACM/IEEE ISLPED, 2009]

Optimum MOSFET selection

[D. Bol, ACM/IEEE ISLPED, 2009]

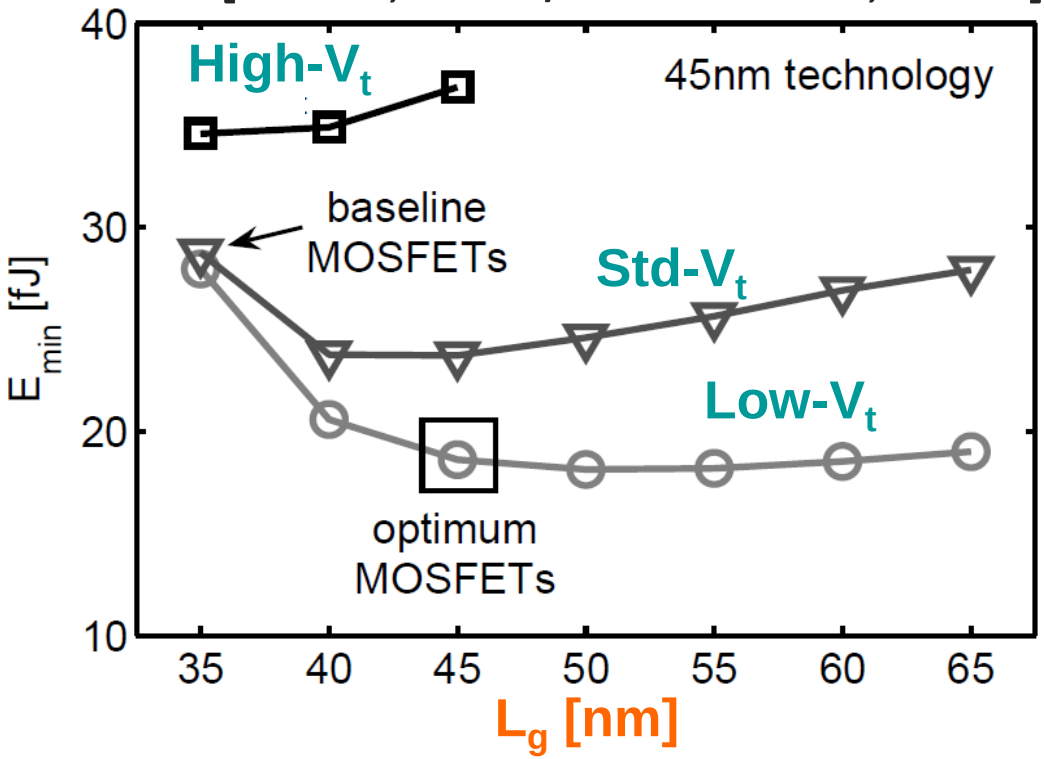
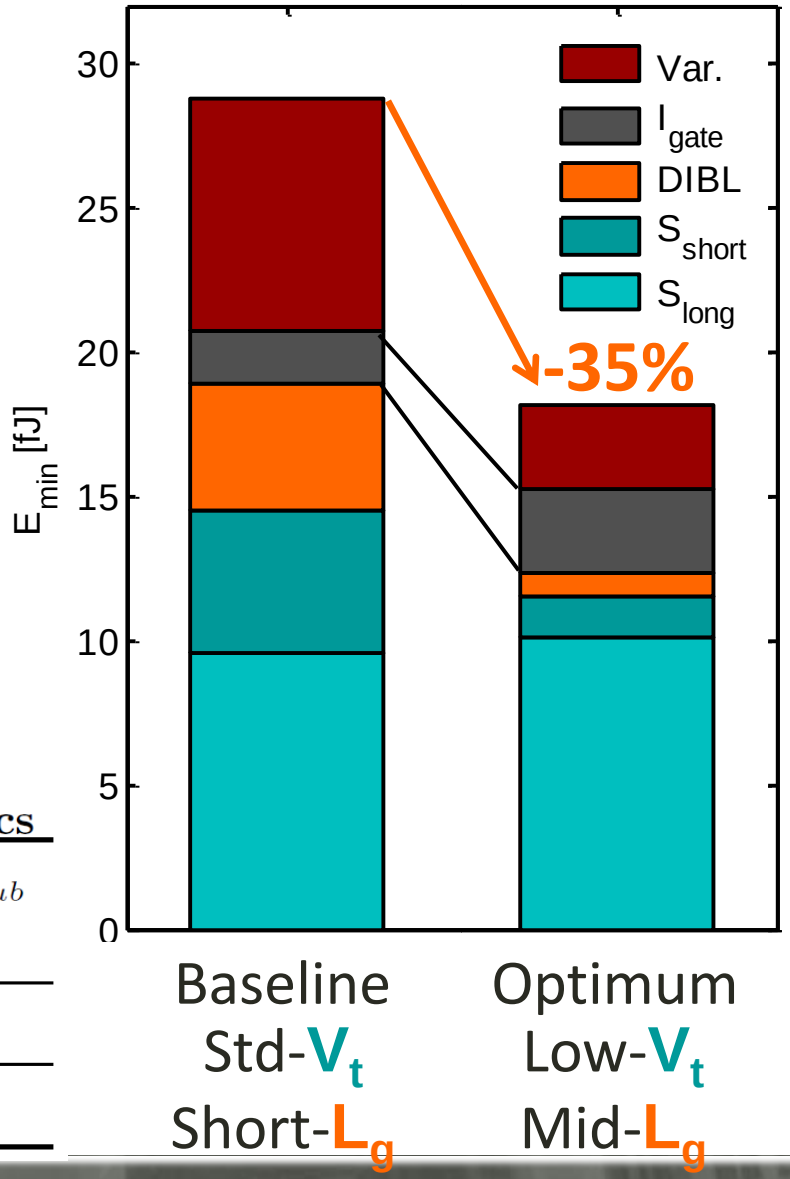
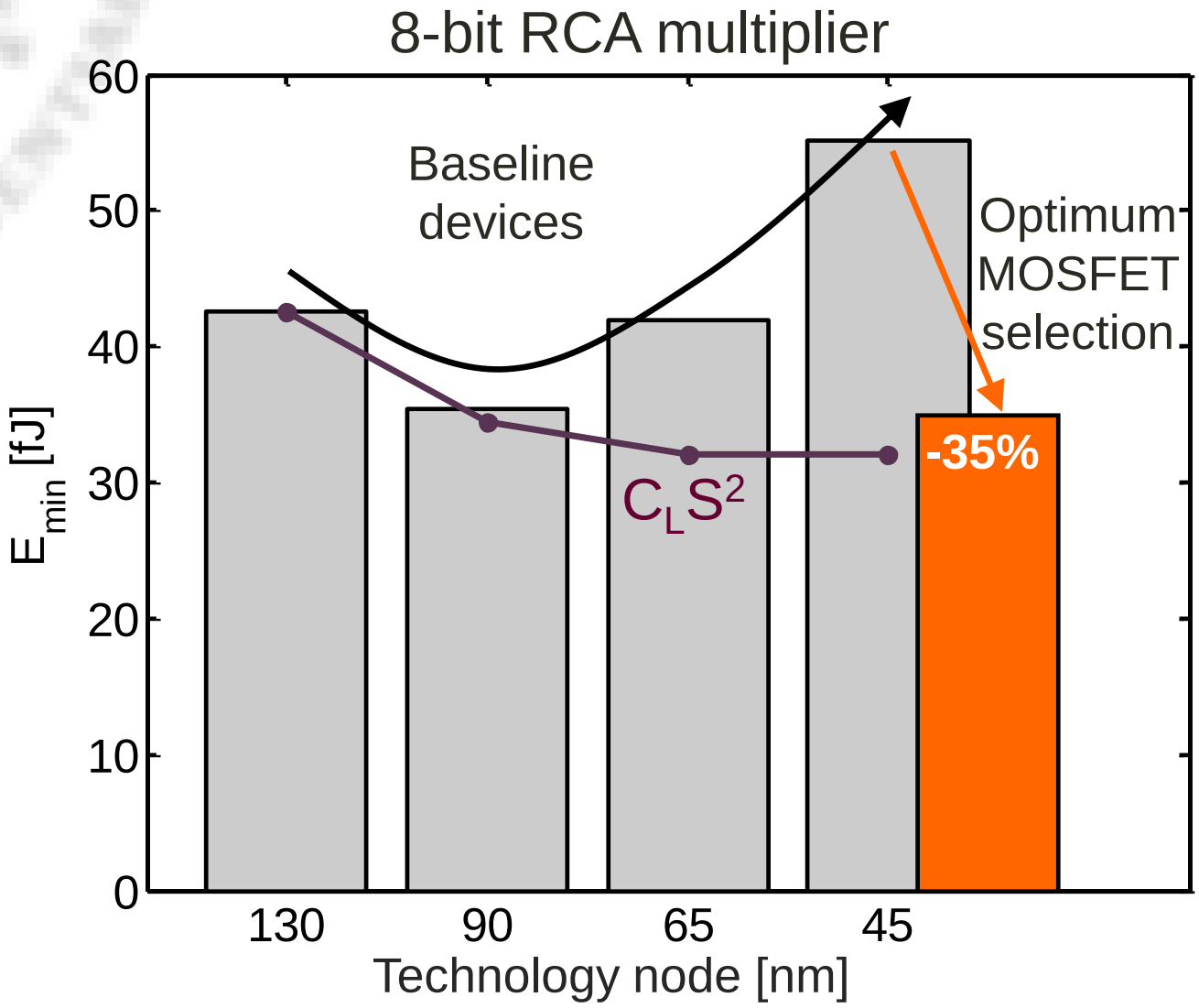


Table 1: Subthreshold MOSFET characteristics

Device type	S $[mV/dec]$	η $[mV/V]$	I_{on} var. $[-]$	I_{gate}/I_{sub} $[-]$
Baseline	92.5	183	29.7×	0.09
Optimum	81.9	83	13.1×	0.16



E_{min} scaling trend



- T=25°C
- Foundry BSIM4 compact models
- GP bulk
- Statistical variability

[D. Bol, ACM/IEEE ISLPED, 2009]

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Timing closure

- RC delays are short proportionally to logic delay [Hanson, IEEE JSSC, 2008]

  → Less repeaters

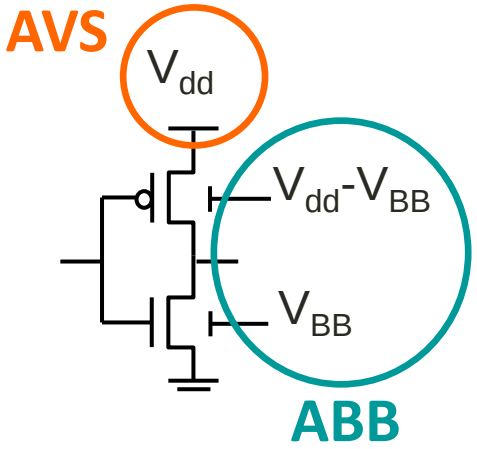
- Subthreshold operation magnifies the impact of PVT variations on logic delay:
  - process → exponential dependence on V_t
  - voltage → exponential dependence on V_{dd}
  - temperature → exponential dependence on V_t
- Worst-case design (slow, low V_{dd}, **low T°**) for timing closure implies prohibitive margins:
  - up to **20×** on maximum frequency !
  - up to **3×** on Energy per operation

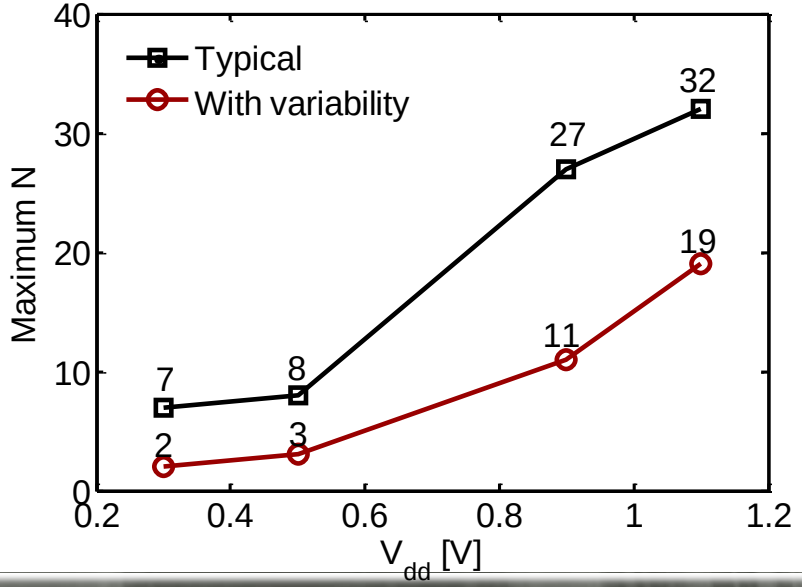
[D. Bol, ACM/IEEE ISLPED, 2009]

Timing closure

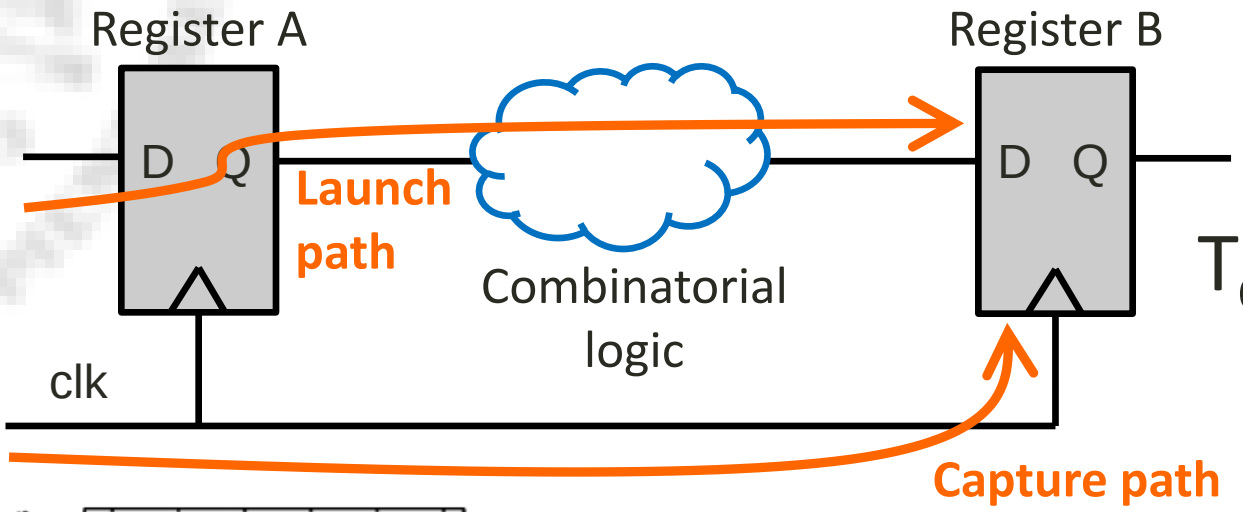
- Adaptive techniques are highly desired
  - Adaptive Frequency Scaling (AFS) – critical path replica
  - Adaptive Voltage Scaling (AVS)
  - Adaptive Body Biasing (ABB)
- ABB is more energy-efficient than AVS
- Dual-V_t assignment to save leakage in non-critical paths is not feasible because of:
  - Large delay difference std-V_t vs. high-V_t
  - High variability of short paths

[D. Bol, ACM/IEEE ISLPED, 2009]



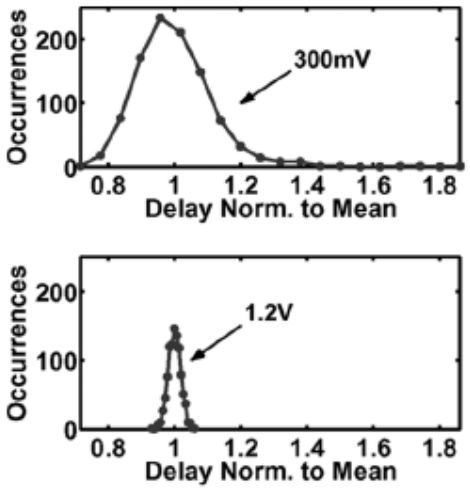


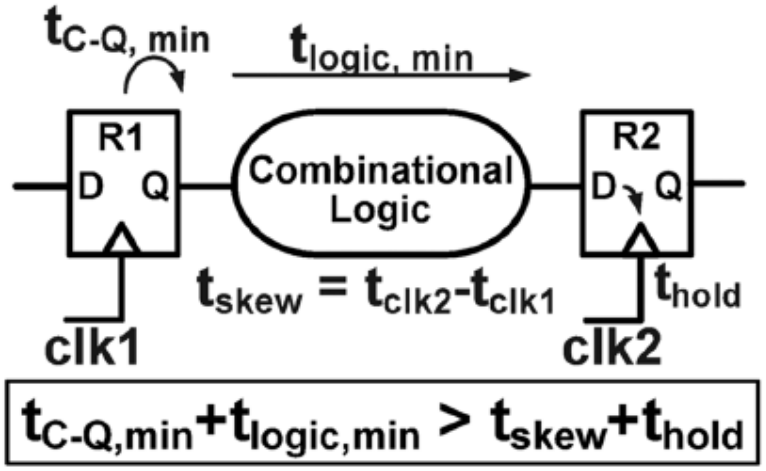
Impact of RDF on timing

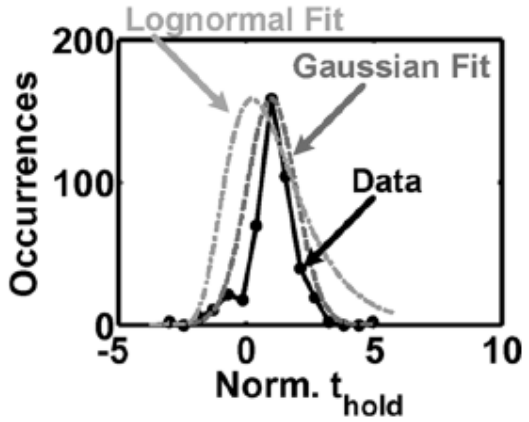


Hold-time constraint

$$T_{C\text{-}to\text{-}Q,min} + T_{path,min} > T_{skew} + T_{hold}$$







Impose hold-time margin or use Statistical STA

[Kwong, IEEE J. Solid-State Circuits, 2009]

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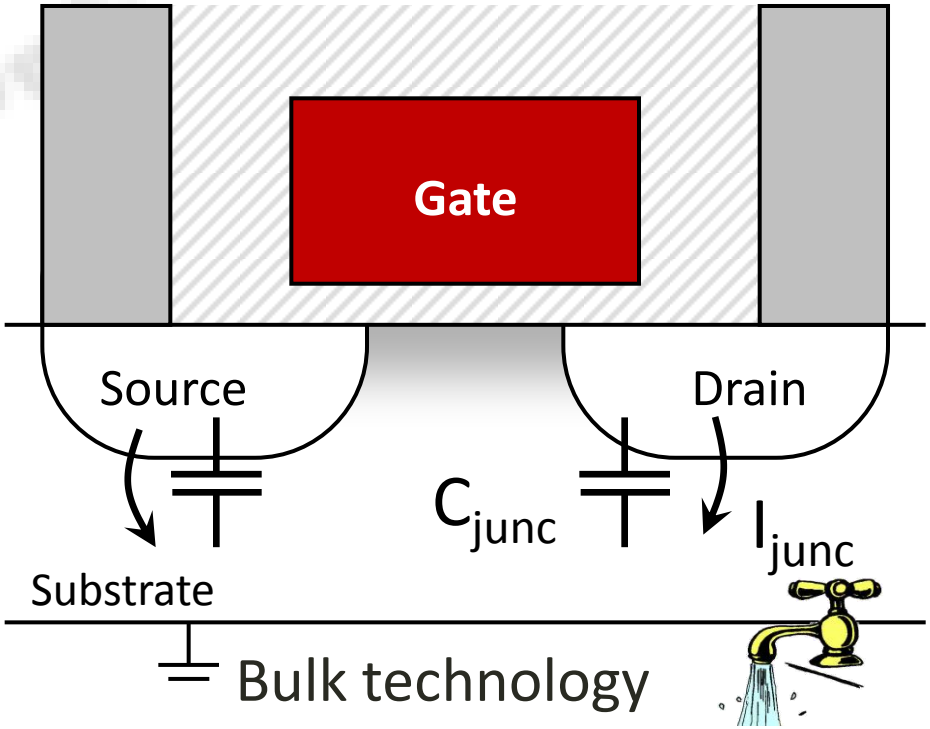
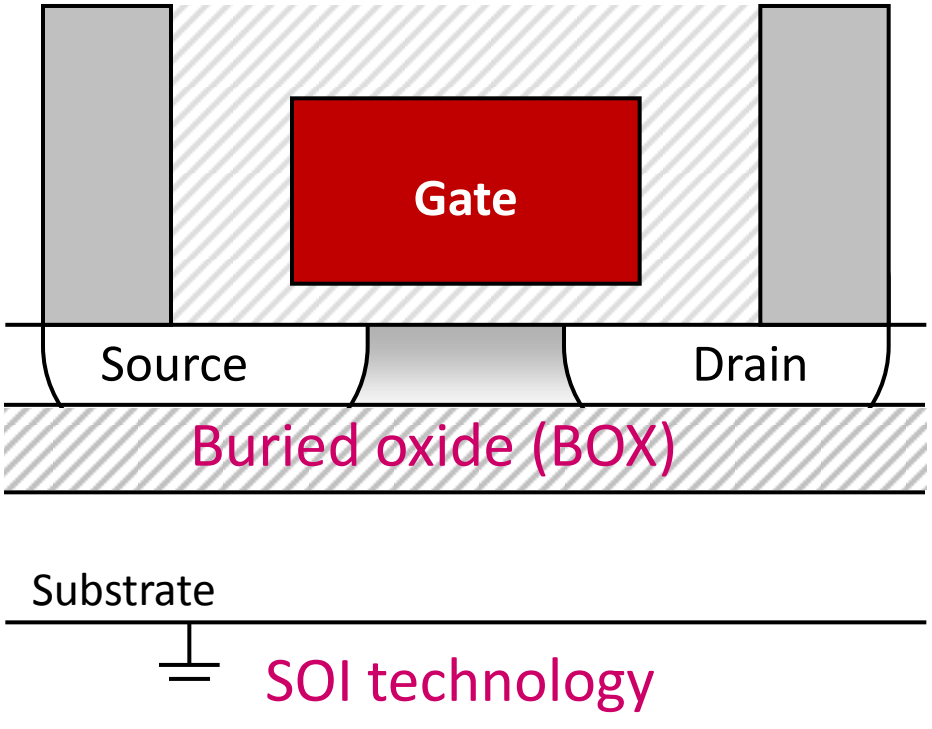
Silicon-On-Insulator (SOI)

MOSFET devices





- Lower C_{junc}, C_{M1}
- Lower I_{junc}

SOI for high-performance circuits

- Typical claims of Partially-Depleted (PD) SOI :
  - **+15/30%** speed @ iso-power
  - **-20/40%** power @ iso-speed

  < C_{junc}, C_{M1} reduction
  < larger I_{on}

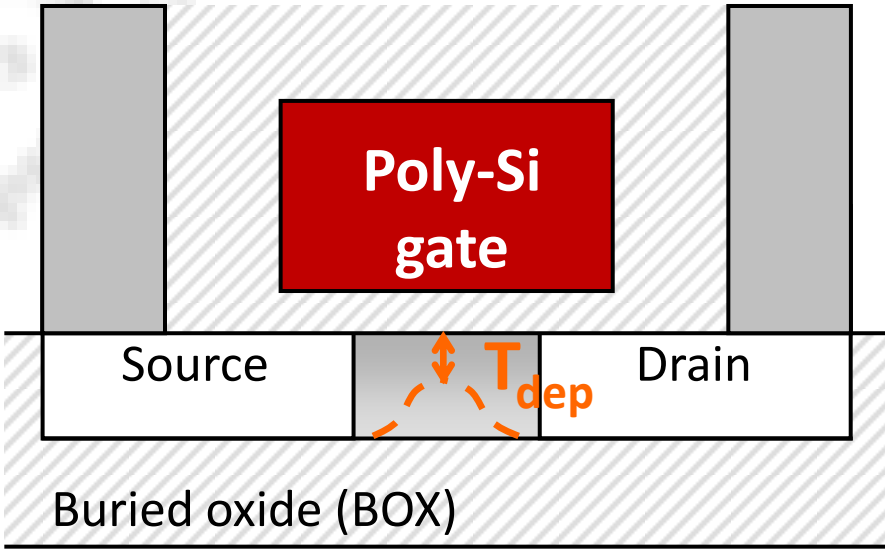
  - **area reduction**
- Drawbacks:
  - Self heating (because BOX = thermal insulator)

    
  - History effects (variable delay < floating body)

    
- Introduced by IBM at 180nm generation for high-performance microprocessors, production down to 45nm

Fully-depleted SOI technology

Partially-depleted (PD) SOI

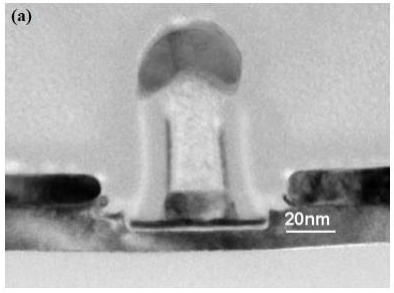


$T_{dep} \sim 1/\sqrt{N_{ch}}$

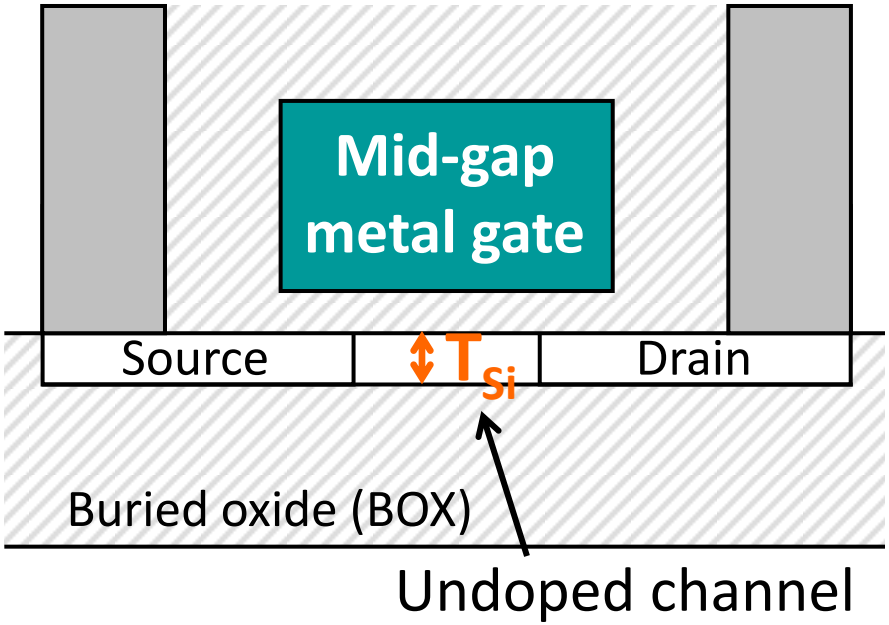
Doping similar to bulk to control the SCE

Substrate

32nm FD SOI MOSFET with high-κ/metal gate



Fully-depleted (FD) SOI



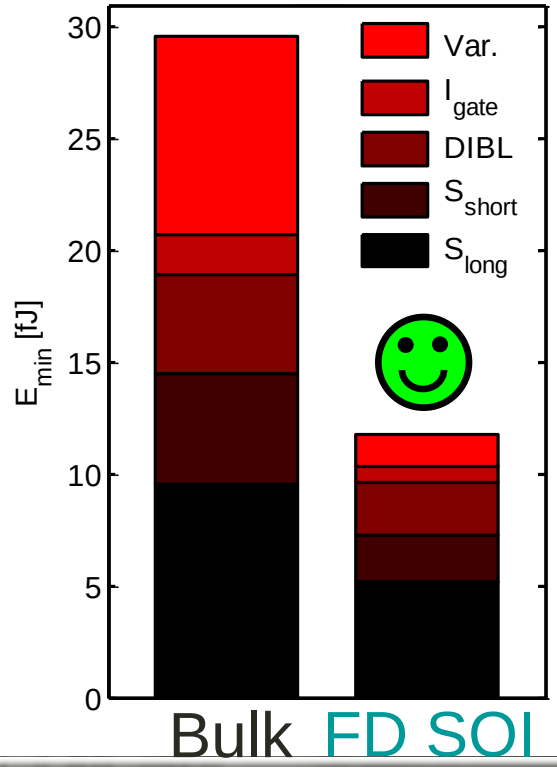
Substrate

[Weber, IEDM'08]

- No RDF → low variability
- No history effect

FD SOI for ultra-low-voltage circuits

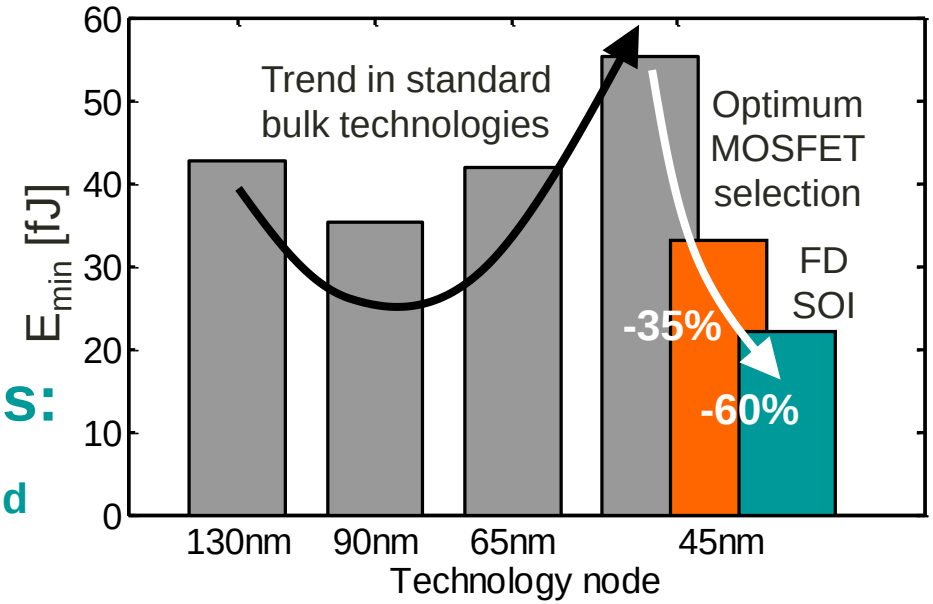
45nm technologies	S [mV/dec]	η [mV/V]	I_0 [pA/µm]	σ_{Vt} [mV]	C_L [fF/µm]
Bulk	92.5	183	340	46	21.5
Undoped FD SOI	**70.2**	**167**	340	**15.1**	**18.7**



- **Energy: -60% E_{min}**
- **Speed: 10x boost @0.4V**
- **Robustness: minimum V_{dd} -90 mV**

[D. Bol, IEEE SOI Conference, 2008]

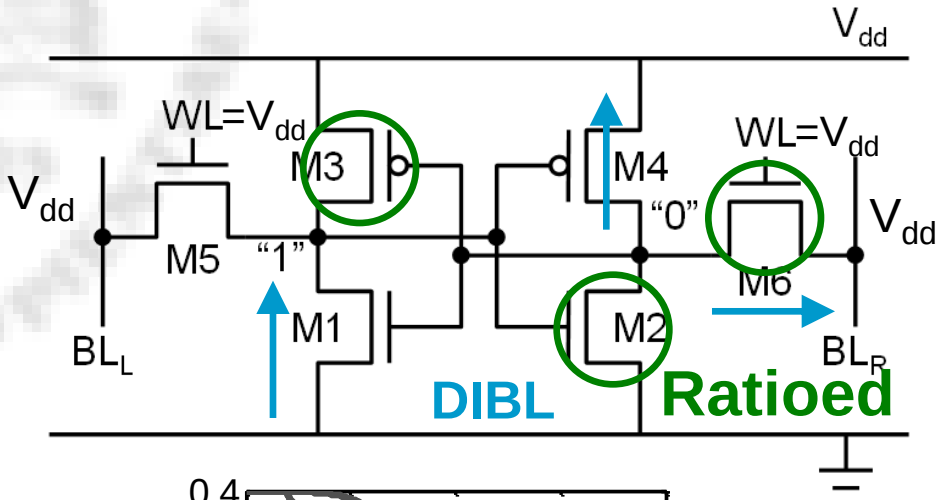
Ultra-low-power → no self-heating

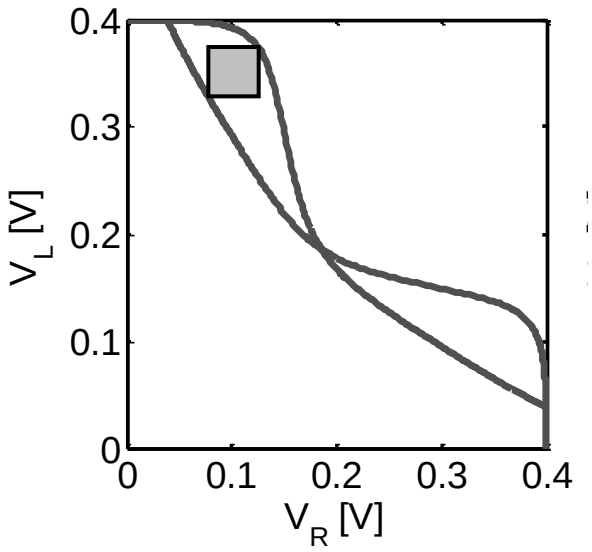


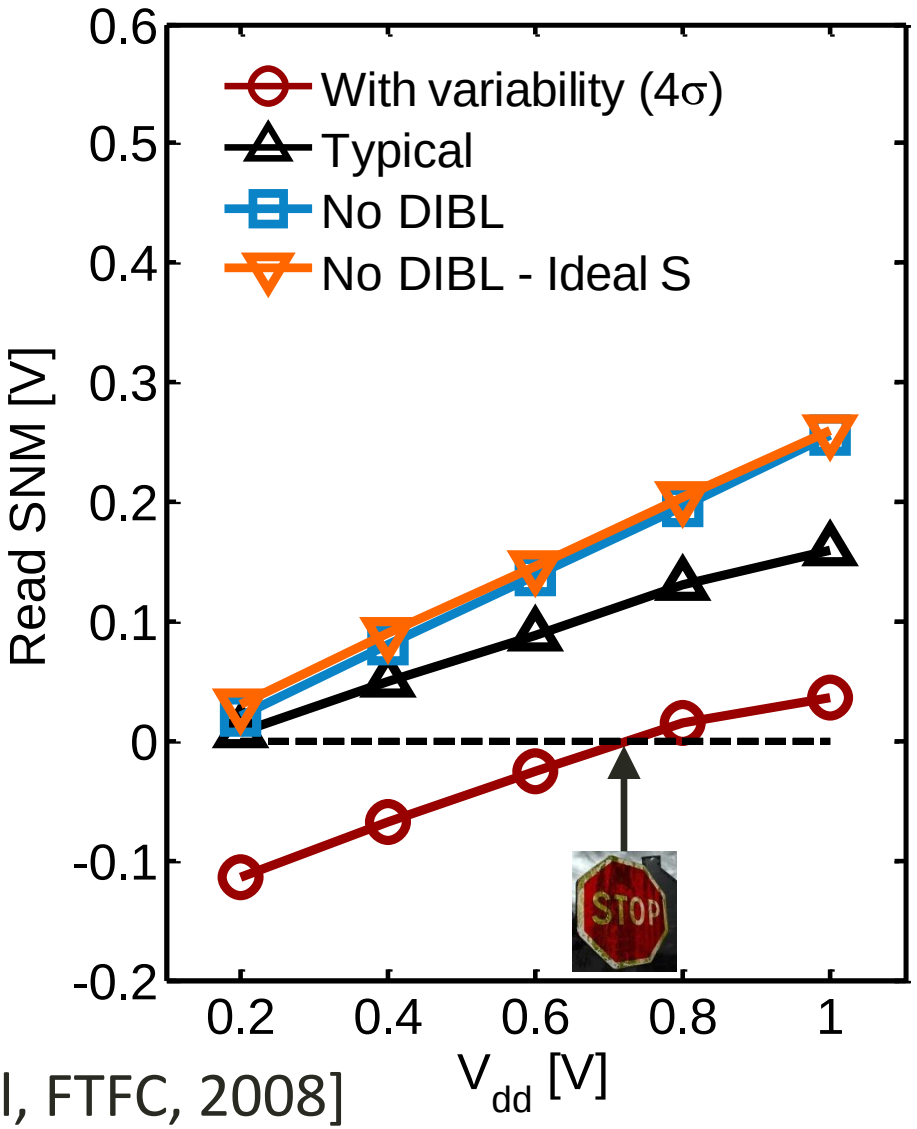
Outline

- Motivation
- Background: CMOS technology scaling
- Ultra-low-voltage logic
- **Ultra-low-voltage SRAM**
- Low-voltage co-integration with analog/RF

SRAM stability issue







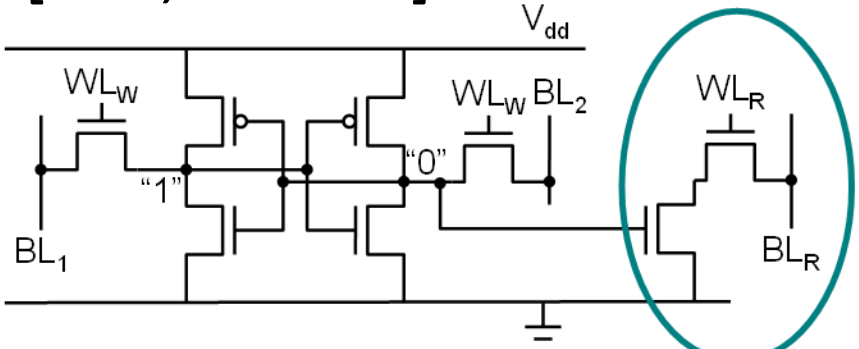
45nm technology, PTM models,
25°C, σ_{Vt} = 44mV

[D. Bol, FTFC, 2008]

Possible solutions

Read-buffer insertion:

8T SRAM [Chen, JSCC'06], [Chang, SympVLSI'07], [Verma, JSSC'08], [Kim,JSSC'08]



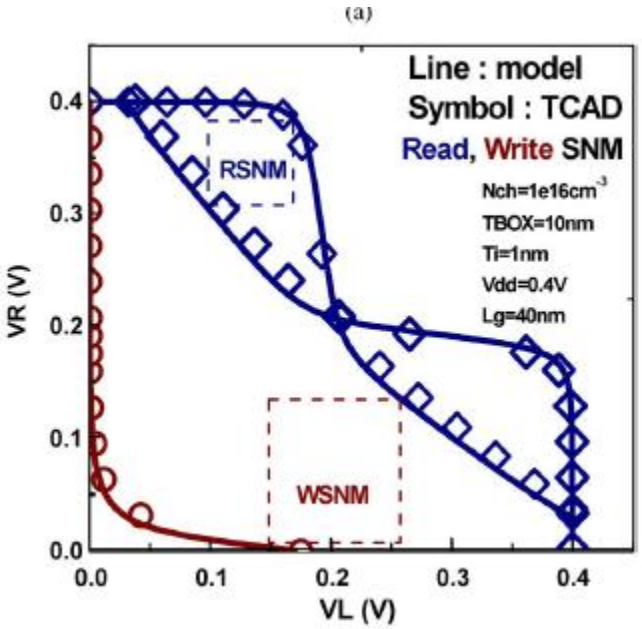
Hold SNM ↑ Read SNM

Read buffer

Area overhead

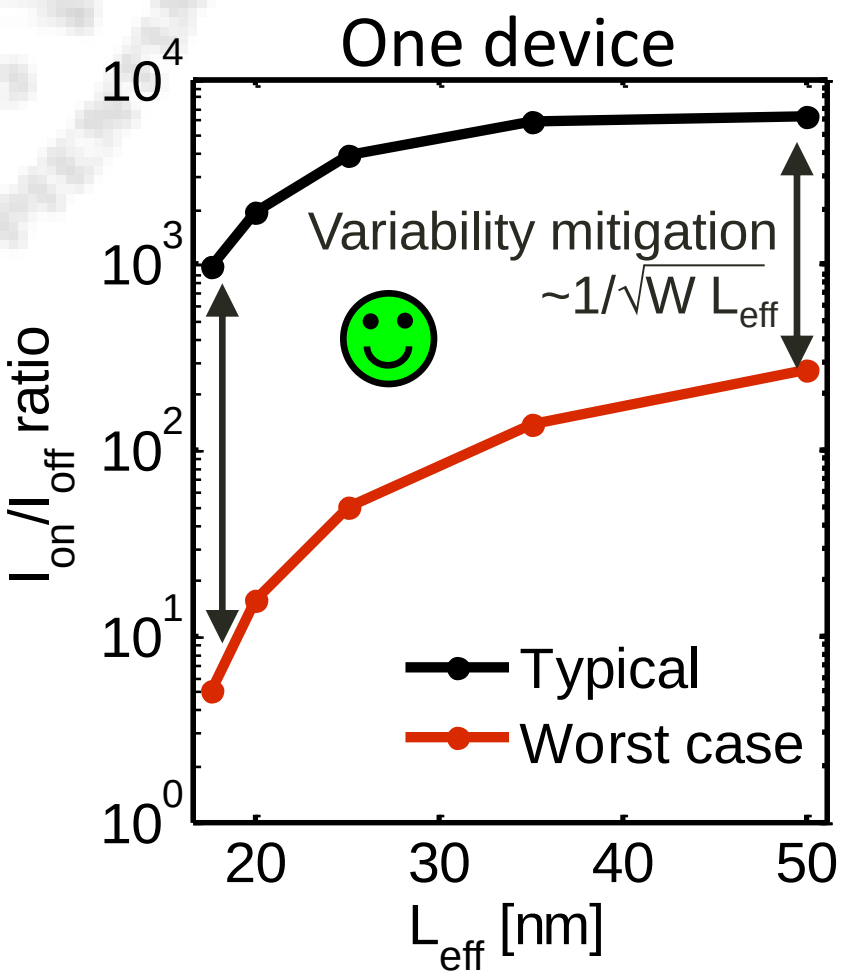
FD SOI technology

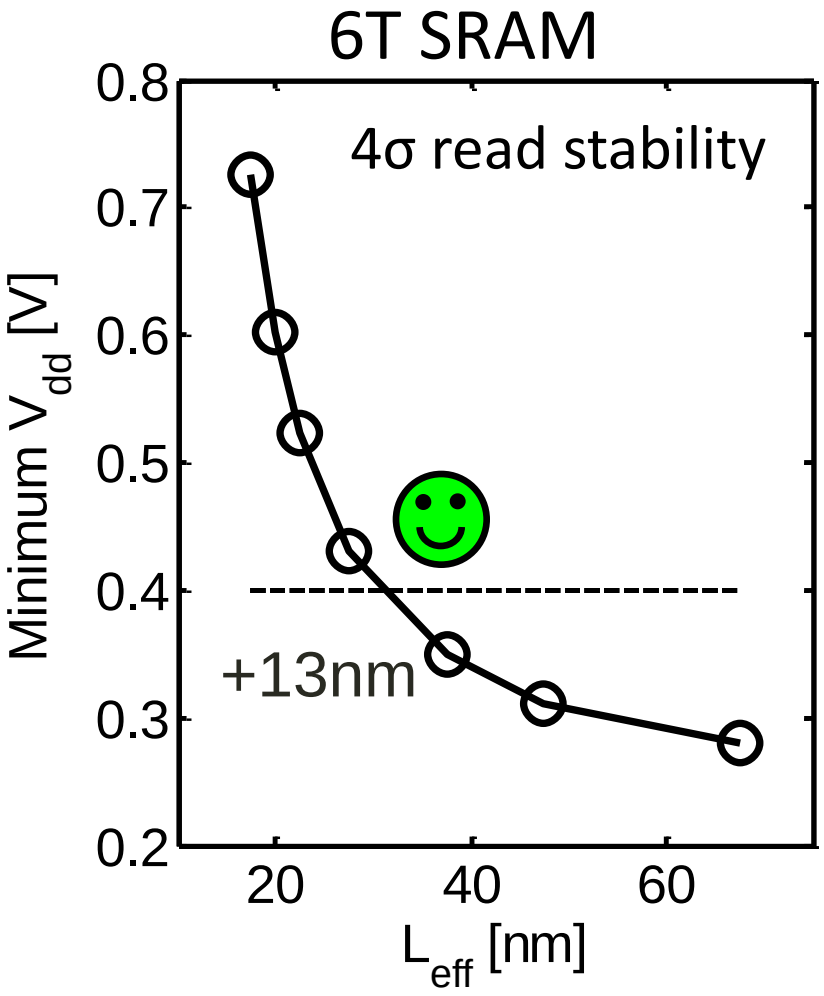
[Hu, TED'09]



- Inherently higher SNM
- Back-gate bias opportunities

Channel length upsize





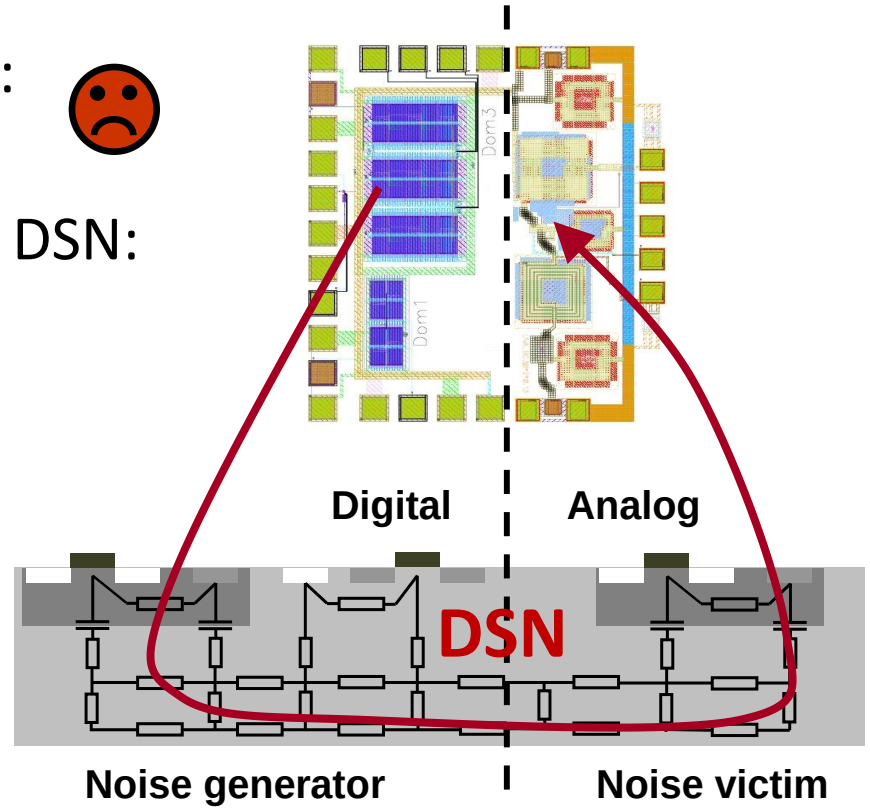
45nm technology, PTM models, 25°C,WC=3σ, σ_{Vt} = 44 mV [D. Bol, FTFC, 2008]

Outline

- Motivation
- Background: CMOS technology scaling
- Ultra-low-voltage logic
- Ultra-low-voltage SRAM
- **Low-voltage co-integration with analog/RF**

Facts

- Increasing integration :
  - Higher performance
  - Low-power consumption
  - Higher reliability
- Co-integration raises new problem: Digital Substrate Noise (DSN)
- Nanometer technologies increases DSN:
  - Low-voltage analog
    → higher sensitivity to DSN
  - More complex digital
    → higher DSN generation
  - Analog and digital closer
    → higher DSN propagation

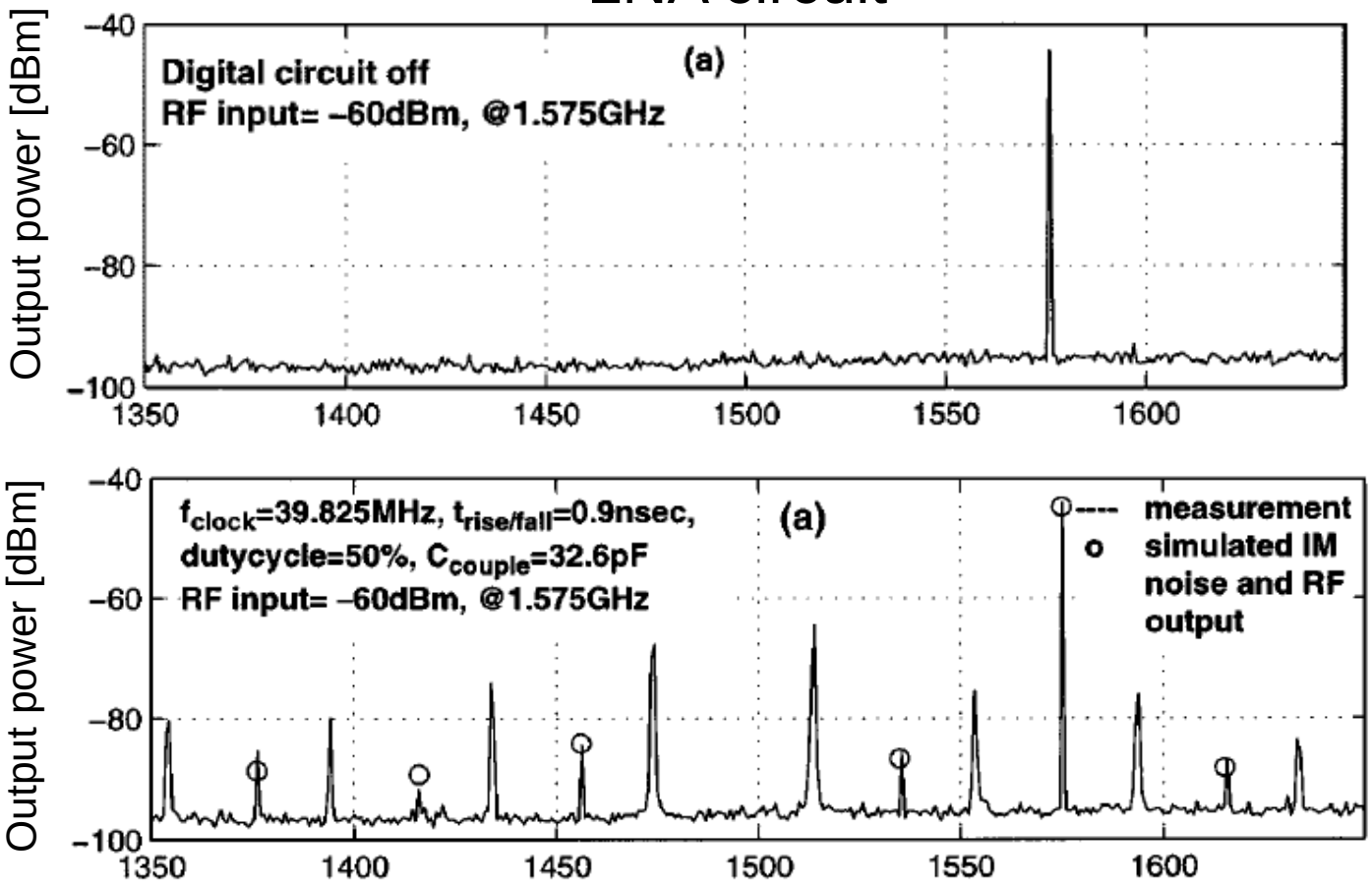


Impact of DSN

Digital OFF

Digital ON

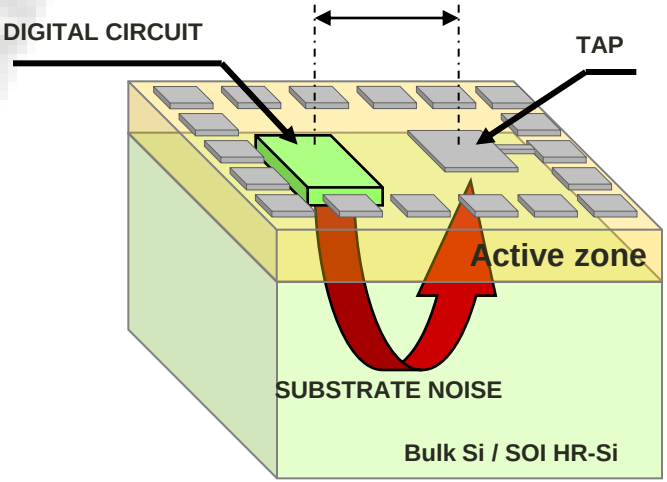
LNA circuit

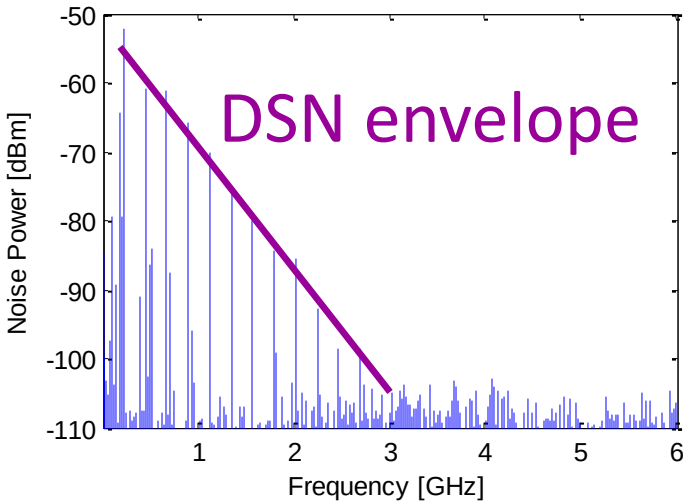


[Xu, IEEE JSSC, 2001]

Current solutions: large guard rings

Experimental setup

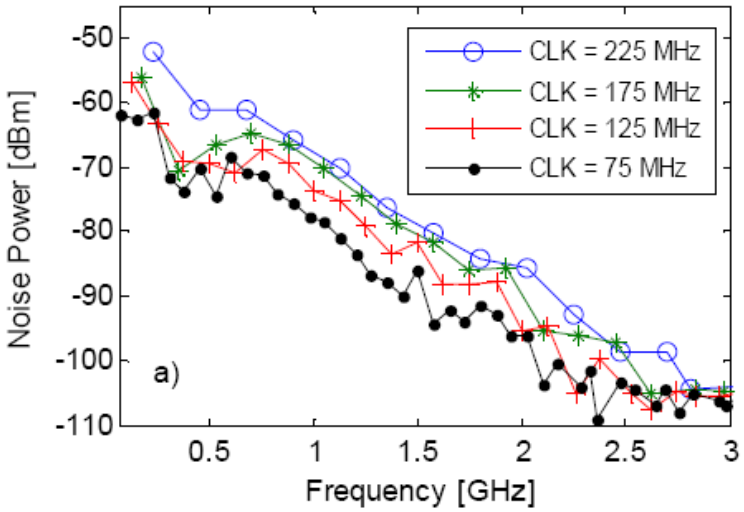


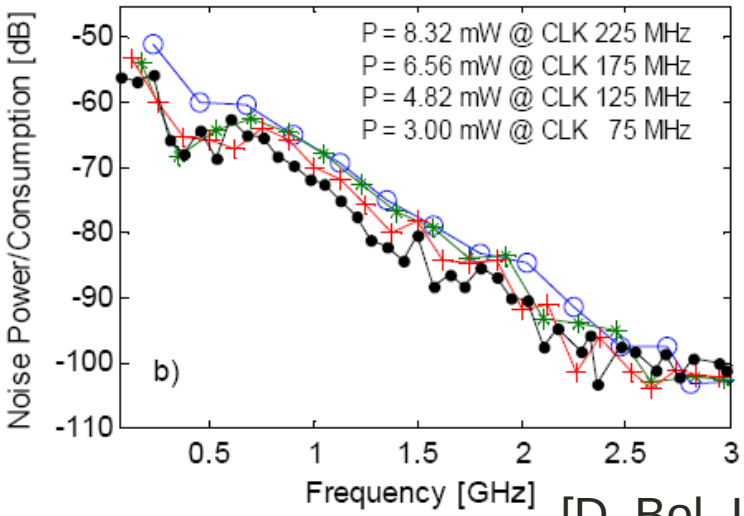


- Two circuits: ST 0.13 µm SOI and bulk CMOS technologies
- Digital circuit generating noise → inverter trees
  - Number of switching inverter trees controllable
  - Input clock signal generated by external source
- DSN probing system → active tap connected to coplanar RF pad
- DSN characterized using wideband spectrum analyzer

[D. Bol, IEEE SOI Conf. 2007][C. Roda Neve, FTFC, 2008]

DSN and frequency scaling



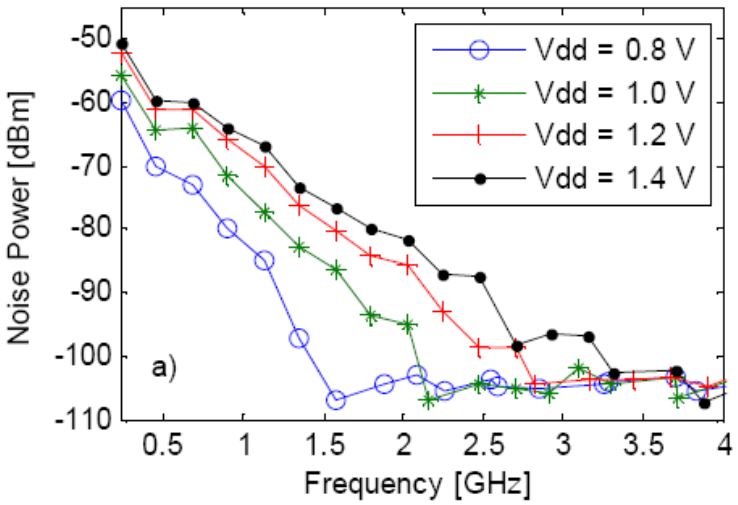


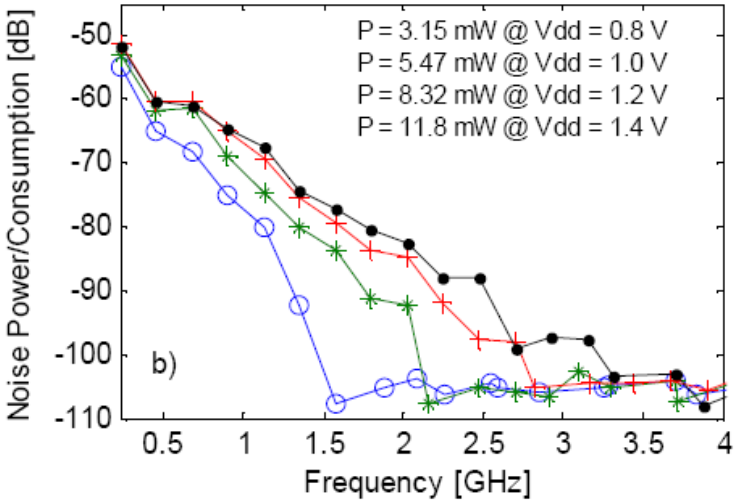
- Setup:
  - Bulk circuit
  - 8 switching inverter trees
  - 1.2 V power supply
- Lowering power reduces DSN: power divided by 3 → 10 dBm noise reduction
- Response frequency shape stays the same
- Normalizing DSN with power consumption shows close envelop curves

  → DSN is proportional to power consumption

[D. Bol, IEEE SOI Conf. 2007][C. Roda Neve, FTFC, 2008]

DSN and voltage scaling



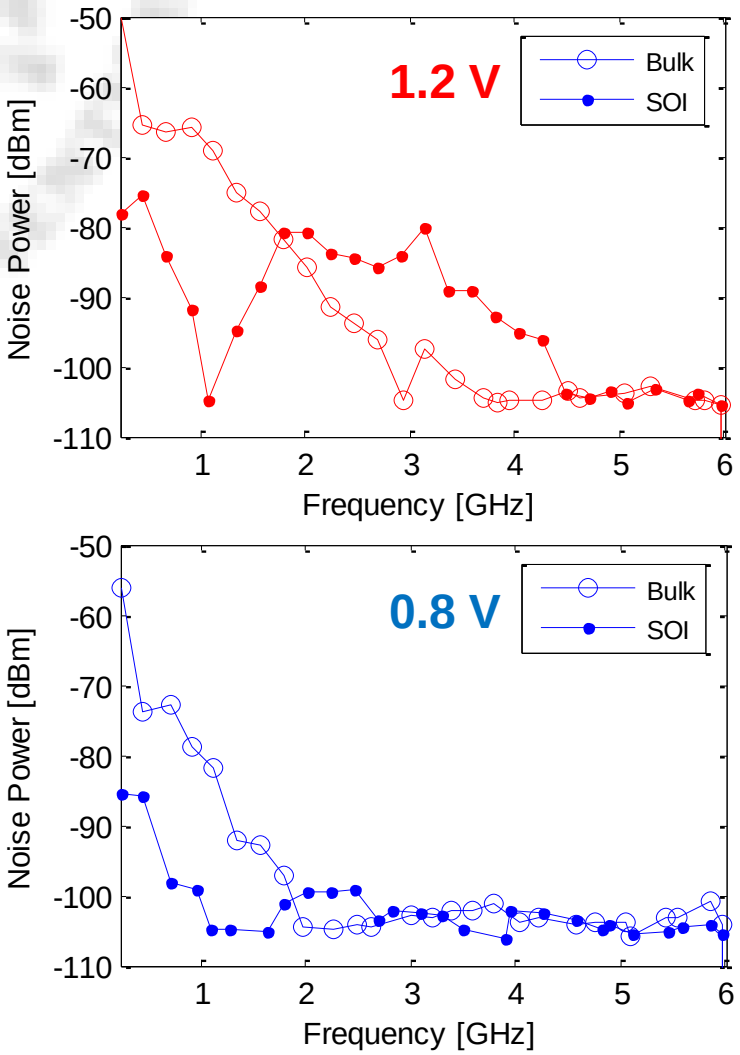


- Setup:
  - Bulk circuit
  - 8 switching inverter trees
  - 225 MHz input clock frequency
- Lowering power reduces DSN
- Lowering supply voltage reduces maximum noise frequency
- First harmonic of the normalized DSN at same level → DSN proportional to supply power
- Steeper edges at high V_{DD}
  → Higher DSN at high frequency

Low-voltage design
= low DSN generation

[D. Bol, IEEE SOI Conf. 2007][C. Roda Neve, FTFC, 2008]

DSN and SOI



- Setup:
  - 8 switching inverter trees
  - 225 MHz input clock frequency
  - 0.8 and 1.2 V supply voltage
- At 1.2 V, SOI strongly reduces DSN level at low frequency
- At 1.2 V, high frequency DSN due to power rail ringing is present in SOI → attention must be paid to supply rail in SOI
- **At 0.8 V, DSN is lower in SOI for the whole frequency range**

Low-voltage design + SOI = lowest DSN generation !

[D. Bol, IEEE SOI Conf. 2007][C. Roda Neve, FTFC, 2008]

Conclusions 1

Ultra-low-voltage logic in nanometer CMOS

- Rising functional limit on V_{dd}

  → **Logic gate with limited stack height**

  → **Channel length upsize**

- Increased E_{min} level

  → **Optimum MOSFETs (low-Vt mid-channel)**

- E_{min} operation at mid-performance frequencies

  → **Choice of technology flavor (GP for mid performances and LP for low performances)**

Conclusions 2

Ultra-low-voltage logic in nanometer CMOS

- Hold-time uncertainties
  - → **Margining**
  - → **Statistical STA**
- High sensitivity to V_t
  - → **Adaptive technique desired**
  - → **No dual-V_t technique**
- **Undoped-channel Fully-Depleted SOI technology significantly helps for all issues**

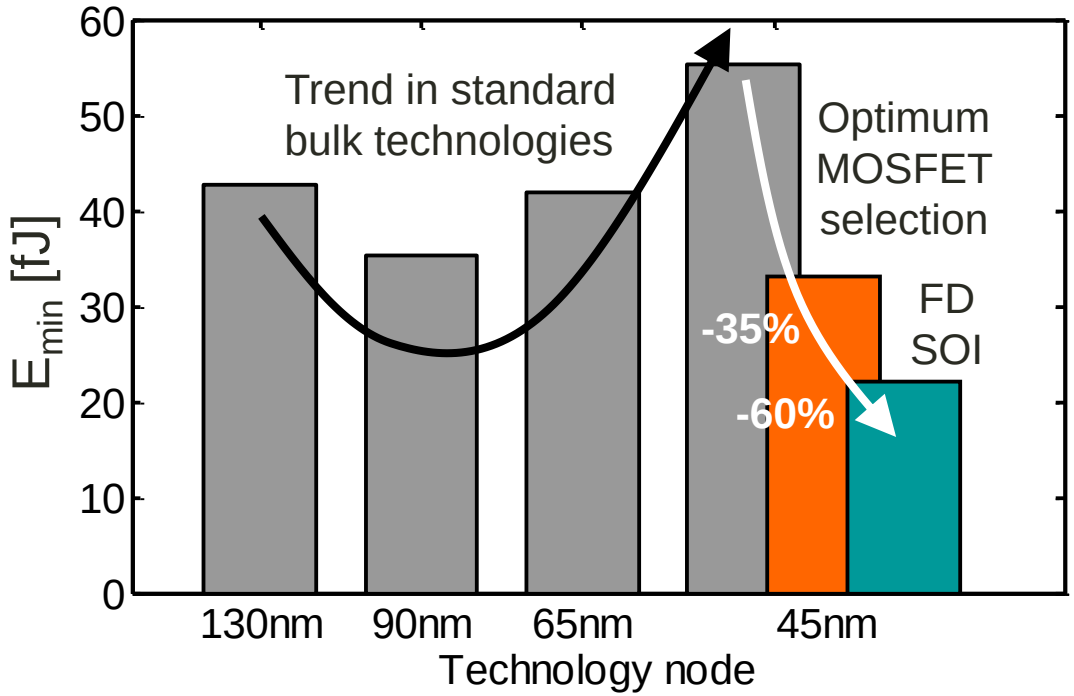
Conclusions 3

Ultra-low-voltage SRAM in nanometer CMOS

- Vanishing read SNM
  - → **8T cell**
  - → **FD SOI technology**
  - → **Channel length upsize**

Low-voltage co-integration with analog/RF

- Digital substrate noise is magnified
  - → **Low-voltage logic and SOI technology**



Thank you!

Any questions ?

[D. Bol, "Roadmap for nanometer ultra-low-power digital circuits", *www.soiconsortium.org*, 2009]

Acknowledgement:

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