

# Publications of David Bol

## PAPERS IN SCIENTIFIC JOURNALS

- C. Gimeno, D. Flandre, M. Schramme, C. Frenkel and D. Bol, "A 2.24-pJ/bit 2.5-Gb/s UWB receiver in 28-nm FDSOI CMOS for low-energy chip-to-chip communications", in *AEU International Journal of Electronics and Communications*, vol. 114, 8 p., 2020.
- P. Xu, D. Flandre and D. Bol, "Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors", in *IEEE J. Solid-State Circuits*, vol. 54, pp. 2717-2729, 2019.
- C. Frenkel, J.-D. Legat and D. Bol, "MorphIC: A 65-nm 738k-Synapse/mm<sup>2</sup> Quad-Core Binary-Weight Digital Neuromorphic Processor with Stochastic Spike-Driven Online Learning", in *IEEE Trans. Biomedical Circuits and Systems*, vol. 13, pp. 999-1010, 2019.
- R. Dekimpe, P. Xu, M. Schramme, P. Gérard, D. Flandre and D. Bol, "A Battery-less BLE Smart Sensor for Room Occupancy Tracking Supplied by 2.45-GHz Wireless Power Transfer", in *Elsevier Integration*, vol. 67, pp. 8-18, 2019.
- C. Frenkel, M. Lefèbvre, J.-D. Legat and D. Bol, "A 0.086-mm<sup>2</sup> 12.7-pJ/SOP 64k-Synapse 256-Neuron Online-Learning Digital Spiking Neuromorphic Processor in 28-nm CMOS", in *IEEE Trans. Biomedical Circuits and Systems*, vol. 13 (1), pp. 145-158, 2019.
- C. Gimeno, D. Bol and D. Flandre, "Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits", in *IEEE Trans. VLSI Systems*, vol. 26, no. 9, pp. 1807-1811, 2018.
- C. Gimeno, D. Flandre and D. Bol, "Analysis and Specification of an IR-UWB Transceiver for High-Speed Chip-to-Chip Communication in a Server Chassis", in *IEEE Trans. Circuits and Systems I*, vol. 65, pp. 2015-2023, 2018.
- F. Stas and D. Bol, "A 0.4-V 0.66-fJ/Cycle Retentive True-Single-Phase-Clock 18T Flip-Flop in 28-nm Fully-Depleted SOI CMOS" in *IEEE Trans. Circuits and Systems I*, vol. 65, pp. 935-945, 2018.
- J. Aguirre, D. Bol, D. Flandre and C. Sánchez-Azqueta, "A robust 10 Gbps duobinary transceiver in 0.13  $\mu$ m SOI CMOS for short-haul optical networks", in *IEEE Trans. Industrial Electronics*, vol. 65, pp. 1518-1525, 2018.
- G. de Streel, F. Stas, T. Gurné, F. Durant, C. Frenkel, A. Cathelin and D. Bol, "SleepTalker: A ULV 802.15.4a IR-UWB Transmitter SoC in 28-nm FDSOI Achieving 14 pJ/b at 27 Mb/s With Channel Selection Based on Adaptive FBB and Digitally Programmable Pulse Shaping", in *IEEE J. Solid-State Circuits*, vol. 52, pp. 1163-1177, 2017.
- S. Bernard, M. Belleville, J.-D. Legat, A. Valentian and D. Bol, "Ultra-wide voltage range pulse-triggered flip-flops and register file with tunable energy-delay target in 28 nm UTBB-FDSOI", in *Elsevier Microelectronics Journal*, vol. 57, pp. 77-86, 2016.
- N. Couniot, G. de Streel, F. Botman, A. Kuti Lusala, D. Flandre and D. Bol, "A 65 nm 0.5 V DPS CMOS Image Sensor With 17 pJ/Frame.Pixel and 42 dB Dynamic Range for Ultra-Low-Power SoCs", in *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2419-2430, 2015.
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- F. Botman, D. Bol, J.-D. Legat and K. Roy, "Data-dependent operation speed-up through automatically inserted signal transition detectors for ultra-low voltage logic circuits", in *IEEE Trans. VLSI Systems*, vol. 22, no. 12, pp. 2561-2570, 2014.
- G. de Streel and D. Bol, "Study of back biasing schemes for ULV logic from the gate level to the IP level" in *MDPI J. Low-Power Electronics and Applications*, vol. 4, no. 1, pp. 168-187, 2014.
- A. Barenghi, C. Hocquet, D. Bol, F.-X. Standaert, F. Regazzoni and I. Koren, "Combined Design-Time/Test-Time Study of the Vulnerability of Sub-Threshold Devices to Low Voltage Fault Attacks", in *IEEE Trans. Emerging Topics in Computing*, vol. 2, no. 2, pp. 107-118, 2014.
- J. De Vos, D. Flandre and D. Bol, "A sizing methodology for on-chip switched-capacitor DC/DC converters", in *IEEE Trans. Circuits and Syst. I*, vol. 61, no. 5, pp. 1597-1606, 2014.
- S. Bernard, A. Valentian, D. Bol, J.-D. Legat and M. Belleville, "Robust and Energy Efficient Pulse-Triggered Flip-Flop Design for Ultra Low Voltage Operations", in *ASP J. Low Power Electronics*, vol. 10, pp. 1-9, 2014.

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- [D. Bol](#), J. De Vos, R. Ambroise, D. Flandre and J.-D. Legat, "Building ultra-low-power high-temperature digital circuits in standard high-performance SOI technology", in *Solid-State Electronics*, vol. 52, no. 8, pp. 1939-1945, 2008.
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## BOOK CHAPTER

- [D. Bol](#), "Ultra-low-voltage design of nanometer CMOS circuits for smart energy-autonomous systems", in *Advanced Circuits for Emerging Technologies*, K. Iniewski (Ed.), pp. 57-83, Wiley, 2012.
- [D. Bol](#) and G. de Streel, Springer, 2020.

## PATENTS

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- [D. Bol](#) and N. Couniot, "Image sensor", US patent US9807326B2, 2017.
- [D. Bol](#), D. Flandre and J.-D. Legat, "Ultra-low-power circuits", GB patent GB0708324D0, 2007, European patent EP2151056A1, 2008 and US patent US8294492B2, 2010.

## INVITED TUTORIALS AND KEYNOTES

- [D. Bol](#), "The Rising Energy Footprint of the Internet", invited talk at DataBeer Brussels, 2019.
- [D. Bol](#), R. Dekimpe, P. Xu, M. Schramme and D. Flandre, "Can we supply IoT smart sensors wirelessly through simultaneous wireless and power transfer ?", invited talk at FETCH, 2019.

- D. Bol, "Ultra-low-power wireless communications for IoT smart sensors", invited talk in the "Sensors and Energy Harvesting" tutorial of IEEE European Solid-State Circuits Conf., 2018.
- D. Bol, "Electrical power consumption of the Internet: use cases and sustainability challenges", in Sustainable IoT Workshop of the European Nanoelectronics Consortium for Sustainability (ENCOS), 2018.
- D. Bol, "Ultra-Low-Power SoCs for Local Sensor Data Processing", invited talk in the forum "Intelligent Energy-Efficient Systems at the Edge of IoT" of IEEE Int. Solid-State Circuits Conf., 2018.
- D. Flandre, V. Kilchytska, C. Gimeno, D. Bol, B. Kazemi, J.-P. Raskin, "Measurement and modelling of specific behaviors in 28nm FDSOI UTBB MOSFETs of importance for analog / RF amplifiers", in MOS-AK workshop, 2017.
- D. Bol, "Notre usage d'Internet: écologiquement irresponsable?", in *Midis de l'Éthique*, UCL, 2017.
- D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way ? A Technology/Circuit Perspective", (invited in the Hot-Topic Session) in *Proc. IEEE SOI-3D-Subthreshold Microelectronics Tech. Unified Conf.*, 3 p., 2015.
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- D. Flandre, O. Bulteel, G. Gosset, B. Rue and D. Bol, "Disruptive ultra-low-leakage design techniques for ultra-low-power CMOS circuits", CMOS Emerging Technologies Conference, 2012.
- D. Bol, "Green SoCs for a Sustainable Internet-of-Things World", at ST Microelectronics Crolles and at CSEM Neuchâtel, 2012.
- D. Bol, "Electronics and the Environment – An Introduction", at Université catholique de Louvain, 2011.
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