Publications of David Bol

PAPERS IN SCIENTIFIC JOURNALS

BOOK CHAPTER


PATENT


INVITED TUTORIALS AND KEYNOTES

- D. Bol, “Digital design on SOI in the nanometer era - from high-performance to ultra-low-power circuits”, in tutorial on “SOI design” of the 5th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EuroSOI), 2009.

CONTRIBUTIONS IN INTERNATIONAL CONFERENCES

• G. de Streel, J. De Vos, D. Flandre and D. Bol, “A 65nm 1V to 0.5V linear regulator with ultra low quiescent current for mixed-signal ULV SoCs”, in Proc. IEEE FTTC Conference, 4 p., 2014. This paper was awarded the Best student IC Design Award of the conference.
• A. Barenghi, C. Hocquet, D. Bol, F.-X. Standaert, F. Regazzoni and I. Koren, ”Exploring the feasibility of low cost fault injection attacks on sub-threshold devices through an example of a 65nm AES implementation”, in Proc. RFIDSec Workshop on RFID Security and Privacy, 14 p., 2011.
• J. De Vos, D. Flandre and D. Bol, ”Variability and ripple analysis of an on-chip all-digital AVS system”, in Proc. VARI Workshop on CMOS Variability, 4 p., 2011.


• D. Bol, R. Ambroise, D. Flandre and J.-D. Legat, “Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications”, in Proc. IEEE International SOI Conference, 2 p., 2008. This poster presentation was awarded as Best Poster of the conference.


