Another simulation was made, with the circuit simulated in the basic form, without enhancement circuits, assuming G_m/G_{ds} and C_{gs}/C_{gd} ratios of 1000, with the biasing and signal current sources assumed as ideal. This is not realistic for the basic structures, but is reasonable when it is assumed that the additional enhancement circuits are present. The result is curve "d". The same simulation for the alternative realizations resulted in similar curves (not shown).

In the simulations, it was assumed that the circuit stabilizes completely between the switching instants. Errors due to signal-dependent clock feedthrough and other nonlinear effects were not considered (these errors are dependent on details of the final implementation).

IV. Conclusion

The direct synthesis of exact SI bilinear simulations of passive filters using second-generation Euler integrators was demonstrated. A low-pass filter was used as example, but, as in SC realizations, the method can be extended to all the filter types. Second generation integrators were used due to their superior sensitivity characteristics, and simpler final structure. Comparisons made with alternative realizations demonstrate that the proposed synthesis method is preferable, at least in the examined case of single-path filters, with unbalanced signals.

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A CMOS Analog Circuit for Gaussian Functions

J. Madrenas, M. Verleysen, P. Thissen, and J. L. Voz

***Abstract*—A simple CMOS analog circuit that performs the Gaussian function for classification applications is introduced. Combining the exponential characteristics of MOS transistors in weak inversion and the square characteristics in strong inversion the function is built. Design constraints and mismatch effects are discussed, as well as the layout optimization. The circuit has been designed in a SOI technology and manufactured. Good experimental results are obtained which shows that the circuit is suitable to be included as a building block of an IC to perform classification tasks or other possible applications.**

I. Introduction

Data classification is an application where neural algorithms show promising capabilities [1]. In many neural classification algorithms, the decision on the class associated to an input pattern is based on the comparison of the different probabilities to belong to each possible class [2]. In the associated calculations, the probability density functions are needed. In many cases these functions can be modeled by normal distributions (or combinations).

Even though these algorithms can be conveniently implemented on workstations, in real time, portable and other space or power constrained applications, dedicated hardware implementation is a promising solution [3]. Because of its good integration of processing capabilities, the analog approach has been taken in many CMOS neural network IC's. In this paper a compact analog circuit that generates the Gaussian function for neural or signal processing algorithms is proposed.

Other approaches to implement in CMOS technologies the Gaussian function in weak inversion operation [4] or as a piece-wise linear approximation [5] have been reported. The circuit we propose generates a true Gaussian form in weak inversion using only five transistors and can approximate the function also in strong inversion operation mode. The Gaussian function is defined in (1), where x is the input and y the output of the

$$y = Ae^{-\frac{x^2}{2\sigma^2}} \tag{1}$$

function, and A, σ are adjustable constants which define, respectively, the amplitude and the width of the Gaussian function.

The function is constructed in two steps. First the input x is squared by means of the quadratic *V-I* characteristic of a MOS transistor in saturation, secondly a negative exponential obtained with a MOS transistor operating in weak inversion mode completes the transfer function. If the input variable is a current instead of a voltage, the MOS transistor can be replaced by a current squarer circuit [6].

In our approach, the circuit performs one half of the function. Since the Gaussian is an even function, the other half side can be easily

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implemented by rectifying the input variable [3] (or, in the case of using a current squarer this is directly done).

Sections II and III present the exponential circuit principle and the Gaussian circuit. The two next sections consider the modification of the σ parameter and mismatch effects, which lead to design constraints. In Sections VI and VII the design and experimental results are reported. Section VIII discusses the operation in strong inversion. Finally the conclusion of this brief is presented.

II. Principle of the Exponential Circuit

The principle of the exponential circuit is shown in Fig. 1(a). V_{SX}, V_{DX}, and V_{GX} are, respectively, the source, drain and gate voltages of transistor M_X. In this circuit the two MOS transistors form a current mirror, with resistors R_1 and R_2 serially connected to the transistor sources. If the two resistors R_1 and R_2 are identical, currents I_o and I_R will also be identical at the equilibrium, when there is no current I_1. When a current I_1 is sourced to the cell, voltages V_{S1} and V_{S2} differ, and the circuit behaves as a Widlar or logarithmic current mirror [7].

Reference current I_R is set small enough to make transistors M_1 and M_2 working in weak inversion. Under this condition, we can express the currents in M_1 and M_2 as [8]

$$\begin{aligned} I_R &= I_s e^{\frac{V_{G1}}{nu_T}}\left(e^{-\frac{V_{S1}}{u_T}} - e^{-\frac{V_{D1}}{u_T}}\right) \\ I_o &= I_s e^{\frac{V_{G2}}{nu_T}}\left(e^{-\frac{V_{S2}}{u_T}} - e^{-\frac{V_{D2}}{u_T}}\right) \end{aligned} \tag{2}$$

where $u_T = KT/q$, n is the slope factor (slightly higher than unity), and I_s is the specific current, related to technology parameters. V_{D1} and V_{D2} are much higher than u_T at the operating point of the transistors; since we have also $V_{G2} = V_{G1}$, we obtain.

$$I_R \cong I_s e^{\frac{V_{G1}}{nu_T}} e^{-\frac{V_{S1}}{u_T}}, \quad I_o \cong I_s e^{\frac{V_{G1}}{nu_T}} e^{-\frac{V_{S2}}{u_T}}. \tag{3}$$

Substituting V_{S1} and V_{S2} leads then to

$$I_o = I_R e^{\left(\frac{R_1 I_R - R_2 I_o - R_2 I_1}{u_T}\right)}. \tag{4}$$

Finally, assuming that I_1 is greater than I_R (and thus I_o lower than I_R), which can be easily guaranteed since I_R is small as stated before,

$$I_o \cong I_R e^{-\frac{R_2 I_1}{u_T}} = I_R e^{-\frac{V_{S2}}{u_T}}. \tag{5}$$

The output current I_o decreases exponentially with current I_1, which linearly modifies $V_{S2} \cdot R_2$ determines the exponential constant. In order to have a good control on the output current, R_1 is set equal to R_2 in further analysis, and thus $I_o = I_R$ for $I_1 = 0$. Furthermore, by taking $R_1 = R_2$ (5) holds not only for $I_1 \gg I_R$, but also for values of I_1 in the order of I_R (since $R_1 I_R - R_2 I_o$ approaches 0).

Notice that the circuit has a current input instead of the usual voltage input. This allows a higher flexibility for input current summing, and also, the biasing of the circuit is straightforward done by the reference current.

III. The Gaussian Circuit

The complete circuit is shown in Fig. 1(b) M_3 and M_4 work in their linear region and are used in strong inversion as variable resistors. In this region, the drain current can be expressed by

$$I_D = \beta(V_D - V_S)\left[V_C - V_{TN} - \frac{n}{2}(V_D - V_S)\right]. \tag{6}$$

The gate voltage V_C controls the output conductance of M_3 and M_4, whose value is approximately given by (since $V_{S3} = V_{S4} = 0$)

$$g_{ds3,4} = \frac{\partial I_{D3,4}}{\partial V_{D3,4}} \cong \beta_{3,4}(V_C - V_{TN3,4}) \tag{7}$$

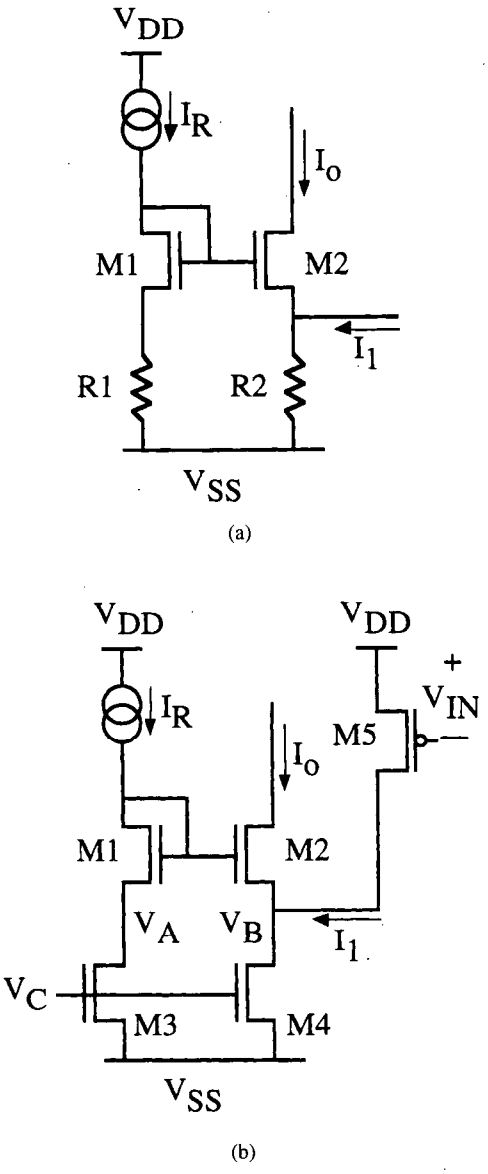

Fig. 1. (a) Principle of the exponential circuit. (b) The Gaussian circuit.

where we assume that V_{D3}, V_{D4} are small for the linear operation

$$V_C - V_{TN} \gg V_{D3}, V_{D4}. \tag{8}$$

This condition guarantees the operation far from the saturation region. M_5 works in saturated region and in strong inversion. Its drain current is thus a square function of the gate voltage

$$I_1 = \frac{\beta_5}{2n}(V_{IN} - |V_{TP}|)^2 \tag{9}$$

where V_{IN} is the gate voltage of M_5 referred to V_{DD} [Fig. 1(b)]. Combining (5) and (9), the global transfer function of the cell is then

$$I_o = I_R e^{-\frac{I_1}{u_T g_{ds4}}} = I_R e^{-\frac{\beta_5 (V_{in} - |V_{TP}|)^2}{2nu_T \beta_4 (V_C - V_{TN})}} \tag{10}$$

which has the desired Gaussian form given in (1), provided $x = V_{in} - |V_{TP}|$. The constant V_{TP} can be compensated (if necessary) by an offset voltage generated with a diode-connected MOS transistor biased by a small current, and connected to M_5 gate.

IV. Modification of σ

The value of σ in (1) is controlled by V_C in the circuit, but it could be controlled by a multiplying factor of the input signal as well. If it is to be controlled internally, its limits of variation can be calculated.

The lower limit of I_o (Fig. 1) for a maximum input current I_1 sets an upper limit for V_{S2} which in turn determines a minimum value for V_C, (8) having to apply for the whole dynamics of the output current. The upper bound of I_o is obviously I_R, when $I_1 = 0$. Let us assume an equivalent 8-b precision over the output current. The upper bound of V_{S2} may be calculated by

$$I_{o\,\min} = \frac{I_R}{2^8} = I_R e^{-\frac{V_{S2\,\max}}{u_T}} \Rightarrow V_{S2\,\max} = u_T \ln(256). \quad (11)$$

We obtain, for $u_T = 26$ mV, $V_{S2\,\max} = 144$ mV, which is the voltage drop that I_1 has to generate in order to decrease I_o to its minimum value $I_{o\,\min}$. Neglecting the voltage drop produced by the small I_R, 250 mV can be taken as a practical lower limit for $V_{C\,\min} - V_{TN}$ to satisfy (8). Using V_C to control σ in (1), the maximum variation of conductances $g_{ds3,4}$ is

$$\beta(V_{DD} - V_{TN}) \geq g_{ds} \geq (V_{C\,\min} - V_{TN}). \quad (12)$$

The maximum swing of σ is thus given by

$$\frac{\sigma_{\max}}{\sigma_{\min}} = \sqrt{\frac{g_{ds\,\max}}{g_{ds\,\min}}} = \sqrt{\frac{V_{DD} - V_{TN}}{V_{C\,\min} - V_{TN}}} \quad (13)$$

which leads to a factor 4 for a 5 V supply and typical threshold voltages.

V. Limitations of Mismatch

Since the circuit is based on the symmetry of a current mirror, performance is limited by mismatches in the $M_1 - M_2$ and $M_3 - M_4$ pairs. Slight differences in β and V_{TN} of the pairs are considered to analyze the effects in circuit operation.

Taking into account these mismatches, the following output current expression for the current mirror at equilibrium ($I_1 = 0$) can be obtained

$$I_o = I_R(1 + \varepsilon_\beta) e^{\frac{\Delta V_{TN}}{n u_T}} e^{\frac{\Delta V_S}{u_T}} \quad (14)$$

where ε_β is the relative error of β in pair $M_1 - M_2$, $\Delta V_{TN} = V_{TN1} - V_{TN2}$, and ΔV_S is the error produced by the $M_3 - M_4$ mismatches

$$\Delta V_S = V_{S1} - V_{S2} = \frac{I_R}{g_{ds3}} - \frac{I_o}{g_{ds4}}. \quad (15)$$

If there is no mismatch, the output current is equal to the reference current, $I_o = I_R$.

Let us first consider the variation of the output current Io produced by mismatches of pair $M_1 - M_2$. As expressed by (14), I_o depends exponentially with ΔV_{TN}, and linearly with $\varepsilon\beta$, which suggests that mismatch in V_{TN} is more critical than mismatch in β.

In Fig. 2, output current relative error $(I_o - I_R)/I_R$ is shown as a function of ΔV_{TN} and ε_β. As a numerical example [9], for a typical process and a NMOS transistor of $W = L = 20$ μm we obtain $\Delta V_{TN} = 1.5$ mV and $\varepsilon_\beta = 0.12\%$. These values are displayed in the figure as a circle and a cross. As expected, the dominant error is produced by ΔV_{TN}. This explains that ΔV_{TN} is the principal agent of mismatch in current mirrors working at weak inversion [6]. In our circuit, the resistance of pair $M_3 - M_4$ reduces the error because of the negative feedback that ΔV_S introduces in (14). However, since resistance values are small, this reduction has almost no significance.

Even though mismatches cannot be eliminated, they can be kept small enough by means of an accurate technology and suitable layout techniques. Large transistors and proper layout design can reduce the error to a small percent, since the mismatch mainly depends on $\frac{1}{\sqrt{WL}}$ [9], [10].

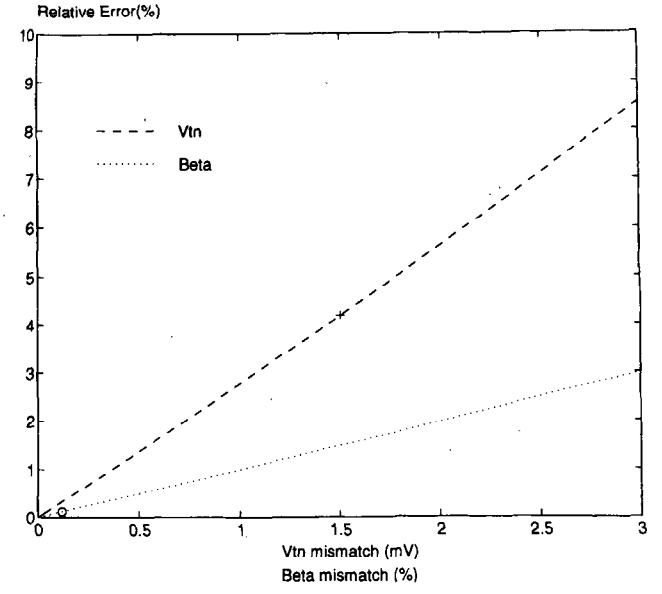

Fig. 2. Relative output current error as a function of β and V_{TN} mismatch of pair $M_1 - M_2$.

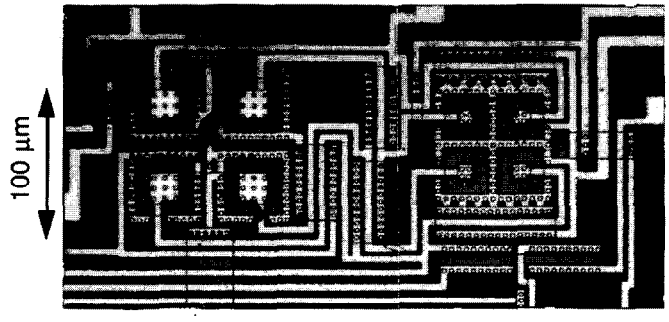

Fig. 3. Photograph of the circuit.

TABLE I
Transistor Sizes in a 3-μm SOI Technology

Transistor	W/L (µm/µm)
M_1, M_2	240/8
M_3, M_4	90/6
M_5	60/8

Another error source is mismatch in pair $M_3 - M_4$, that produces different output currents for $I_1 = 0$ when $g_{ds3,4}$ are different as (15) shows. However this error is made negligible in front of the other error sources by design. The way to minimize the effect of ΔV_S is to make the value of V_S small. Keeping g_{ds3} and g_{ds4} high, V_{S1} and V_{S2} will be small for $I_1 = 0$, and consequently ΔV_S. But g_{ds3} and g_{ds4} cannot be arbitrarily large because this leads to a high I_1 current to achieve at least a drop of 250 mV in V_{S2} for all the range of values of g_{ds4} that V_C can produce. To reduce the error under 1%,

$$e^{\frac{\Delta V_S}{u_T}} \leq 1.01 \Rightarrow \Delta V_S \leq 0.26 \text{ mV} \quad (16)$$

and considering a mismatch of 5% between g_{ds3} and g_{ds4}, $V_{S1,2} \leq$

TABLE II
RELATIVE ERROR TO GAUSSIAN SHAPE FOR THE RANGE OF V_C AT $I_R = 1\ \mu A$, 100 μA

$I_R(\mu A)$	1					100			
$V_c(V)$	5	4.05	3.10	2.15	1.20	5	4	3	2
$E_r(\%)$	0.19	0.18	0.21	0.36	1.05	1.64	1.64	1.88	1.96

5.2 mV. Notice that this small value is in accordance with assumptions in Section III. For $I_R = 1\ \mu A$, we have $g_{ds3,4} \geq 1.9 \cdot 10^{-4} \Omega^{-1}$. A I_1 high enough to produce a 250 mV drop in g_{ds4} is needed for all the margin of values of g_{ds4} (when V_C is used to control σ). For $\frac{g_{ds\,max}}{g_{ds\,max}} = 16$, $I_{1\,min} = 250\ mV \cdot g_{ds\,max} \cong 760\ \mu A$, the current that the squarer circuit has to be able to supply to the exponential circuit. Of course, if σ is not to be modified, a current $I_{1\,min} \cong 47.5\ \mu A$ is enough.

VI. Design and Layout Considerations

Because of the importance of matching and the σ the good matching characteristics that the Silicon-On-Insulator (SOI) MOS technology promises [11], the proposed circuit has been designed and fabricated in a 3-μm SOI technology. Table I shows the dimensions of transistors in this technology.

The test circuit was designed to work in weak inversion for $I_R = 1\ \mu A$. At $V_{IN} = 3$ V output current is to be zero for any selected σ value.

The pairs M_1, M_2 and M_3, M_4 have been designed with a common centroid geometry to reduce mismatching [12]. Also, the edgeless design (ring-shaped transistors) avoids the bird's beak effect that could produce undesirable influence on the transistors in weak inversion. Large dimensions of the transistors are needed to achieve the reference current of 1 μA in weak inversion, to reduce mismatches, and to build edgeless transistors.

The size of the circuit is about 0.07 mm^2 in a single-metal single-poly technology. For a double metal technology it could be easily reduced. Care has been taken to keep overall symmetry and also to avoid contacts or polysilicon wires in series with M_3, M_4, since parasitic resistances could modify the circuit behavior. Access to all the points of the circuit has been provided for this test cell, that is not necessary for normal operation.

VII. Experimental Results

The chip has been manufactured and tested. The layout photograph of the measured cell is shown in Fig. 3.

The measured threshold voltage of the NMOS transistors is 0.87 V. It has been experimentally determined that V_C can be varied from 5 to 1.2 V, for reasonable good Gaussian forms. It is approximately at $V_C = 1.2$ V when transistor $M4$ starts to leave the linear region and enter saturation. Then, condition (8) is not accomplished anymore. The ratio $\frac{\sigma_{max}}{\sigma_{min}}$ is thus 3.5. Measured conductances range from a value of $g_{ds4} = 3.58$ mA/V for $V_C = 5$ V to 1 mA/V for $V_C = 2$ V.

The output current relative error is about 2%, which indicates a good mirror matching. Measures have been done at $I_R = 1\ \mu A$. The inversion coefficient (IC $= I_D/2n\beta u_T^2$, that indicates the border between weak and strong inversion), is 0.46, a value between the weak and moderate inversion regions as desired in order to maximize current while still being in weak inversion. Curves of less than 0.2% of relative error to a Gaussian shape have been obtained. This error is obtained calculating the mean square error between the experimentally measured points and that corresponding to a pure Gaussian curve, and then dividing by the current dynamics, namely the reference current. Table II shows the errors for different V_C values.

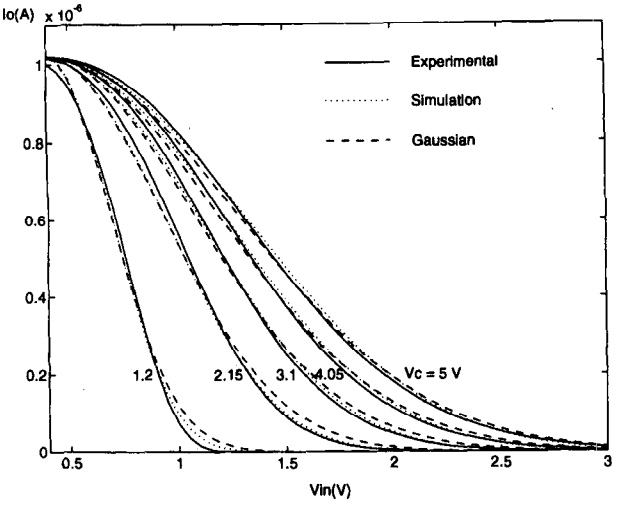

Fig. 4. Output current for $I_R = 1\ \mu A$ and $V_C = 1.2$, 2.15, 3.10, 4.05, and 5 V.

Fig. 4 depicts the experimentally obtained curves compared to half Gaussian functions. The curves have also been compared with simulated Cseverny-Oguey continuous model for weak/strong inversion [13] and fit very well. The effective threshold voltage of the PMOS transistor is 0.4 V and the maximum of I_o is 1.02 μA. This error of 2% is a very low value for a mirror in weak inversion, as discussed in Section V. The different maximum value of the output current for $V_C = 1.2$ V is produced also by mismatches, that have worse effects for the smaller g_{ds}.

To characterize the speed performance of this nonlinear circuit, the settling time (10 to 90% of the output current for a small-signal step function) has been measured. Simulations show $t_{ss} = 0.1\ \mu s$. The measured settling time is $t_{sm} = 1.0\ \mu s$. The difference can be found mainly because of the pad capacitance, since there is no current buffer provided in the prototype cell.

These experimental results are referred to measurements on three samples of the same process, leading to close results. While the output current relative error is random, due to mismatch, the shape error is systematic, probably due to the difference of the exponential and square models of the transistors. Because of this, measurements in other batches would be of interest in order to characterize precisely random errors.

VIII. Strong Inversion Operation

The circuit has also been tested in strong inversion operation ($I_R = 100\ \mu A$), which has the advantage of faster operation, at the price of some shape degradation as Table II shows. V_c is restricted to a lower bound of 2 V.

The analytical expression for the output current as a function of I_1 of the exponential circuit in strong inversion results

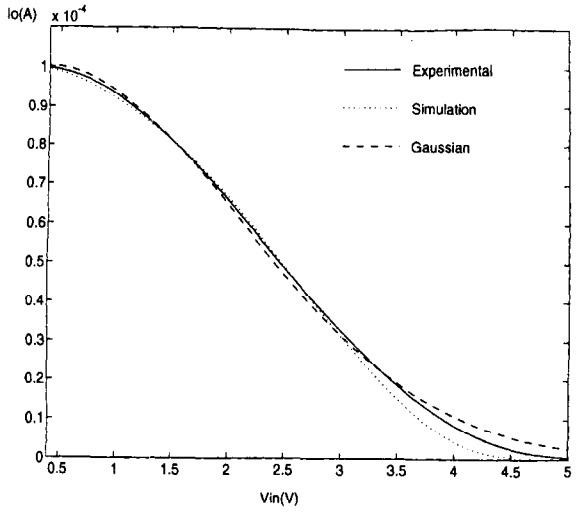

Fig. 5. Output current for strong inversion operation.

$$I_o = g_{\mathrm{ds4}}(V_{G2} - V_{\mathrm{TN2}}) - I_1 + \frac{g_{\mathrm{ds4}}^2}{\beta} \times \left[1 - \sqrt{1 + \frac{2\beta}{g_{\mathrm{ds4}}}\left(V_{G2} - V_{\mathrm{TN2}} - \frac{I_1}{g_{\mathrm{ds4}}}\right)}\right]. \quad (17)$$

Substitution of I_1 in (9) results in the transfer function of the Gaussian circuit. Even though the analytical function is not Gaussian, it is a σ the od approximation, as Fig. 5 shows, where the simulated, experimental and half Gaussian curves are plotted for $I_R = 100\ \mu$A and $V_c = 5$ V. Now the input voltage swing has to go to 5 V in order to decrease to zero the output current, since $\frac{g_{m3}}{I_R}$ is smaller for strong inversion (and thus the decreasing slope of the exponential is smaller too). Simulated and measured settling times are $t_{\mathrm{ss}} = 20$ and $t_{\mathrm{sm}} = 200$ ns, respectively.

IX. Conclusion

A simple 5-transistor circuit that implements a Gaussian function has been proposed. The input voltage is squared and converted to current, and a current mirror in weak inversion then performs the negative exponential function. Adding an offset to V_{IN} alloud to shift the Gaussian center. The input voltage may be easily substituted by an input current through the use of a squarer circuit.

One limitation of the circuit is the mismatch of the transistors in weak inversion. Because of this, design constraints have to be taken into account and a careful layout design is to be done.

A test circuit has been fabricated and tested in a 3 μm SOI CMOS technology. The experimental results show a very good approximation of true Gaussian functions. At a cost of some shape accuracy (systematic errors), the circuit can work also in the strong inversion mode, with the associated speed benefits. Furthermore, random errors due to mismatch are also reduced in strong inversion. The proposed circuit can be readily integrated as an analog Gaussian transfer function circuit in a neural classifier IC or other applications.

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