ISCAS'2001 proceedings - International Symposium on Circuits and Systems, Sydney (Australia), 6-9 May 2001, pp. III 173-176

EMBEDDED FUZZY CONTROL FOR AUTOMATIC CHANNEL EQUALIZATION AFTER DIGITAL TRANSMISSIONS

Carlos Dualibe[1,2], Paul Jespers[2] and Michel Verleysen[2,**]

[1]Laboratorio de Microelectrónica, Facultad de Ingeniería, Universidad Católica de Córdoba, Córdoba, Argentina
[2]Laboratoire de Microélectronique, DICÉ, FSA, Université catholique de Louvain, Louvain-la-Neuve, Belgium

ABSTRACT: A straightforward technique for automatic adaptation of channels equalizers after digital data transmission is presented. Inter-Symbol Interference (ISI) at the received signal is identified by scanning the input stream over time at the data clock frequency. The resulting 2D-figure is compared against an ideal opened Eye Pattern encoded into a two-input one-output analogue Fuzzy Inference System. Any deviation from the reference eye results in an error-signal used to properly locate the symmetric zeros of an analogue amplitude-equalizer biquad gm-c filter intended for the inversion of the channel transfer function. The adaptation can work on-line during transmission and no reference signal is required. The presented methodology was validated by simulations for cable equalization wherein the controller as well as the filter were modeled with their actual measured features drawn from a fabricated CMOS prototype. The system shows self-adapting capabilities for diverse cable length settings and the ISI is removed in all cases.

I. INTRODUCTION

In digital transmission, channel dispersion causes interference between successive symbols making difficult a reliable reception of signals. Therefore equalization is needed [1]. The extend to which the equalizer is able to match the inverse of the channel frequency response determines the extend to which the ISI is eliminated and the Bit-Error-Rate (BER) improved.

Automatic adjustment of the equalizer parameters provides flexibility and robustness whenever the channel characteristics are time-variant and/or they depend on variables inherent to the communication system that may change from one setup to another (i.e.: the cable length in wired transmissions). Well-known methods [1] based on the gradient of an error criterion perform such adjustment but they need a reference signal, turning the implementation worrisome.

In [2], a self-adaptive technique based on Lissajous figures obtained after sampling the signal is proposed. However, the sampling clock phase must be carefully controlled so as to keep the resulting figure close to the reference pattern. In addition, the sampling frequency needs to be at least twice the rate of the transmitted data, compromising the power consumption of the circuits that perform the adaptation.

In this work we present a knowledge-based approach for adaptive equalization, which does not require a training-data set. After the equalizer, the stream is swept at the baud-rate frequency and converted into a figure that should resemble the Eye-Pattern if well equalized. Otherwise, the distorted eye generates an error-signal that is used to adapt the parameters of the equalizing filter in closed loop. Since the adjusting procedure can easily be described through common-sense rules, Fuzzy Logic becomes a smart tool to synthesize the non-lineal adapting servo-controller.

II. SYSTEM DESCRIPTION

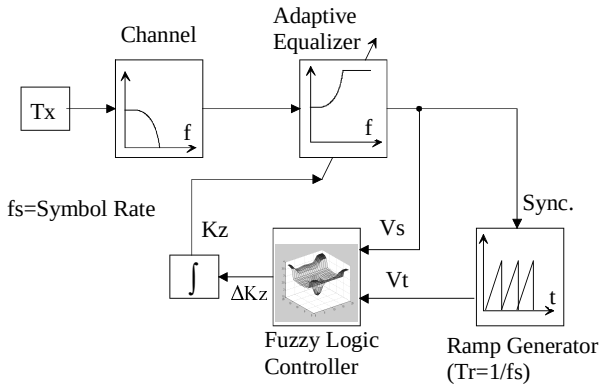


Fig. 1: Adaptive equalizing system.

Figure 1 shows the block diagram of the adaptive equalization system during the transmission of data symbols at fs bauds. The channel is assumed to be a CAT5 unshielded twisted-pair cable, with a loss characteristic given by:

$$\left|C(f)\right|_{dB} = -10^{-2} L \left(2\sqrt{f} + 0.023f + 0.05/\sqrt{f}\right), \qquad (1)$$

where the cable length, L, and the frequency, f, are expressed in meters and Mhz, respectively.

The first block at the receiver stage is an adaptive high-frequency boost equalizing filter that will be described later. It inputs the equalized signal Vs in the fuzzy controller. The second input of the controller, Vt, is fed from a resetable free-running ramp-oscillator whose period Tr equals the inverse of the symbol rate fs. It furnishes a true time-base to the fuzzy system to explore the signal along time, like in any oscilloscope. Synchronization is achieved by detecting every rising edge of the signal after the equalizer. Further details on the ramp generator are omitted for briefness.

As a function of the actual values of Vs and Vt, the fuzzy controller bears continuously the adaptation step ΔKz for the

* M. Verleysen is a research associate of the Belgian FNRS.
* This work was financed by the Belgian FNRS.

adjustable parameter Kz resulting after integration. On the other hand, the magnitude of two symmetrical real zeros belonging to the transfer function of the equalizer is proportional to Kz. Since both zeros have opposite signs, they boost-up the magnitude of the incoming signal without phase-shift. In short, the smaller Kz the bigger is the high-frequency boost.

With regards to the fuzzy system, each input variable is fuzzified by means of five labels: {NB, N, Z, P, PB}, as shown in the block diagram of figure 2. Consequently, the plane [Vs x Vt] is partitioned in 25 clusters, each one corresponding to one rule. Considering that the goal is to keep the figure described by the set of the successive points (Vs(t),Vt(t)) as close as possible of an opened eye, the strategy for the adaptation may be easily formulated in terms of fuzzy statements. For example, if the signal is poorly equalized, the 2D-figure will concentrate at the center of the input plane as a consequence of the severe distortion remaining. It turns out that the central rule should look like: *"if* Vs *is* Z *and* Vt *is* Z *then* ΔKz must *be* NEGATIVE". After executing this rule, the zeros of the equalizer will move towards lower frequencies attempting to open the actual eye by increasing the amount of boosting. Figure 3 gives a graphical interpretation of the control policy needed for the adaptation task.

II-A FUZZY LOGIC CONTROLLER

Because of the good trade-off between simplicity and accuracy, a zero-order Sugeno architecture (consequents are singletons) was chosen [3,4]. Two five-labels Fuzzy Partition Circuits [5,6] deliver currents at their outputs that represent the fuzzified values of inputs Vs, Vt, making them available to the 25 two-inputs MINIMUM circuits to set up the rules-base. From the T-Norms, the firing degrees of the rules are taken care by currents I1-I25 towards the Defuzzifier. At this stage, each current Ii is replicated (n+1) times via unit-gain mirrors, where n stands for the resolution of the singleton discrete-value αi of the consequents. These are codified according to the state of the switches Cn-1…C0. Finally, a shared current-mode digital to analogue D/A converter, performing the weighting operation,

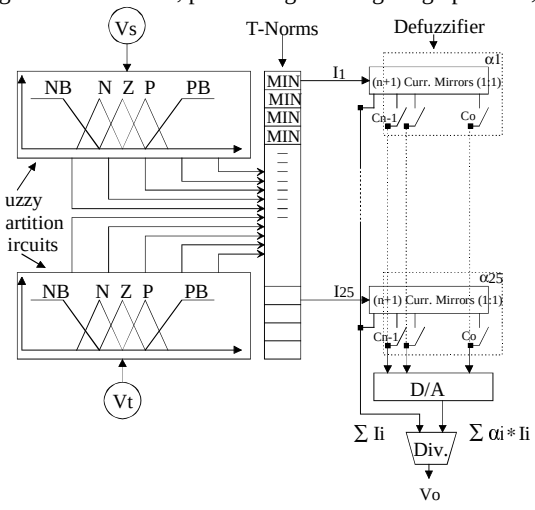


Fig. 2: Block diagram of the fuzzy controller.

together with an analogue divider takes care of the computation of the center-of-gravity. The defuzzified output value is:

$$Vo = kd \frac{\sum_1^{25} \alpha i * Ii}{\sum_1^{25} Ii}, \qquad (2)$$

where kd is a constant inherent to the divider itself.

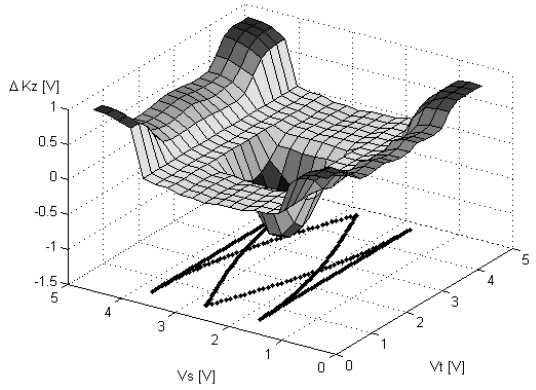


Fig. 3: Measured output of the controller related to the eye pattern.

Fuzzy Partition Circuit: figure 4 shows the circuit generating all fuzzy labels needed for each input-variable. It is composed by four differential pairs (Ma) interconnected by current mirrors (Mb and Mc) Voltages Vk1<Vk2<Vk3<Vk4 define the 25%-overlapping crossover points between contiguous membership functions. In this version, the fixed size of Ma accounts for the MF slopes but the architecture allows easily the implementation of electrically tunable slopes by using triode transconductors as in [3]. Thus, the five current labels {INB… IPB} are spawned when Vin is swept along its range. While keeping similar idea, the VLSI-oriented scheme in [6] needs higher power supplies (i.e.: 8V) and slopes tuning capability is not affordable, whereas [5] would require extra voltage-to-current input converters if intended for our application.

The current consumption depends on the actual value of the input Vin. Assuming the later to be a uniform distributed random

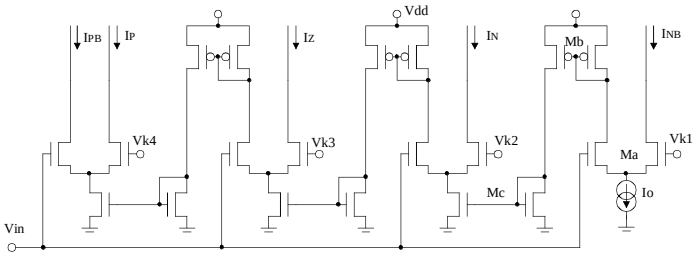


Fig. 4: Compact Fuzzy Partition circuit schematic.

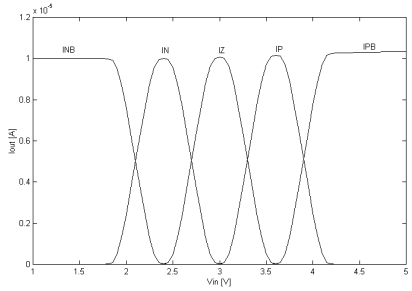


Fig. 5: SPICE simulation of the Fuzzy Partition circuit for Io=10μA.

variable, the mean current needed is equal to 4Io. This represents an improvement with respect to the use of individual fuzzifiers per label [3,4] where the total consumption is constant and rises to 10Io for the same number of membership functions (MF) per input. However, larger delays may be expected due to the cascade interconnections. Random mismatches and noise are minimized using a relative large active area (WxL) for the transistors [4].

Minimum T-Norm: the circuit illustrated in figure 6a makes a comparison between I1 and I2, which are assumed to be mirrors of the two membership functions outputs in a rule. The smaller current will be mirrored to the other branch turning its transistor Mn unsaturated. The minimum is then sourced at the output through transistors Mp5, Mp6. This circuit can also be extended to a multiple-input operator by adding branches and stacked transistors Mp per branch, but it has $O(N^2)$ complexity and the maximum number of inputs is limited by the value of Vdd. Nevertheless, for small fan-in, the simplicity justifies its use.

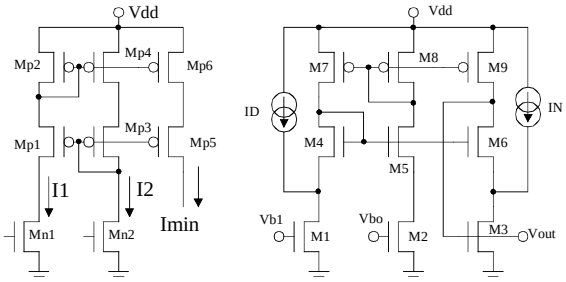


Fig. 6: a) Minimum circuit. b) Transresistance divider.

Defuzzifier: for each rule, a discrete output-singleton αi smaller than 1 is given by: $\alpha i = (Cn\text{-}1)_i\ 2^{-1} + \ldots\ldots + (C0)_i\ 2^{-n}$, for i from 1 to 25 and coefficients $(Cn\text{-}1)_i \ldots\ldots (C0)_i$ taking binary values. At figure 2, the outputs of the n current mirrors related to each singleton are column-wise summed and then weighted in a current-mode D/A converter built by n binary-scaled current mirrors. In view of the linear operations implicated in the D/A conversion, a single weighting block can be shared by all the rules if the summation order is exchanged. In [3] is demonstrated that this solution gives rise to: savings in area, speed improvements and higher accuracy, if compared to circuits with a local D/A per consequent.

Divider: in figure 6b, with equally sized transistors at each row of the circuit, the division is actually performed by transistors M1, M2 and M3 at the bottom layer, all of them being constrained to operate in the triode region. The drain to source voltage drops Vds of those transistors are matched thanks to the common-gate connected transistors M4, M5, and M6, conveying the same current owing to the upper mirrors built by M7, M8, and M9. While Vb1 and Vbo are fixed bias voltages, the gate-voltage Vout of transistor M3 self-adjusts until the drain currents of M6 and M9 get alike. Hence, the following relation holds [7]:

$$Vo = (Vout - Vbo) = (Vb1 - Vbo)\frac{IN}{ID}. \qquad (3)$$

II-B ADAPTIVE AMPLITUDE-EQUALIZER

A fully differential version of the circuit at figure 7 was used for the equalizer. It is a biquad gm-c lowpass filter bringing in amplitude boosting at high frequencies [8]. Adaptability is accomplished by fixing gm1, gm3, gm5 to the maximum value gm_{max} and allowing gm2=gm4 to be tunable from 0 to gm_{max}. Without loading the output node, the transfer function becomes:

$$\frac{Vout}{Vin} = \frac{-(gm_{max}/gm4)s^2 + (gm_{max}{}^2 / C1C2)}{s^2 + \left(gm_{max} / C2\right)s + (gm_{max}{}^2 / C1C2)}. \qquad (4)$$

The zeros of the adaptive filter are thus given by:

$$z1, z2 = \pm Kz\left(gm_{max} / \sqrt{C1C2}\right), \quad \text{with} \quad Kz = \sqrt{gm4 / gm_{max}}\ . \qquad (5)$$

Notice that the poles of (4) (normally complex) remain unchanged while Kz is adapted. However, their positions define the maximum amount of boosting attainable for each value of Kz.

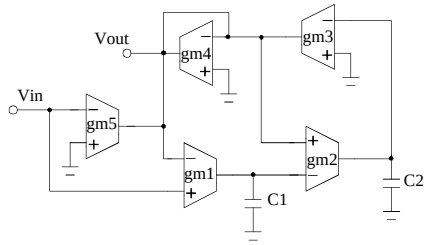


Fig. 7: Single-ended amplitude-equalizer biquad gm-c filter.

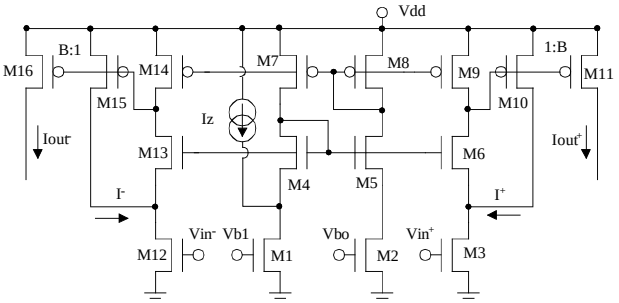


Fig. 8: Proposed pseudo-differential transconductor schematic.

Transconductor gm: based on the circuit of the divider [7] a novel pseudo-differential linear-transconductor is presented in figure 8. In contrast to figure 6b, the gate-voltage of transistor M3 is released to become the input Vin^+ whereas the current I^+ (former IN) through M10 is now controlled by the negative feedback loop performed via the later mentioned transistor. The up-scaled mirror M11 delivers $Iout^+ = B\ I^+$ at the output. Similarly, transistors M12 to M16 set up the complementary branch of the transconductor for the input Vin^-. Provided that M1, M2, M3 and M12 are all being biased in ohmic region, equation (3) still holds. There from we can write:

$$Iout^+ - Iout^- = \frac{B\ Iz}{(Vb1 - Vbo)}\ (Vin^+ - Vin^-) = gm\,\Delta Vin\,. \qquad (6)$$

Accordingly to (6), the transconductance is fully electrically controllable by Iz and (Vb1-Vbo). Considering that there is no technological parameter affecting its value (i.e.: μCox), improvements regarding the matching between the different gm-cells of the filter should be expected. Furthermore, as long as the above electrical variables controlling gm are being supplied by reference bias circuits, stability against temperature and power supply variations are guaranteed.

III. RESULTS AND CONCLUSIONS

Towards the future implementation of the whole system, a first prototype consisting of the controller and the equalizer was fabricated and tested in a CMOS-2.4μ process for a single 5V-supply. Typical parameters values are Vtn $= |Vtp| = 0.85V$, $\mu_n = 580cm^2/Vs$, $\mu_p = 230cm^2/Vs$ and $Cox = 0.855fF/\mu^2$.

At the fuzzy controller, the 'logical one' Io was set to 10μA, trade-off between low-power, speed and noise immunity. Relevant transistors sizes for the fuzzifiers given in [μm/μm] resulted in: $(W/L)_{Ma}=25/5$, $(W/L)_{Mb}=24/5$, $(W/L)_{Mc}=70/5$. The crossover thresholds Vk1 to Vk4 were set to 2.1V, 2.7V, 3.3V and 3.9V respectively. At the MIN circuits: $(W/L)_{Mn}=15/5$ and $(W/L)_{Mp}=20/5$. Singletons αi and the weighting D/A are built by cascoded transistors with (W/L)=15/5. Aiming at the divider 0<IN,ID<40μA and 0<Vo<2V the aspect-ratio for its transistors were found to be: $(W/L)_{M1\text{-}M3}= 16/6$, $(W/L)_{M4\text{-}M6}=20/5$ and $(W/L)_{M7\text{-}M9}=30/5$. The global performances of this controller are summarized as follows: 5-bits of resolution, a RMSE of 56mV (2.8%) between target and measured output surfaces, power consumption of 4.4mW, die silicon area of 3.1 mm^2 and 310 ns of total delay for CLoad ≈20pF.

The design parameters for the equalizing filter were chosen to achieve a 10Mhz band pass. Consequently, gm_{max} was set to 210μS for C1=4pF and C2=2pF. The transient damping ratio of the filter, related to (C2/C1), was fixed to 0.707 for a minimum overshoot and fast settling-time. In the transconductors, Vb1=2V and Vbo=1.5V allow ±1V of output swing centered at the analog reference Vagnd= 2.5V. Low phase-error was targeted by adopting suitable transistors geometry that minimize stray capacitances effects, namely: B=6, $(W/L)_{M1\text{-}3,12}=15/15$, $(W/L)_{M4\text{-}6,13}=20/6$ and $(W/L)_{M7\text{-}10,14}=70/5$. Zeros placement is achieved by changing Iz at gm4, gm2 up to 35μA while fixing the same to 35μA in the others transconductors. A boosting-peak of 37dB was reached at 7 Mhz for Iz=7μA as is shown in figure 9a. It should be noticed that a second pair of poles appears at the peak frequencies due to the capacitive nature of the equalizer output load, which has not been considered in (4) for clarity. This filter dissipates 22.6mW and it demands 5.3 mm^2 of surface.

Due to the simplicity and availability of cable models, wired-transmission was chosen to validate the idea by simulations. Nevertheless, the above measured features for the filter and the controller were included for their models. Three different lengths of cable were adopted for the transmission of a random binary sequence at 5Mb/s, this rate being compatible with the speed of the controller. To introduce a considerable ISI at the involved frequency, L was set to 120m, 240m and 360m. In figure 10a the transmitted, received and equalized signals for the worst case (L=360m) are plotted. Figure 10b shows the evolution of Kz throughout adaptation for the mentioned cable settings. Notice the asymptotic convergence in both directions. Moreover, in contrast to the decision-directed equalizing system presented in [1], simulations confirm that even for noisy-channels self-adaptation is attained since the noise is filtered out by the area tolerance foreseen at the control surface in figure 3. In addition, since there is no need to update Kz in a continuous way (i.e.: one update every ten bits, for instance), adaptation at higher baud-rates is also feasible by sampling signals Vs and Vt, at a sampling frequency in agreement with the controller speed, and replacing the integrator in figure 1 by a discrete-time one.

The presented technique permits to identify patterns by inspection of signals over time. Its appliance exceeds the topic of channel equalization. From an explicit 2D signal representation, fuzzy logic allows to infer meaningful assertions that can be used for adaptation, detection, testing, etc.

IV. REFERENCES

[1] Widrow B. & Stearns S., "Adaptive Signal Processing", Chapter 10, Prentice-Hall, 1985.

[2] Mager K., "Equalizer adaptation with a geometrical criterion and fuzzy logic", *IEEE Trans. on Consumer Electronics*, Vol 40, Nº 3, pp. 372-376, 1994.

[3] Dualibe C., Jespers P. & Verleysen M., "A 5.26 Mflips programmable analogue fuzzy logic controller in a standard CMOS 2.4μ Technology", *IEEE ISCAS'2000*, Vol. 5, pp. 387-380, Geneva, Switzerland, May 28-31, 2000.

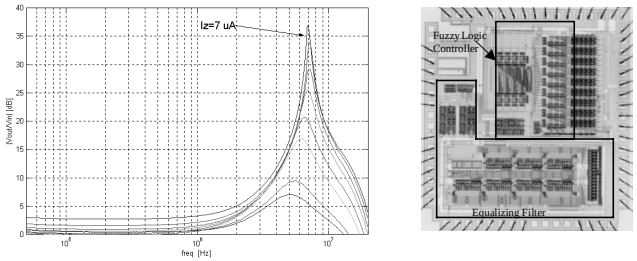
[4] Vidal-Verdu F. *et al*, in "Fuzzy hardware architectures and applications", Chapter 16, *Kluwer Academic Publishers*, 1998.

[5] Conti M. *et al*, "A current-mode circuit for fuzzy partition membership functions", *IEEE ISCAS'99*, pp. V-391-394, Orlando, USA, 1999.

[6] Wilamowsky B. *et al*., "VLSI implementation of a universal fuzzy controller", *Artificial Neural Networks in Engineering '96*, St. Louis, Missouri, USA, 1996.

[7] Dualibe C. *et al*., "Two-quadrant CMOS analogue divider", *Electronics Letters*, June 1998, pp. 1164 -1165.

[8] Wyszynski A. & Schaumann R., - "A current-mode biquadratic amplitude equalizer" , *Analog Integrated Circuits and Signal Processing"*, Kluwer A. P., Nº 4, pp. 161-166, 1993.



a) b)

Fig.9: a) Equalizer measured response. Iz from 7μA. b) Chip photograph.

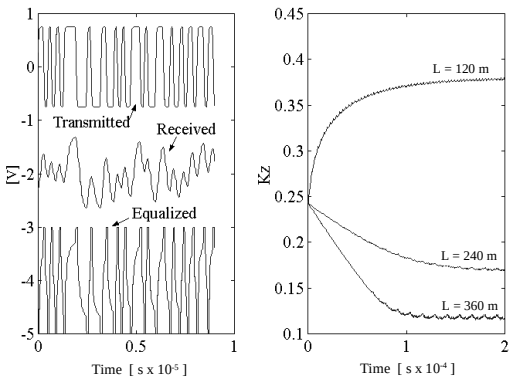


Fig. 10: a) Transmitted, received and equalized signals for L=360m. b) Kz convergence for several cable lengths.