Ultra-low-power computing

Keywords : Microcontroller; Memory; Flip-flops; Adaptive circuits; 28 nm CMOS; IoT.

David Bol, François Stas, Thomas Haine, Ludovic Moreau, Guerric de Streel, Charlotte Frenkel, Khoi Nguyen, Denis Flandre, Jean-Didier Legat

Abstract – For a massive yet sustainable Internet-of-Things, ultra-low-power computing is required without compromising the data processing and storage performances. In the electronic circuits and systems (ECS) group, we pursue new solutions to this challenge with ultra-low-voltage (ULV) digital integrated circuit (IC) and system-on-chip (SoC) design. Latest results feature the evaluation of 28 nm FDSOI CMOS technology for ULV digital circuits and SRAM memories, adaptive back biasing techniques to compensate process and temperature variations and low-energy pulsed flip-flops in collaboration with CEA-LETI.

The connection of our daily life's objects to the cloud according to the Internet-of-Things (IoT) vision is about to revolutionize the way we live. To enable this revolution, a massive deployment of sensor nodes is required with predictions announcing up to trillions of these nodes. Such a massive deployment is not environmentally and economically sustainable with current technologies. Some of the pitfalls lay in the computing capability of IoT nodes whose power consumption needs to be optimized in order to operate on ambient energy harvesting without compromising the data processing and storage performances [1]. Indeed, key applications using audio/vision sensing or brain-machine interfaces (Fig. 1) require the on-chip extraction of the important information from the sensed data to limit the worldwide electrical power consumption of the ICT infrastructure (datacenters and basestations) due to machine-to-machine (M2M) wireless data traffic. Therefore, the IoT nodes need to be able to perform compression, feature extraction or classification within their ultra-low power budget which is not possible with current low-power microcontroller (MCU) technologies because of their limited energy efficiency.

The energy cost of software execution can be avoided by adding key dedicated hardware accelerators to the MCU [2]. ULV operation can further improve the energy efficiency of the HW accelerators. Nevertheless, ULV operation comes at the expense of a degraded speed ultimately below the MHz deep in the subthreshold regime. To overcome the performance degradation, we rely on nanometer CMOS technologies [1] with high-speed design techniques for both logic and memories in 28 nm FDSOI CMOS including:

- the optimization of SRAM memories with respect to their dynamic and statistical stability [3],
- the generation of adaptive back biasing voltages to compensate process and temperature effects on the speed of logic and SRAM memories [4],
- the design of ultra-dense low-clock load pulsed flip-flops in collaboration with CEA-Leti (Grenoble, France) [5] and true-single-phase flip-flops.

Some of these techniques have been used to design a 0.4V ultra-low-power SRAM memory whose prototype codenamed MEMPHIS is under test (Fig. 2). Its dual-voltage divided-wordline architecture featuring the UCL patented ULP SRAM bitcell with adaptive back biasing and low-energy skewed sense amplifiers should allow 100-MHz operation with record access energy. Next research will focus on the design of a high-performance ULV MCU-based computing platform in 28 nm FDSOI CMOS.

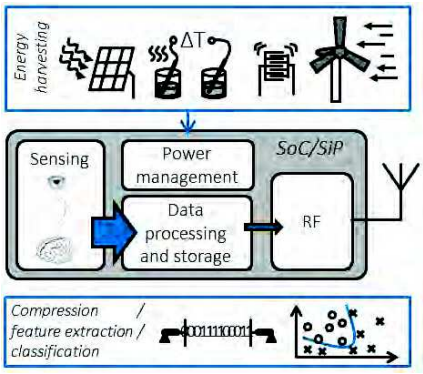

Figure 1: Data processing and storage in IoT nodes need to perform compression, feature extraction of classification at an ultra-low power.

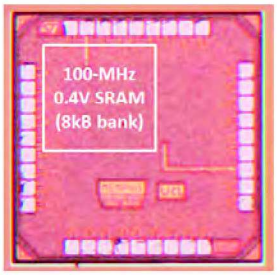

Figure 2: Die microphotograph of the MEMPHIS prototype in 28 nm FDSOI CMOS.

References

[1] D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective," in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 49-50, 2015.

[2] L. Moreau, "Conception d'une Plateforme SoC de Traitement de Signaux Numériques à Ultra-Basse Consommation pour la Détection des Crises d'Epilepsie", Master Thesis, UCL, 2014.

[3] A. Elthakeb, T. Haine, D. Flandre, Y. Ismail, H. Abd Elhamid and D. Bol, "Analysis and Optimization for Dynamic Read Stability in 28 nm SRAM Bitcells", in Proc. IEEE Int Conf. Circuits and Systems, pp. 1414-1417, 2015.

[4] Q.-K. Nguyen, "Adaptive Back Biasing System for Compensation of PVT Effects on SRAM Dynamic Stability", Master Thesis, UCL, 2015.

[5] S. Bernard, M. Belleville, A. Valentian, J.-D. Legat and D. Bol, "Experimental Analysis of Flip-Flops Minimum Operating Voltage in 28 nm FDSOI and the Impact of Back Bias and Temperature", in Proc. International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), 2014.

Ultra-low-power imaging

Keywords : CMOS image sensor; Digital pixel sensor; Time-based readout; IoT.

David Bol, Thomas Haine, François Stas, Denis Flandre

Abstract – For a massive yet sustainable Internet-of-Things, ultra-low-power sensing is required without compromising quality of the signal acquisition. CMOS imagers are one of the most difficult sensing devices to implement at ultra-low power due to the numerous pixels required. In the electronic circuits and systems (ECS) group, we pursue new solutions to this challenge with ultra-low-voltage (ULV) CMOS imager design. Latest results include a 0.5V imager successfully prototyped within a 3-mm^2 solar-powered video analysis System-on-Chip (SoC) co-denamed SunPixer.

The connection of our daily life's objects to the cloud according to the Internet-of-Things (IoT) vision is about to revolutionize the way we live. To enable this revolution, a massive deployment of sensor nodes is required with predictions announcing up to trillions of these nodes. Such a massive deployment is not environmentally and economically sustainable with current technologies. Some of the pitfalls lay in the sensing capability of IoT nodes whose power consumption needs to be optimized in order to operate on ambient energy harvesting while preserving sufficient acquisition quality for effective extraction of the meaningful information from the sensed data [1]. This is particularly challenging for multi-dimensional sensing devices such as CMOS image sensors for vision applications.

The first research we made in this area was the design of a 0.5V CMOS imager in 65nm CMOS for integration within the SunPixer SoC (Fig. 1), which is a 3-mm^2 solar-powered video analysis SoC. It features an inductorless indoor/outdoor energy-harvesting power management unit, a 50-MHz 32-bit microcontroller (MCU) for on-chip image/video analysis and a 128 $\times$ 128-pixel imager prototype. The imager uses digital pixel sensors (DPS) for time-based readout at 0.5V to reach record energy efficiency of 17pJ/frame.pixel. However, as the high transistor variability (mismatch) at ULV significantly degrades the image quality, we had to introduce key techniques to restore a 42dB dynamic range with two of them under patent application: wide-range adaptive body biasing [2], low-R_{ON} gating of the 2-transistor in-pixel comparator [3] and robust digital readout performing delta-reset sampling (Fig. 2). Extrapolation of these results to a VGA image resolution would give a power consumption of only 80μW at 15 frames per second, which corresponds to a power reduction of at least 400 $\times$ compared to the commercial state-of-the-art. SoC integration further allows avoiding the prohibitive energy cost of image transfer from a CMOS imager to an MCU chip through the external 1.8-2.5V I/O bus.

The second research in this field aims at transferring this design on a low-cost 0.18μm CMOS process with a VGA image resolution. A prototype CMOS imager codenamed CAMEL (Fig. 3) was designed in collaboration with nSilition (LLN, Belgium). The chip is currently under prototyping.

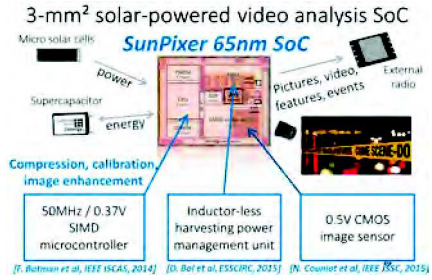

Figure 1: SunPixer SoC in 65nm CMOS.

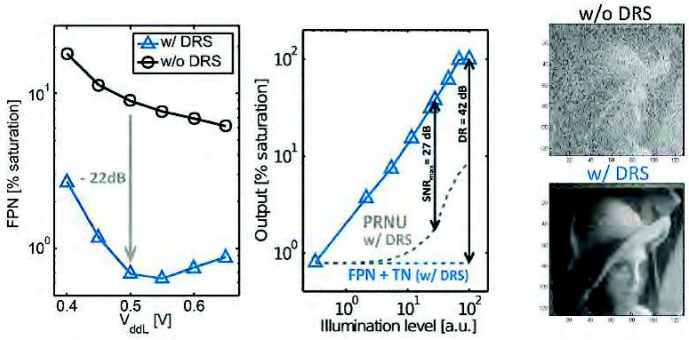

Figure 2: Image quality results of the CMOS imager inside the SunPixer SoC.

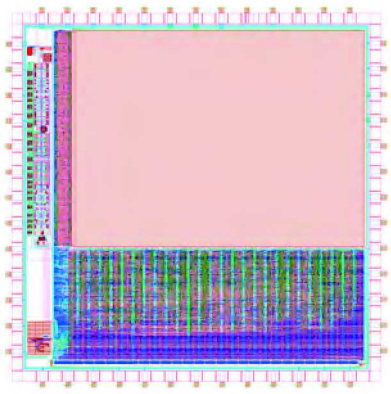

Figure 3: Layout of the CAMEL imager under prototyping in 0.18μm CMOS.

References

[1] D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective" in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 49-50, 2015

[2] N. Couniot, G. de Streel, F. Botman, A. Kuti Lusala, D. Flandre and D. Bol, "A 65 nm 0.5 V DPS CMOS Image Sensor With 17 pJ/Frame.Pixel and 42 dB Dynamic Range for Ultra-Low-Power SoCs", in IEEE J. Solid State Circuits, vol. 50, no. 12, pp. 2419-2430, 2015.

[3] D. Bol and N. Couniot, "Image sensor", Europe Patent WO2015/110647, Jan. 24, 2014.

[4] D. Bol and N. Couniot, "Image sensor", Europe Patent WO2015/110646, Jan. 24, 2014.

Ultra-low power management and voltage regulation

Keywords : Energy harvesting; Switched-capacitor converters; Linear regulators; IoT.

David Bol, Pierre-Antoine Haddad, Khoi Nguyen, Guerric de Streel, Denis Flandre

Abstract – For a massive yet sustainable Internet-of-Things, ultra-low power management and voltage regulation are required to operate the nodes on ambient energy harvesting (EH) while delivering the required supply voltages to the sensing, computing and communication blocks. Latest related results obtained in the electronic circuits and systems (ECS) group include indoor/outdoor solar EH power management units licensed to and industrialized by e-peas semiconductors, RF-harvesting rectifiers, a reconfigurable switched-capacitor converter with a wide load power range in collaboration with ST Microelectronics, a voltage reference with the record 0.2V minimum and an ultra-low-quiescent current linear regulator with most of them included in a 3-mm^2 solar-powered video analysis System-on-Chip (SoC) codenamed SunPixer.

The connection of our daily life's objects to the cloud according to the Internet-of-Things (IoT) vision is about to revolutionize the way we live. To enable this revolution, a massive deployment of sensor nodes is required with predictions announcing up to trillions of these nodes. Such a massive deployment is not environmentally and economically sustainable with current battery-operated technologies. Indeed, to avoid the cost and the ecotoxicity of battery replacement, the IoT nodes need to operate by harvesting the ambient energy present in various forms: solar, thermoelectric, piezoelectric or electromagnetic RF [1].

Commercial energy-harvesting power management units (EH-PMU) fail to meet the demand for autonomous startup (cold start) when the energy storage is empty. A first EH-PMU for micro PV cells based on an inductive boost converter was designed with the specific target to provide robust cold start functionality and maximum-power-point tracking while allowing to supply a wide range of off-the-shelf sensing, computing and communication components. It was licensed to e-peas semiconductors spin-off which successfully prototyped and industrialized it under its AEM product line [2]. A second EH-PMU for micro PV cells was designed based on a single bidirectional multi-gain/multi-mode switched-capacitor converter for direct harvester/load connection and on-chip integration in 65nm CMOS without external inductor [3]. It was integrated within the SunPixer SoC (Fig. 1), which is a 3-mm^2 solar-powered video analysis SoC.

RF electromagnetic energy from wireless communication signals is another interesting energy source in densely populated zones. Front-end interfaces for RF EH-PMU must include an AC/DC converter typically implemented by a rectifier. An optimization method for rectifiers has been developed and validated on the design of a 13.56-MHz rectifiers [4] using UCL-patented ULP diodes on simple Greinacher architecture and with more complex architectures (cross-coupled, differential drive).

From the system supply voltage generated by the EH-PMU, the specific ultra-low-voltage (ULV) load supplies need to be generated and regulated with circuits including:

- the first voltage reference circuit starting at a 0.2-V supply voltage that was successfully prototyped in 65nm CMOS [5],
- an ultra-low-quiescient current linear regulator with a high-dropout (HDO) architecture that was successfully prototyped in 65nm CMOS [6],
- a multi-mode switched-cap DC/DC converter for a wide output power range that was successfully prototyped in 28nm FDSOI CMOS [7] in collaboration with ST Micro (Crolles, France).

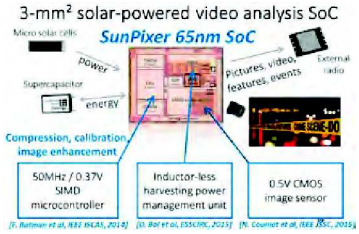

Figure 1: SunPixer SoC in 65nm CMOS.

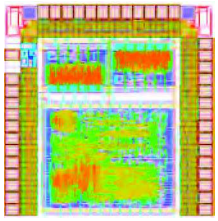

Figure 2: Layout of ADELE LDO regulator in 0.13μm CMOS.

Next research in this field is focused on multi-source EH-PMUs and all-synthesized PMUs using only digital standard cells. A prototype all-synthesized low-dropout (LDO) regulator codenamed ADELE (Fig. 2) was designed. The chip is currently under prototyping.

References

[1] D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective", in IEEE S3S Conf., pp. 49-50, 2015.

[2] http://e-peas.com/products/aem10940/

[3] D. Bol, E.H. Boufouss, D. Flandre and J. De Vos, "A 0.48mm2 5μW-10mW Indoor/Outdoor PV Energy-Harvesting Management Unit in a 65nm SoC based on a Single Bidirectional Multi-Gain/Multi-Mode Switched-Cap Converter with Supercap Storage", in Proc. European Solid-State Circ. Conf., pp. 241-244, 2015

[4] P.-A. Haddad, G. Gosset, J.-P. Raskin and D. Flandre, "Automated design of a 13.56 MHz 19 μW Passive Rectifier with 72% Efficiency under 10 μA load", in IEEE J. Solid-State Circuits, 2016

[5] G. de Streel, J. De Vos and D. Bol, "A ΔVT 0.2V to 1V 0.01mm^2 9.7nW Voltage Reference in 65nm LP/GP CMOS", in Proc. IEEE SOI-3D-Subthreshold Microelectronics Conf., 2 p., 2015.

[6] G. de Streel, J. De Vos, D. Flandre and D. Bol, "A 65nm 1V to 0.5V linear regulator with ultra-low quiescent current for mixed-signal ULV SoCs", in Proc. IEEE FTFC Conference, 4 p., 2014.

[7] S. Clerc et al, "A 0.33V/-40°C Process/Temperature Closed-Loop Compensation SoC Embedding All-Digital Clock Multiplier and DC-DC Converter Exploiting FDSOI 28nm Back-Gate Biasing", in Proc. IEEE Int. Solid-State Circuits Conf., pp. 150-151, 2015.

Ultra-low-power wireless communications

Keywords : RF; Ultra-wideband; Software-defined radio; 28nm CMOS; Noise-cancelling; IoT.

Guerric de Streel, Cecilia Gimeno, François Stas, Denis Flandre, David Bol

Abstract – For a massive yet sustainable Internet-of-Things, ultra-low-power wireless communications are required without compromising connectivity. In the electronic circuits and systems (ECS) group, we pursue new solutions to this challenge with ultra-low-voltage RF integrated circuit (IC) and system-on-chip (SoC) design. Latest results feature a 0.55V IEEE 802.15.4a Impulse-Radio Ultra-Wideband (IR-UWB) transmitter successfully prototyped in 28nm FDSOI CMOS and 0.5V 0-6GHz noise-cancelling LNA for software-defined radio receivers.

The connection of our daily life's objects to the cloud according to the Internet-of-Things (IoT) vision is about to revolutionize the way we live. To enable this revolution, a massive deployment of sensor nodes is required with predictions announcing up to trillions of these nodes. Such a massive deployment is not environmentally and economically sustainable with current technologies. Some of the pitfalls lay in the wireless communications of IoT nodes whose power consumption needs to be optimized in order to enable operation on ambient energy harvesting without compromising the connectivity [1]. Recent wireless solutions usually tackle the energy problem with low-duty cycled radios taking advantage of the ultra-low requirement on speed by the sensing application. However, key applications using audio/vision sensing or requiring low latency call for high datarates.

Impulse-Radio Ultra-Wideband (IR-UWB) is considered as a promising solution for high data-rate, short range and low-power solution due to the duty-cycled nature of the signal as well as the potential for low-complexity and low-power transmitter (TX) architectures. These characteristics have been the driving force behind the development of the IEEE 802.14.4a standard covering datarates from 0.11 to 27.24Mbps. In 2016, we propose a mostly-digital UWB transmitter System-on-Chip (SoC) codenamed SleepTalker, which was designed for ultra-low voltage in 28nm FDSOI CMOS compliant with the IEEE 802.15.4a standard. Operated at 0.55V, it achieves a record energy efficiency of 24pJ/bit (i.e. 650μW at 27Mbps) with embedded power management, highly duty-cycled digital baseband and programmable pulse shaping. This is a 250 $\times$ improvement compared to the commercial state-of-the-art. Wide-range on-chip adaptive forward back biasing is implemented for threshold voltage reduction, compensation of process/temperature variations and tuning of both the carrier frequency and the output power. The TX shown in Fig. 1 occupies a core area of 0.93mm^2.

Another connectivity challenge comes from the massive deployment of IoT nodes. To avoid the congestion of the RF spectrum, cognitive communications based on software-defined reconfigurable radio (SDR) architectures covering bands up to 6 GHz are needed for agile wireless communications. On the receiver (RX) side, these radios impose though requirementq on the low-noise amplifier (LNA) over a wide frequency range. In order to be integrated in complex SoCs, such LNAs should also be implemented in nanometer CMOS technologies to follow SoC development trends while benefiting from their high f_T. This technology scaling, however, has led to a supply voltage reduction to maintain device reliability. The simultaneous threshold voltage reduction is not as fast in order to keep the leakage current manageable. Reducing the supply voltage of RF analog circuits to ensure compatibility with digital parts or to reduce the power consumption challenges the analog design due to the reduced voltage headroom.

Figure 1: SleepTalker SoC microphotograph and application scenario (chip manufacturing donation from ST Microelectronics, Crolles, France).

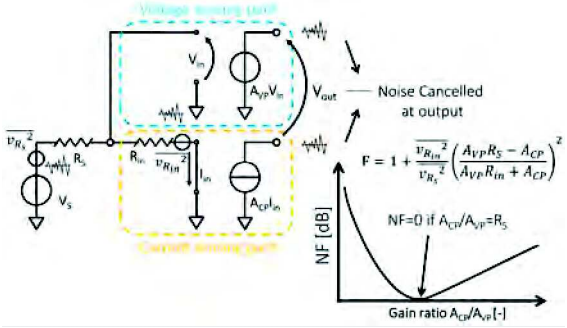

Figure 2: Noise cancelling principle used to build an ultra-low voltage LNA.

We show, that reducing the supply voltage pushes devices from strong inversion to moderate inversion and that forward back biasing can be used to mitigate this trend and increase the design space. We also study the impact of technology scaling on important RF figures of merit to highlight the ability of advanced 28nm FDSOI CMOS to trade speed for power. We then illustrate this ability at circuit level by looking at the optimum sizing of a noise cancelling ultra-low-voltage wideband LNA targeting the hot topic of SDR [2]. For this LNA, which operating principle is illustrated in Fig. 2, we show that technology scaling and forward back biasing are shifting the minimum supply voltage limitation from the bandwidth constraint to the noise constraint.

References

[1] D. Bol, G. de Streel and D. Flandre, "Can We Connect Trillions of IoT Sensors in a Sustainable Way? A Technology/Circuit Perspective", in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 49-50, 2015.

[2] G. de Streel, D. Flandre, C. Dehollain and D. Bol , "Towards Ultra-Low-Voltage Wideband Noise-Cancelling LNAs in 28nm FDSOI", in IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp. 236-237, 2015.