Université Catholique de Louvain

École Polytechnique de Louvain
ICTEAM institute

Design of a Single-Input/Multiple-Output Power Management Unit for Energy Autonomous Systems

Olivier de Caritat de Peruzzis

A Master thesis submitted in partial fulfillment of the requirements for the degree of Electromechanical Engineering

Advisors:
Denis Flandre (UCL)
Bob Puers (KULeuven)

Assistants:
David Bol
Julien De Vos

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Abstract

Energy autonomous systems (EASs) will be more and more used in applications that range from medical implant, biological detection and machine diagnosis to home security and other military applications. These systems achieve autonomy by harvesting energy from their immediate environment. Due to very low available power and volume constraints, EASs motivate the development of management systems, both power- and space-saving.

In this Master thesis, a state of the art of EASs is first presented with focus on the specific constraints of these systems and on the ways to answer them. A switched capacitor DC-DC converter is then proposed to power multiple outputs with different voltage and power levels. Three typical EAS devices, i.e a low-power microcontroller ($200\mu W$, $1V$), a radio ($30mW$, $2V$) and a sensor ($1\mu W$, $0.7V$), share this converter to be supplied from a $1.2 - 1.5V$ input source. An integrated on-chip converter that supplies the microcontroller and the radio achieves an efficiency close to 60% for a consumed silicon area smaller than $1.5mm^2$.

Résumé

Dans ... :)

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Introduction

Energy autonomous systems (EASs) take advantage of the ever-improving efficiency of energy harvesters, low-voltage digital circuits and battery technology to spread to new applications. Their autonomy and small size allow them to reach hard to access places where frequent battery replacements may be either infeasible or prohibitively expensive. In more and more industrial and medical applications, they will be used to get relevant information and provide it to the decision unit.

The power consumption of many embedded systems has been reduced to the same level as micro-scale energy harvesters are capable of generating. So, in order to achieve autonomy, EASs extract energy from their immediate environment. An in-depth understanding of various design considerations and tradeoffs is required when designing an efficient micro-scale energy harvester.

The volume of the components is critical as it limits both the amount of stored and harvested energy. The entire system should therefore be carefully designed to extract as much power as possible and transfer it to the consumers with minimal losses. Typical consumers are a micro-controller as processing unit, a sensor that measures a physical quantity and a radio for the information transmission. These consumers must obviously be as energy efficient as possible while respecting the volume constraints.

Due to the great variability of environmental energy sources, EASs usually dispose of a storage device as well as of a power conversion circuit. By storing energy for later use, continuous operation is made possible even at moments where there is no energy to harvest. The role of the conversion circuitry is to provide suitable voltage levels for each consumer. It is essential that the power management circuit dissipates very low quiescent power and can be accommodated

in a small volume.

The main topic of this Master thesis is to develop a management unit that respects the specific constraints of EASs. The first chapter gives a general overview of energy autonomous sensor systems and introduces two types of DC-DC converters : single inductor (SI) and switched capacitor (SC) converters. Both types enable efficient up and down conversion of the voltage but, for output powers lower than $50mW$, SC are generally preferred as they are more adapted to on-chip integration.

In the second chapter, the specifications of the problem studied in this Master thesis are defined and various possible solutions are discussed. SI or SC solutions are considered as well as combination of both types in a single converter. This analysis allowed us to imagine the converter proposed in this work and it gave us a comparison base as well as improvement perspectives.

In the third chapter, a switched capacitor converter is chosen because of its efficiency both in terms of power and volume consumptions. Its operation principle and the components design are first detailed. Afterwards, the associated control system is explained; it ensures a good regulation of the output voltages, in all operation modes.

In the fourth chapter, a simplified circuit is thorough studied. Two implementations are proposed and compared : the first one uses classical transistors and achieves an efficiency of 52.3% whereas the second one uses ultra-low-power (ULP) transistors as power switches and achieves an efficiency of 57%.

In the fifth chapter, a layout is realized for the ULP implementation; the consumed area is lower than $XXmm^2$. In order to establish the test methodology of the system, measurements were done on a similar converter.

CHAPTER 1

Energy Autonomous Sensor Systems : State of the Art

Exploiting the ever-improving energy efficiency of low-voltage digital circuits, battery technology and energy harvesters, it is possible, for some applications, to build sensor systems that do not require to be recharged during their entire operation life-time. In this chapter, an overview of energy autonomous systems will be presented. Afterwards, DC-DC converters that manage the energy transfers in EAS will be discussed. Single inductor and switched capacitor converters, will both be considered.

1.1 Overview of energy autonomous systems

An Energy Autonomous System (EAS) is defined as "an electronic system designed to operate and/or communicate as long as possible in known or unknown environments providing, elaborating and storing information without being connected to a power grid" [7]. The general structure of EASs, with the energy and data paths, is presented in Figure 1.1.

Along the energy axis, we can recognize four key functions in an EAS :

- **Energy generation :** to produce the energy needed in the system, from a solar cell, a fuel cell, a piezoelectric device, an antenna, a wind turbine or many other forms of energy sources.

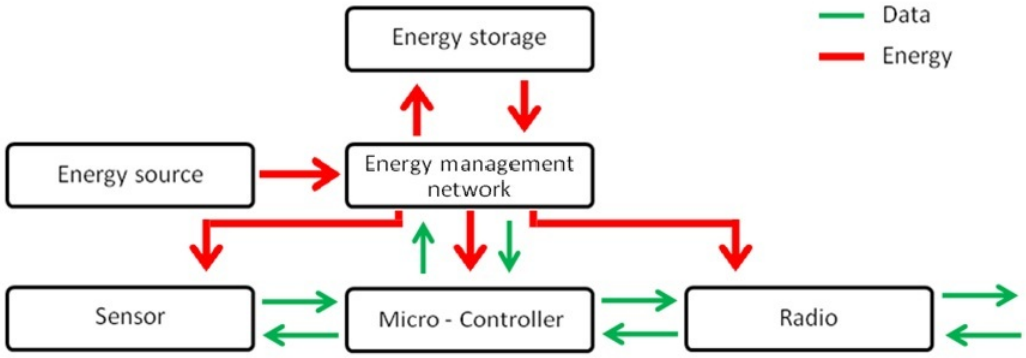


Figure 1.1 - Structure of typical Energy Autonomous Systems.

- **Energy storage :** to allow the system to continue its operations, energy must be stored in a capacitor, a battery or another storage element.
- **Energy conversion and optimization :** a rectifier or a DC-DC voltage converter is required to manage the energy transfers between the harvester, the battery and the energy consumers.
- **Energy use :** for sensing, computing and communicating.

Lower power consumption, better energy storage efficiency as well as suitable computation-communication tradeoffs are consequently very relevant research topics. The size of EASs is another critical point; most potential applications demand that each of the network components be unobtrusive. Medical monitoring and ambient intelligence are two examples of applications where EASs should be seamlessly embedded in the environment where they have to operate. The volume of the components must therefore be kept as small as possible. These volume constraints limit the amount of energy that can be stored or harvested by the EAS. The main design challenge is to enable continuous operation and long life-time despite these limitations.

Even through further improvements are desirable, the average power consumption in some miniature EAS components is low enough to be provided by embedded energy harvesting systems. Different harvesting principles will be discussed in section 1.1.1. When there is no energy to harvest, the system must draw on its reserve to ensure continuous operation. Some storage devices will be compared in section 1.1.2. Harvesting energy from the direct environment allows systems to recharge their batteries, eliminating thereby the maintenance costs of replacing them periodically. The highest contributor to energy consumption in EASs often remains the wireless data transmission [8]. In section 1.1.3, various operational life extension techniques will be briefly introduced.

1.1.1 Energy harvesting

Energy harvesting consists of extracting energy from the immediate environment. Harvesting light or thermal energy outputs power in the form of direct current (DC) whereas harvesting mechanical vibrations or radio electromagnetic waves provides power in the form of alternating current (AC). Since integrated circuits usually operate on a DC power source, AC-DC conversion is required in AC cases to rectify the power supply. Power density (W/cm^3) is the main characteristic of energy harvesters as they never run out of energy as long as the ambient energy source is present; they cannot be viewed as capacity-limited energy sources. Results of a survey [7] on the estimated energy output values for each harvesting principle at the state of the art, are presented in Table 1.1.

Sources	**Source Characteristics**	**Physical Efficiency**	**Harvested Power**	**Output current**
Photovoltaics				
Indoor	$0.1\frac{mW}{cm^2}$	$10-24\%$	$10\frac{\mu W}{cm^2}$	DC
Outdoor	$100\frac{mW}{cm^2}$		$10\frac{mW}{cm^2}$	
Thermal energy				
Human	$20\frac{mW}{cm^2}$	0.10%	$25\frac{\mu W}{cm^2}$	DC
Industry	$100\frac{mW}{cm^2}$	3%	$1-10\frac{mW}{cm^2}$	
Vibration/Motion				
Human	$0.5m@1Hz$ $1\frac{m}{s^2}@50Hz$	max power is source dependent	$4\frac{\mu W}{cm^2}$	AC
Industry	$1m@5Hz$ $10\frac{m}{s^2}@1kHz$		$100\frac{\mu W}{cm^2}$	
RF (EM energy)				
$900MHz$ GSM	$0.3-0.03\frac{\mu W}{cm^2}$	50%	$0.1\frac{\mu W}{cm^2}$	AC
$1800MHz$	$0.1-0.01\frac{\mu W}{cm^2}$			

Table 1.1 - Estimated power output values per harvesting principle.

Photovoltaics is a method of generating electrical power by converting solar radiation using semiconductors that exhibit the photovoltaic effect. Outdoors, that solution presents a relatively high harvested power which is however reliant on adequate exposition conditions. Indoors, artificial lighting is more constant but allows for less harvested power. Typical single junction solar cells have an efficiency of 10 to 24%. Research is being carried out on multi-junction solar cells to achieve an efficiency of over 40% but they are currently more expensive to mass produce [34]. The I-V characteristics as well as the maximum-power point of solar cells are function of the light intensity and the temperature.

The thermoelectric effect extracts energy from a temperature difference between two junctions to generate a small amount of electricity. At the atomic scale, an applied temperature gradient causes charges to diffuse in the material from the hot to the cold side. The output power mainly depends on the thermal gradient.

The piezoelectric effect is one of several ways to convert vibrational energy to electrical power; an electrical potential is generated on certain crystal or ceramic materials in response to an applied mechanical stress. The electrostatic effect (capacitive) or electromagnetic effect (inductive) also allows extraction of power from vibrations. The output power depends both on the magnitude and the frequency of the source waveform.

Concerning the radio frequency, ambient electromagnetic radiation emitted from wi-fi transmitters, cell-phone antennas, TV masts and other sources, is converted into AC electrical current. The path loss in free space is proportional to the square of the ratio $\frac{R}{\lambda}$, with R the distance between the power source and the harvester, and λ the wavelength of the RF signal; the estimate presented in Table 1.1 is based on average power densities measured in a home environment.

In order to obtain suitable voltages, it can be necessary to stack multiple harvesters. For example, photovoltaic cells $(0 - 0.5V)$ can be stacked in series to obtain a higher output voltage. So as to decrease the temporal variability of the generated power or to increase the total collected energy, it can be useful to combine multiple harvesting modalities to form a hybrid energy harvester. The design of the harvester is crucial insofar as it significantly impacts the complexity and the performances of the conversion circuit.

Due to the great variability of the temporal profiles of sources based on harvesting, an important issue is to design a mechanism allowing output nodes to maintain their power supply at sufficient levels. Moreover, the output power of an energy harvester varies with the intensity of the source but also with the load it sees. The maximum power point MPP is the optimum that best matches the inherent impedance of the harvester [24] [26]. Achieving the MPP in a hybrid energy harvester is an important research topic.

1.1.2 Energy storage

Harvesters extract virtually unbounded ambient energy but their power levels are particularly low, intermittent and often unpredictable. Thus, as the availability of harvested energy is sporadic, it must be detected and stored : the system needs to continue its operations even when there is no energy to harvest. In order to fulfill the volume constraints of EASs and to deal with the related small amount

of energy, storage components need to be compact and efficient.

Various energy-storage devices are presented in Figure 1.2. The devices typically do not present high energy and high power densities concurrently. Capacitors and inductors offer relatively high power densities and a good round-trip efficiency [17] but they suffer from self-discharge. Another disadvantage to using capacitors is the fact that the more they are charged, the more difficult it becomes to add extra charges. Lithium-ion batteries offer a balanced compromise in energy, power and speed while exhibiting low losses. Batteries however suffer from aging and rate-capacity problems from which capacitors are immune. A typical battery can store about $1000 J/cm^3$ whereas high performance ceramic capacitors can store $1 - 10 J/cm^3$ [23].

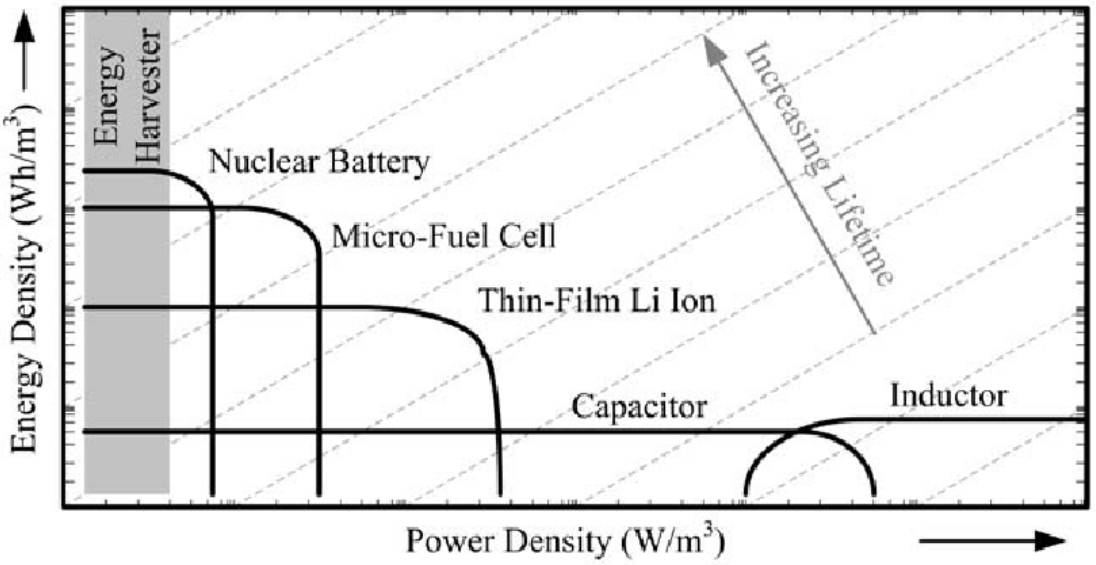


Figure 1.2 - Ragone plot of state-of-the-art energy sources [9].

Fuel cells and nuclear batteries present good energy densities but are not rechargeable, i.e. they can not store any excess energy from the harvester. An atomic battery uses the emissions from a radioactive isotope to generate electricity. They are very expensive but have an extremely long life time. A fuel cell converts chemical energy into electric energy. In addition to low power levels and finite on-board energy, they also suffer from slow reaction times and fuel loss through the membrane.

The choice of an energy storage device depends on the temporal profile of power consumption of the load. For example, a system that needs to operate for a long period without being recharged and store large amounts of energy, say, for an all-night use after an all-day charge, will need the energy density offered by a battery.

The most commonly used rechargeable batteries are [25] : Nickel Metal Hydride, Lithium based, Nickel Cadmium and Sealed Lead Acid. The two last types are less common because of their lower energy density and their temporary capacity losses. At the moment, secondary Lithium-ion batteries are the most commonly used energy storage devices for EASs [7] [17] [27]. Compared to Nickel Metal Hydride batteries, they are more efficient, have a longer cycle life-time and a higher density; they also present a lower self-discharge rate. However, Lithium based batteries are usually more expensive, even if their increased life cycle is taken into account. Table 1.2 presents some characteristics of various battery types [29] [35].

Battery type	Energy density $[Wh/dm^3]$	Self-discharge [% per year]	Cycles
Ni-Cd	100	15-20	300
Ni-MH	175	20	300
Li-ion	200	5-10	500

Table 1.2 - Main characteristics of commonly used batteries.

Batteries are a relatively mature technology : after about 15 years of fast improvements, their energy density approaches its theoretical maximum. However, a battery typically needs to be supplied with a voltage of $1.5 - 3.7V$ in order to start storing energy [22]. Voltage up-conversion is therefore necessary if the harvested voltage is lower as is typical for photovoltaic cells, thermo-electric generators or micro-fuel cells. Another issue is that miniature batteries provide intrinsically lower energy density than their macroscopic counterparts [8]. Indeed, the ratio between passive packaging material and active material becomes larger in small batteries.

Research is ongoing to miniaturize batteries for use in EAS and to make them compatible with integrated circuit (IC) processes. Using new materials is necessary in order to try to obtain a life-time of more than 10 years or several thousand charge and discharge cycles.

1.1.3 Operational life extension

Different techniques exist to extend EASs' operational life :

- **Duty-cycling** : it allows to decrease the average power consumed by performing the power-intensive tasks on demand, periodically or asynchronously, often letting the system idle. Duty-cycling however does not influence the peak power requirements. Many algorithms using duty-cycling were developed to maximize task performances [19] [28]. Some of them use models to predict future energy opportunities based on historical data [20].

- **Dynamic voltage scaling** : By adapting the digital circuit supply voltage V_{dd}, it allows to meet dynamically varying performance requirements while maintaining peak performances [38] [21].
- **Body Bias technique** [36] : the circuit characteristics can be modified. By applying a reverse body bias, the gate leakage of a transistor can be decreased by increasing the threshold voltage. In so doing, the consumption in idle mode can be reduced. By applying a forward body bias, a lower threshold voltage makes higher transistor speeds possible. This way, the performance of a digital circuit in active mode can be increased. This technique however requires new voltages if they are not already available, so up or down conversion, with inherent losses, is necessary.
- **Frequency reduction** : it reduces the power consumption but negatively impacts performance.
- **Hybrid system** : it can avoid over-sizing a single storage device or a single source [9].

To meet all their requirements, EASs need tradeoffs between the energy consumed by processing, storage and communication resources on one hand and the fidelity, throughput and latency on the other hand. Another way to supervise the consumption is then to make the appropriate tradeoffs. Figure 1.3 shows the consumption of some typical wireless transceivers and microprocessors. The power corresponding to a lower data rate is lower. It also seems that transmitting data wirelessly consumes more power on average than processing data at a given rate. That justifies the tradeoff between communication and processing, i.e. one will process the information on chip in order to send a smaller amount of data.

1.1.4 Example of application

Energy autonomous sensors can be used in Body Area Sensor Networks (BASNs); those networks take advantage of the integration of intelligent, miniaturized, low-power sensor nodes in, on, or around human bodies to monitor body functions [10] [18] [30]. BASNs enable personalized and individual monitoring in healthcare, fitness, entertainment or interactive gaming. Researchers are working on improvements for medical applications as varied as drug delivery, heart regulation, prosthetic actuation or deep brain stimulation. Note that this technologies will also help protect people exposed to life-threatening environments such as soldiers, astronauts or first responders.

The size, cost, compatibility and perceived value are some of the many obstacles to address in order to make those systems comfortable enough to overcome inconvenience and invasiveness. Constraints specific to applications such as biocompatibility or resistance to extreme temperatures or pressures also

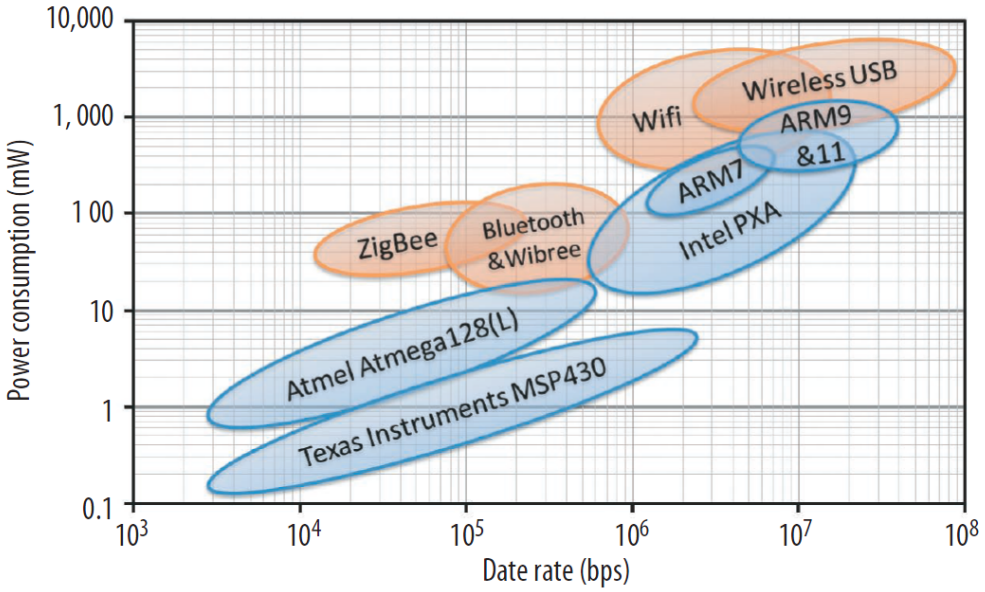


Figure 1.3 - Wireless transceivers (orange) consume more power on average than processors (blue) for a given data rate [10].

are to be taken into account.

Figure 1.4 presents a wireless electroencephalography (EEG) acquisition system. On the top layer is the radio used to communicate with the computer. The micro-controller (μC)is integrated on the layer below while the layer beneath holds the sensor. As for the power layer, a prismatic Li-ion battery with $150mAh$ capacity and a $3V$ voltage regulator is used.

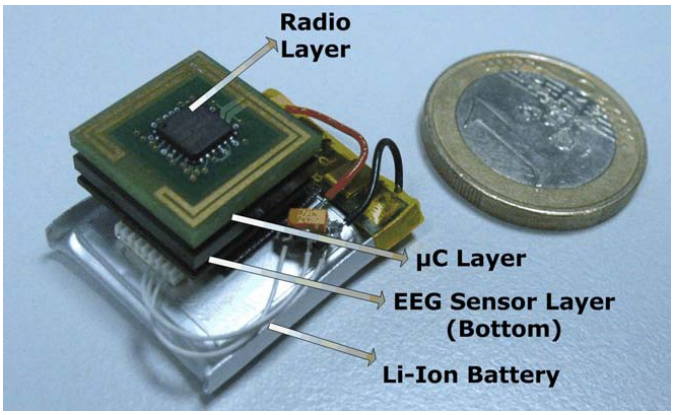


Figure 1.4 - $1cm^3$ EEG acquisition system [30].

The power dissipation of this $1cm^3$ wireless EEG acquisition system is dominated by that of the radio. For a sampling rate of $2048Hz$, the consumptions of the radio, the micro-controller and the EEG sensor are respectively

$2.25mW$, $0.7mW$ and $0.3mW$. The sensor is responsible for only 10% of the total power disspation. As a result, the system has a power autonomy of $60h$ until the battery runs out. To increase the autonomy, a thermoelectric generator is placed on the forehead of the subject to convert waste heat from the forehead into electrical power [33]. At $23°C$, it produces approximately $2mW$ or $30\mu W/cm^2$ while the power dissipation of the electronic system reaches $0.8mW$.

1.2 DC-DC converters

Energy harvesters generate AC or DC power that can vary over time, depending on the available energy. At the other end, the electronic systems usually require a stable voltage supply. In addition, the energy consumers often need to be supplied at another voltage than the one given by the storage element. Therefore, to provide suitable voltage levels, a conversion bloc is normally needed in EAS components which get energy from energy harvesters. That bloc must manage the energy transfers in the system. If the available harvested energy is an AC signal, it must be transformed into DC by an appropriate rectifier. In this section, converters using an inductor or based on the switched capacitors technique will be discussed.

1.2.1 Single inductor DC-DC converters

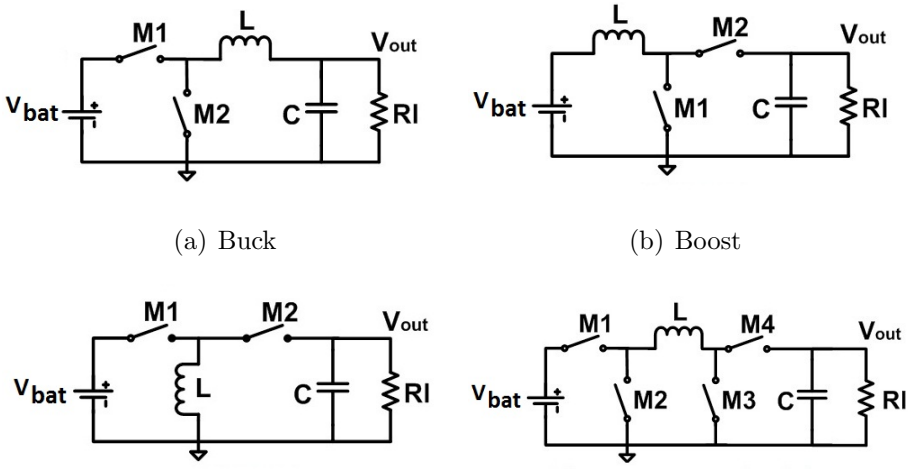
A Single Inductor (SI) DC-DC converter is an electronic circuit that converts a supply voltage V_{in} to an output voltage V_{out}, using only one inductor and switches. The working principle of SI converters is ordinarily decomposed into two phases:

- Phase ϕ_1 : Establishment of the current in the inductor.
- Phase ϕ_2 : That current charges the output capacitor.

In this section we will first present some SI converter architectures. We will then identify the main contributors to power losses as well as the specific problems of inductive converters. Finally, an example of an EAS application using an inductor based converter will be discussed.

Single-inductor single-output DC-DC switching regulators

Figure 1.5 presents four conventional Single-Inductor Single-Output (SISO) DC-DC switching converters.



(a) Buck (b) Boost

(c) Inverting buck-boost (d) Non-inverting buck-boost

Figure 1.5 - Conventional topologies of SISO DC-DC switching regulators.

The charges and discharges of the inductor are regulated by the switches with non overlapping phases ϕ_1 and ϕ_2. During phase ϕ_1, the current is established through the inductor (L) : switches $M1$ and $M3$ are passing. During phase ϕ_2, switches $M2$ and $M4$ are passing such that the current flowing through L charges the capacitor (C). A control-loop ensures that the output voltage (V_{out}) becomes as close as possible to a reference voltage. The buck 1.5(a) and boost 1.5(b) architectures can respectively only increase or decrease the battery voltage (V_{bat}). The inverting 1.5(c) and non-inverting 1.5(d) buck-boost schemes can both increase and decrease this voltage.

Single-Inductor Multiple-Output DC-DC switching regulators

The four SISO schemes of Figure 1.5 can be transformed into Single-Inductor Multiple-Output (SIMO) versions by duplicating the switch on the load side. Note that, as the single output buck scheme 1.5(a) does not have any switch on the load side, it is necessary to add an extra switch for each output. As an example, the scheme of a buck converter with two outputs is shown in Figure 1.6.

In order to supply multiple outputs with a single inductor, it is necessary to time-share the inductor current between various loads. In that case, particular care has to be taken to avoid cross regulation, as explained later in this section. In the example of Figure 1.6, either $M3$ or $M4$ is passing.

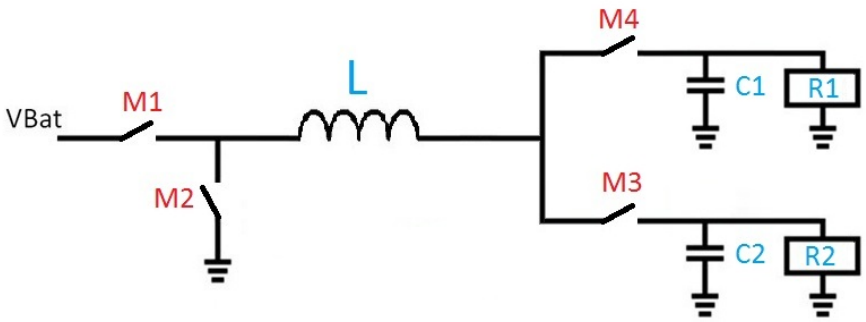


Figure 1.6 - Single-input dual-output buck converter.

Efficiency

Power efficiency is defined by the ratio $\eta = \frac{P_{out}}{P_{in}}$, where P_{in} and P_{out} are respectively the input power and the power transferred to the output. Their difference gives the power loss : $P_{loss} = P_{in} - P_{out}$.

The main contributions to P_{loss} are [36] the conduction losses resulting from the ohmic losses in the switches and in the inductor serial resistor : $P_{conduction} = \sum_i I_{rms,i}^2 R_i$ where $I_{rms,i}$ is the root mean square (rms) current through the resistance R_i. Because of the increasing effective resistance of the inductor, those losses increase with the frequency.

The switching losses are mainly caused by the charging and discharging of the gate capacitances of the power switches and of the parasitic capacitances : $P_{switching} = \sum_i f C_i V_g^2$ where V_g is the gate voltage of the switch, generally equal to the supply voltage V_{bat}. They are obviously proportional to the switching frequency f and the value of those capacitances C_i. The switching losses and the conduction losses must be traded off : increasing the size of the power switches will increase the switching losses but decrease the conduction losses. Another trade-off can be made on the gate voltage of the power switches V_g : increasing the gate to source voltage V_{gs} will increase the switching losses but decrease the conduction losses.

The dead-time losses occur when both power switches of each phase are in the off-state. If the inductor current I_L is not equal to zero during that dead-time period, it will flow through the body diode of one of the power switches, giving : $P_{dead-time} = I_L V_{diode}$ where V_{diode} is the body diode forward voltage.

Finally, when the inductor uses a magnetic core, inductor core losses occur. They include eddy-current and hysteresis losses which are both frequency dependent. Using a magnetic core has the advantages of a smaller inductor area

and of a reduction of the electro-magnetic interference (EMI) concerns.

Power switches driving

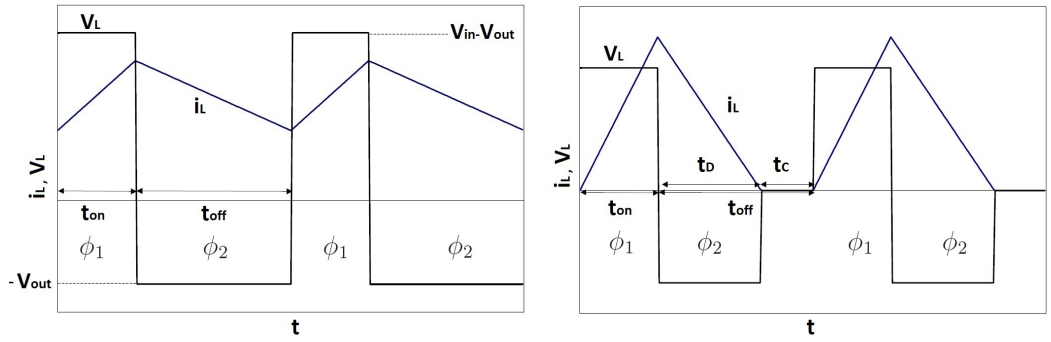
The power switches driving strategy impacts the system efficiency in terms of both area and power. The switches connected to the battery and those connected to the ground are obviously made by p-channel and n-channel devices, respectively; this way, the threshold voltage does not negatively influence the charge transfer. There are however three possibilities for the load side switches [5] :

- A P-channel switch is a good solution when the output voltage is much higher than the transistor threshold voltage. Considering their lower conductivity, P-channel switches require a higher area in order to present the same resistance as their N-channel equivalent.
- An N-channel switch needs a gate voltage higher than the supply voltage to be properly opened. The higher sypply voltage can be provided by a small charge pump, i.e. a kind of DC-DC converter using capacitors. Nevertheless, this solution can lead to area and efficiency issues. For a multiple output buck converter, the gate voltage of the load side switches can be equal to the supply voltage.
- A Complementary switch, combining an NMOS and a PMOS switches, requires almost twice the area. This solution is usually reserved for applications with very low current. In that case, the size of the transistors and therefore the power required to charge and discharge their gate are not excessively large.

Conduction mode

A converter with a single inductor operates either in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). Figure 1.7 presents the inductor current i_L and the voltage across the inductor V_L of a buck converter 1.5(a), both in CCM 1.7(a) and DCM 1.7(b). In CCM, the current is established in the inductor during t_{on}, thereby also powering the load Rl. Then, during t_{off}, the inductor (L) is partly discharged into the output capacitor C and the load Rl. In DCM, the current is established in the inductor during t_{on}. Afterwards, during t_D, the inductor is fully discharged into C and Rl. Finally, during t_C, Rl is powered by C as there is no more current flowing through the inductor.

In the case of multiple outputs, CCM leads to stability concerns due to cross regulation as i_L does not decrease to zero : if cross regulation occurs, the outputs are more difficult to regulate independently because changes in one output may affect the others. Moreover, CCM requires a high switching frequency and the associated losses could be excessive in a low power system. In DCM, the current



(a) Continuous Conduction Mode (CCM). (b) Discontinuous Conduction Mode (DCM).

Figure 1.7 - Conduction modes of a buck converter.

falls down to zero before the end of the conduction period and it stays at zero until the next charge period. DCM thus allows one to avoid cross regulation but the current ripples and the peak inductor current are larger, which affects the performance of the converter on voltage ripples, switching noise and dynamic response.

By placing an additional switch across the inductor, a pseudo-continuous conduction mode (PCCM) can be obtained [6] which allows the inductor current to stay above zero as in the CCM while the cross regulation is eliminated.

Energy transfer

In an inductive converter, the energy transferred per cycle E_L is proportional to the square of the load current [8]:

$$E_L \propto \frac{LI_{load}^2}{2} \tag{1.1}$$

where L is the inductance used in the converter and I_{load} is the load current. Considering a constant output voltage, the output power decreases linearly with the current while the energy transferred per cycle decreases quadratically. As a consequence, larger inductors or higher switching frequencies must be used in lower power applications. The first option requires large volumes which are difficult to realize in miniature EAS. The second option may lead to a lower efficiency because of the losses in the switches.

Example of an SI DC-DC converter in an EAS

In the literature, there is a trend to reduce the number of successive converters in low power applications [14] [15] [16]. Combining converters allows one to reduce

the system cost and to increase the total power efficiency by reducing the number of converters between the harvesters and the load. The control of those converters is however more complicated.

An SI dual input dual output DC-DC converter for solar energy harvesting applications [14] is shown in Figure 1.8. The inputs are a rechargeable battery (V_{Bat}) and photovoltaic cells (V_{PH}) while the outputs are a load (V_O) and the battery. The role of the converter is double : to provide a regulated output voltage to the load and also to regulate the input voltage in order to extract the maximum power from the photovoltaic cells.

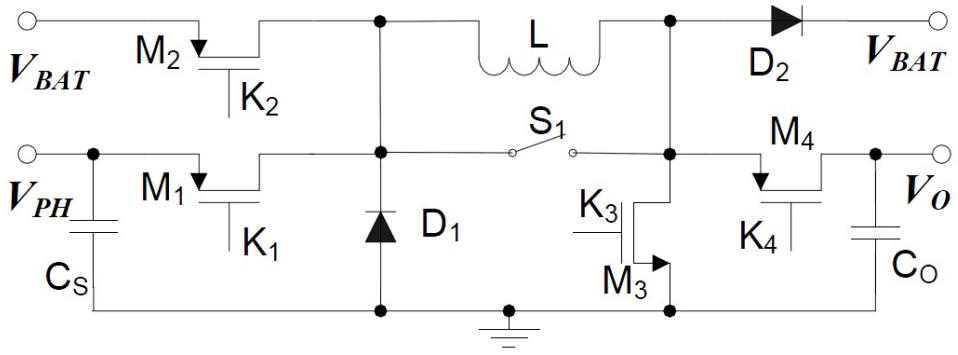


Figure 1.8 - Single-Inductor Dual Input Dual Output [14].

The converter operates in different modes according to the load power consumption and the photovoltaic cells power output. The battery is charged (resp. discharged) when the power provided by the PV cells is larger (resp. lower) than the power consumed by the load. The power transfer efficiency, defined as the ratio of the power flowing out the converter over the power flowed into the circuit, was simulated for different operating modes. The results are presented for different load powers in Figure 1.9.

Light intensity 1 corresponds to $2.19V$ and $2.54mA$ at the PV cells output while light intensity 2 corresponds to $2.56V$ and $5.72mA$. Since the PV output power depends on the light intensity, the mode switch between light and heavy load operates when the load current becomes higher than $3mA$ in case 1 and than $8mA$ in case 2. The power efficiency in the light load mode is lower than the one in the heavy load mode because more power transistors are switched in light load mode, so the switching power loss is larger. The efficiency of that converter reaches 90% for an output power close to $18mW$.

1.2.2 Switched capacitor DC-DC converters

A Switched Capacitor (SC) converter, also called a charge pump, is an electronic circuit that converts a supply voltage V_{in} to an output voltage V_{out} several times

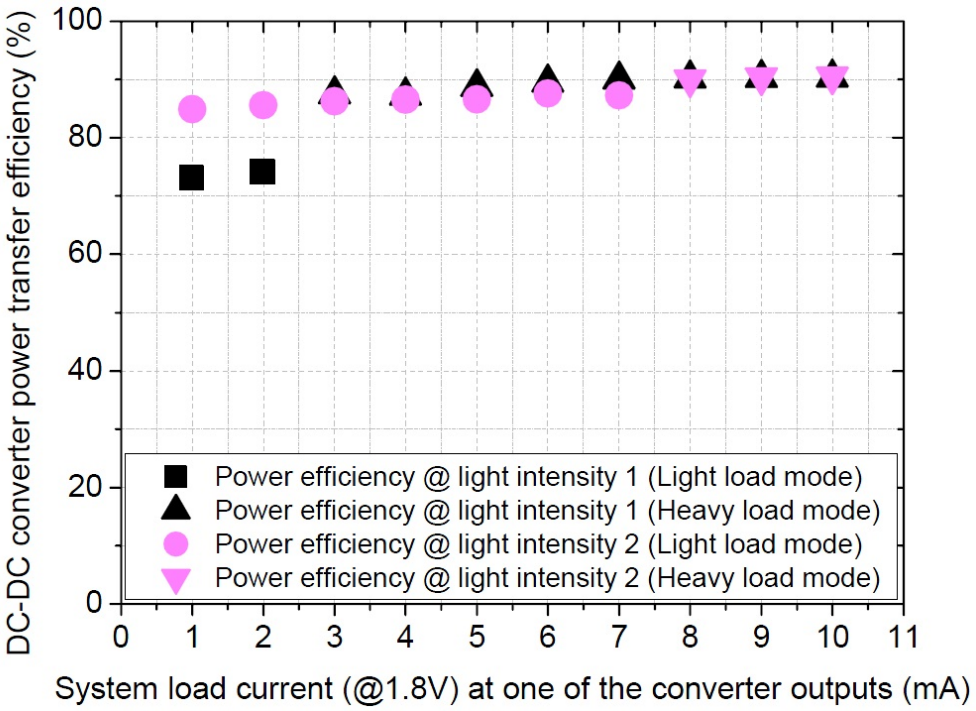


Figure 1.9 - The power transfer efficiency reaches 90% [14].

higher or lower. SC converters are only made of capacitors and switches, thereby facilitating the integration on silicon in comparison with an inductor based solution. Indeed, in SC converters, the size of the switching component do not have to increase as the output power decreases, so, they have a better quality factor than SI converters. The working principle of SC converters is ordinarily decomposed into two phases :

- Phase ϕ_1 : Charge of the transfer capacitor C_T.
- Phase ϕ_2 : Transfer of the charges of C_T to the output.

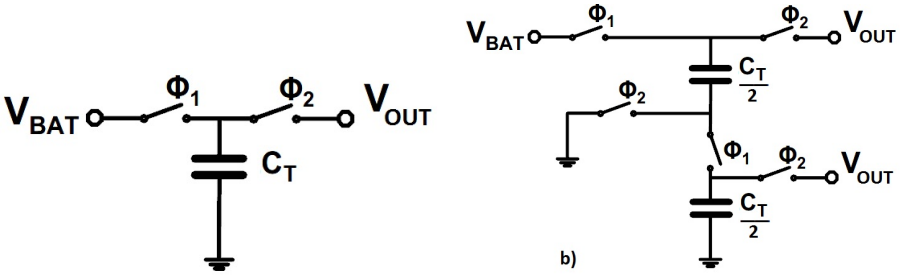
The total transfer capacitor C_T is used to transfer charges from the input to the load.

SC converters generally require a feedback control system in order to ensure appropriate line and load regulations [2]. On the one hand, their voltage conversion ratio is indeed fixed by the structure of the circuit, i.e. without control, a change of the input voltage would imply a proportional change of the output voltage. On the other hand, a feedback is necessary to maintain a constant output voltage despite changes in the load consumption.

Different architectures have been presented in the literature, some of which will be briefly discussed in the following of this section. We will then study the power delivery of this type of converter before identifying different sources of losses.

Topologies of Switched Capacitor Converters

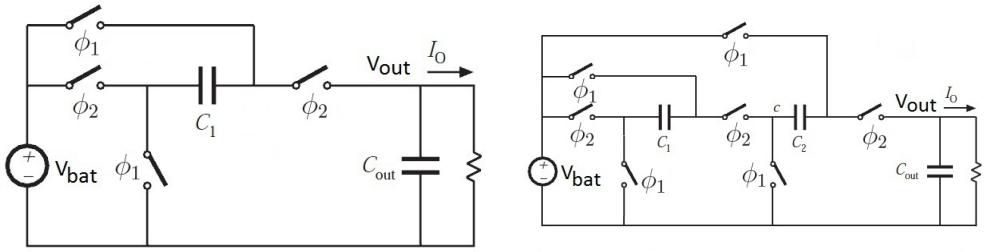
Two simple topologies of SC converters are presented in Figure 1.10. The SC based linear voltage regulator of Figure 1.10(a) provides V_{bat} at no load whereas the voltage divide-by-2 circuit of Figure 1.10(b) uses two transfer capacitors $\frac{C_T}{2}$ to provide $\frac{V_{bat}}{2}$ at no load. In the last topology, the transfer capacitors are charged in series and discharged to the load in parallel. Transfer capacitors two times smaller were used to maintain the consumed silicon area.



(a) Linear voltage regulator. (b) Voltage divide-by-2 circuit.

Figure 1.10 - Two SC converter topologies.

It is also possible to raise the voltage with SC converters. The topologies of a voltage doubler and that of a voltage tripler are presented in Figure 1.11.



(a) Ideal SC voltage doubler. (b) Ideal SC voltage tripler.

Figure 1.11 - Two SC converters rising voltage. Switches '1′ are on during phase ϕ_1 and switches '2′ during phase ϕ_2.

Power delivery

In order to calculate the power delivered to the output, we will study the switched capacitor circuit with and without its load. We consider in the following that the switches are big enough to transfer the charges in the alloted period. We first consider the no-load case, in other words, the case where the transferred power and the load current are null : $P_{load} = I_L = 0$. In this case, the output voltage

only depends on the circuit topology : $V_{out} = V_{no-load}$.

We now consider the load case, i.e. when the load current is different from 0 : $I_L \neq 0$. The average current is equal to :

$$I_{av} = \frac{Q}{T_s} = f_s \cdot Q \tag{1.2}$$

where Q represents the amount of charges transferred from the transfer capacitors to the output, T_s is the switching period and f_s the switching frequency. Considering the system in regime, the output voltage is, on average, equal to V_{out}. Before the charges are transferred to the output, the voltage across the transfer capacitors is equal to $V_{no-load}$ while it decreases to the output voltage when the transfer is complete. The transferred charges Q and the corresponding average current I_{av} are then :

$$Q = C_T(V_{no-load} - V_{out}) = C_T \Delta V \tag{1.3}$$

$$I_{av} = f_s C_T \Delta V \tag{1.4}$$

Finally, the power transferred to the output is found by multiplying this current by the output voltage V_{out} :

$$P_{load} = f_s C_T V_{out} \Delta V \tag{1.5}$$

P_{load} then depends on the frequency f_s at which the charges are transferred to the output capacitor, the total value of the transfer capacitor C_T, the output voltage V_{out} and the difference of output voltages between a loaded and an unloaded output : $\Delta V = V_{no-load} - V_{out}$. For a given switching frequency, V_{out} has to be decreased with increasing load current in order to allow C_T to provide enough charges to the output, another solution is to increase the total transfer capacitor C_T.

Efficiency analysis

The efficiency of the power converter is a key metric for autonomous systems. The main contributors to efficiency loss in SC DC-DC converters are : conduction loss, loss due to bottom-plate parasitic capacitors, gate-drive loss and power consumed by the control circuitry.

A theoretical upper limit for the efficiency η of two phases SC DC-DC converters is given by :

$$\eta_{max} = \frac{V_{out}}{V_{in} \cdot M_i} = \frac{V_{out}}{V_{no-load}} \tag{1.6}$$

where M_i is the ideal DC conversion ratio when the converter is unloaded : $\frac{V_{no-load}}{V_{in}}$. It only depends on how the capacitors are interconnected in the

switched networks corresponding to the two phases. Thus, the efficiency might be unacceptably low if V_{out} is not close enough to the product $V_{in} \cdot M_i$ which is a condition difficult to satisfy if V_{in} or V_{out} presents a wide range of values. That upper limit to the efficiency is due to the fact that the charges Q, that were initially at a potential $V_{no-load}$, are distributed on the capacitors C_T and C_{out} at a lower potential V_{out}. This way, the system minimizes its intrinsic energy.

To illustrate those losses, we can make an analogy with communicating vessels, as shown in Figure 1.12. In a first state, the water is in one container, just as the charges are on a capacitor. When a valve allows the water to flow in another container, the system will go to state 2 where the total potential energy of the water is the smallest; the charges will be distributed the same way on the two capacitors. The energy dissipated in the transfer is equal to the energy required to return to the previous state. The dissipation occurs within the path resistance between the vessels or between the capacitors. In this example, it is also clear that the first vessel, i.e. C_T, will not transfer all its energy to the output but that the transfered energy will be proportional to the height difference, i.e. ΔV.

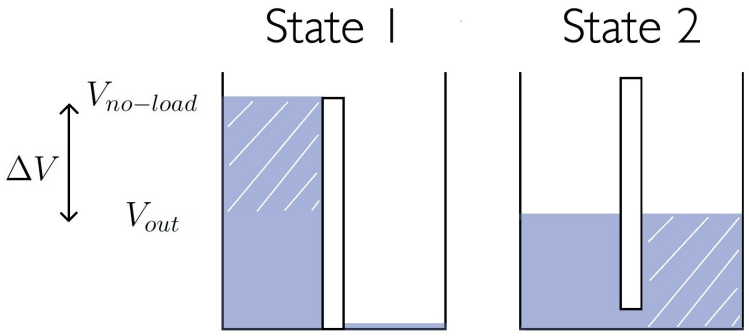


Figure 1.12 - The system minimizes its intrinsic energy.

Conduction losses are one of the main sources of loss in SC converters. They happen through the parasitic resistance of the circuit while charging and discharging the transfer capacitor.

The parasitic capacitor between the bottom-plate of C_T and the substrate is charged and discharged during the circuit phase changes. Figure 1.13 illustrates the bottom plate capacitor. This switching is undesirable because it does not contribute to the energy transfer. To reduce those losses, we should avoid capacitors built close to the substrate, or at least reduce the capacitor value by decreasing the plate surface S_{bottom} and by increasing the distance to the substrate d_{sub}. Reducing the switching frequency f_s also limits the energy spent to the charging and discharging of this capacitor. It is interesting to note that different topologies providing the same M_i ratio can generate different amounts of bottom-plate losses.

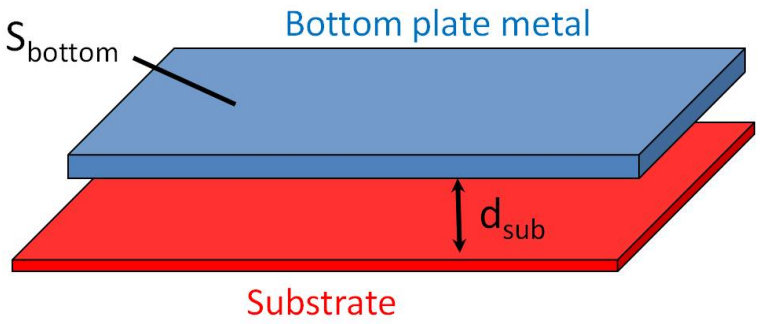


Figure 1.13 - Bottom plate capacitor.

Gate-drive losses are induced by the charges and discharges of the gate capacitors of the switches which are typically wide transistors in SC networks. A common way to reduce those losses is to dynamically adapt the size of the switches to the current to be driven. This way, the gate capacitor of each commanded transistor is kept as small as possible at each time.

Concerning the control strategy, two different approaches can be distinguished : Pulse-Width Modulation (PWM) and Pulse frequency Modulation (PFM). With PWM, the duty cycle for driving the power switches is varied while the switching frequency is kept fixed. On the contrary, in the PFM case, the frequency will increase with the output current to be delivered. The use of PFM instead of PWM allows us to reduce the number of switchings, especially at low output power, thereby enabling us to reduce gate-drive losses and the bottom-plate parasitic capacitors losses [3] [36]. Indeed, the switching losses are kept proportional to the output current I_{out}. The main drawback of using PFM is the unpredictable spectrum of the generated noise, as the frequency modulation depends on the required I_{out}.

The power consumed by the control circuitry that generates the gate signals of the switches is a direct loss. Circuits hungry for quiescent current should therefore be avoided.

Example of an SC converter in an EAS

A voltage scalable SC converter makes use of multiple topologies to achieve scalable voltage generation [3]. The idea is to suitably combine parts of the total transfer capacitor C_T to obtain various topologies. 12 capacitors of equal value were used which made it possible to reach 70% efficiency over a range of load power from $5\mu W$ to $1mW$, while delivering load voltages ranging from $0.3V$ to $1.1V$.

see [36] p. 6-7 for the remarks

example in [2].

1.3 Conclusion of the chapter

In this chapter we have investigated different types of DC-DC converters and given some examples of applications.

SC converters are more suitable for low power devices (BECAUSE ?) but...

SC and *SI* converters both introduce noise on the power supply due to their inherent switching nature. That makes them more suitable for noise-tolerant digital systems.

An *SI* converter requires the use of an inductor, whereas an *SC* one uses only capacitors, making it more adapted to on-chip integration. It is indeed easier to integrate capacitors on chips than inductors.

We briefly described the major harvesting sources and possible energy storage methods. Based on this study, we came to the conclusion that the combination of energy harvesters with storage elements represents a promising solution to supply EAS.

For low output power generators, switched capacitor converters are favored due to their better integration possibilities compared to inductive converters.

Drawbacks of technological improvements mean that the processes combine high cost per area with low energy storage density which complicates the integration of the necessary reactive elements.

Different strategies were presented to limit the power losses. It should be noted that a common approach is to combine some of the exposed strategies to get their different benefits.

Note that the comparison among the different applications proposed in the literature is both complicated and unfair because of the different functionality and constraints required in each case, e.g. size, power consumption or input and output voltages.

In this chapter, the state of the art of energy autonomous systems was described. Both switched capacitor and inductive power converters were presented. Both type enable efficient up and down conversion, which is required in many applications.

Comparing the converters, inductive converters generally enable higher output powers whereas switched capacitor converters are more suitable for low output powers. However, SC with output power in the range of inductive converters are appearing [36] (EN PARLER AILLEURS).

CHAPTER 2

Problem Statement : SIMO Power Management Unit

Energy Autonomous Systems often require a converter bloc to manage the energy transfers. In this chapter, different Single-Input Multiple-Output (SIMO) DC-DC converters will be considered. First, the goals and constraints of the problem will be explained. Second, two types of converters will be studied : we will present single inductor based solutions and inductorless solutions. Finally, weaknesses and strengths will be detailed for each case.

2.1 Definition of the Problem

The objective of this work is to develop a converter that has to provide power to a microcontroller (MC), a radio (rad) and an analogical sensor (A) in various operation modes. The different specifications of those consumers will be given in section 2.2. In this chapter, we will consider that a battery of $1.5V$ is available as an energy source. The topology of the converter is presented in Figure 2.1.

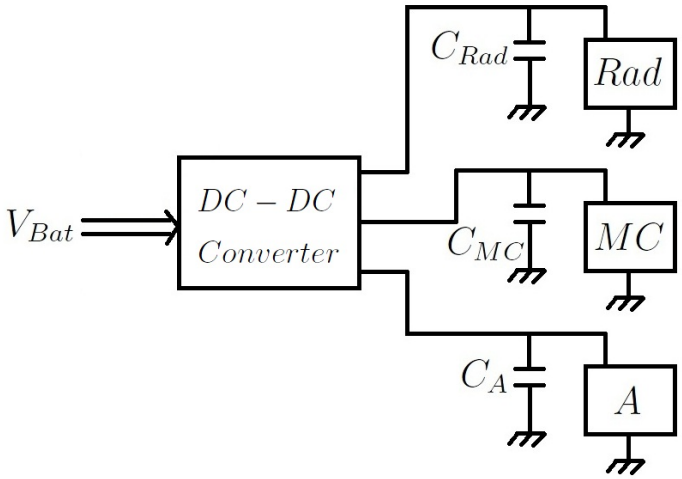


Figure 2.1 - The DC-DC converter must supply three consumers from one battery.

The converter must be efficient and its volume must be kept as small as possible. Moreover, the converter should ensure good line and load regulations, i.e. it must keep the output voltage constant when the input voltage or the output current varies.

2.2 Specifications

The system must meet the component specifications of the UCL platform but it would be applicable to others. These specifications are presented in Table 2.1. Both the MC and the radio can operate in active or in sleep mode. The sensor is in active mode or shut down. In sleep mode, the devices are still supplied at a non-zero voltage so that they can perform some task such as keeping data in memory. However, a shut down device does not consume any power.

The microcontroller tolerates an input voltage stable between 0.9 and $1.5V$. However, considering the tradeoff between performance and consumption, it works in preference between 0.9 and $1.2V$. The MC admits a ripple of about $20mV$ on its supply voltage.

The analogical sensor [31] operates with a supply voltage close to $0.7V$ and consumes around $1\mu W$ in active mode. It presents a maximum sampling rate of $7kS/s$ with 8 bits samples, giving a maximum data rate of $56kb/s$.

We had to choose between two available radios. On the one hand, the Semtech SX212 [11] has a bit rate up to $150kb/s$ and a wake-up time from sleep mode shorter than $500\mu s$. It has relatively low power consumption in receiver

	V_{min} $[V]$	V_{max} $[V]$	P $[\mu W]$	Data rate $[kb/s]$
MC				
Active	0.9	1.5	200	-
Sleep	0.9	1.5	1	-
Radio SX212				
Receiver	2.1	3.6	$6.3e^3 - 12.6e^3$	
Transmitter	2.1	3.6	$33.6e^3 - 75.6e^3$	$25 - 150$
Sleep	2.1	3.6	$0.21 - 7.2$	
Radio CC1101				
Receiver	1.8	3.6	$25e^3 - 59.4e^3$	
Transmitter	1.8	3.6	$27e^3 - 54e^3$	$0.6 - 600$
Sleep	1.8	3.6	$0.36 - 3.6$	
Sensor				
Active	~ 0.7		1.1	56
OFF	-		0	

Table 2.1 - Specifications of each component

mode. On the other hand, the Texas Instrument CC1101 [12] has a data rate from 0.6 to $600kb/s$ and a startup time from sleep to active mode of $t_{start-up} = 240\mu s$. During this startup time, the radio consumes as in active mode but it does not send information yet. Although its receiver mode is energy consuming, both its sleep and transmitter modes consume less power than the SX212. Given that this two modes will be the most used in our system, and considering its higher data rate, the CC1101 radio is preferred to the SX212 one.

In transmitter mode, the CC1101 radio presents a gain of $0dB$. In the following, we will consider that it will be in active mode maximum once each hundredth time : $\beta = \frac{1}{100}$. Indeed, the designer should ensure that the microcontroller consumes more on average than the radio; communication is indeed more power consuming than data processing as explained in section 1.1.3.

The amount of data to send with the radio strongly depends on the application. Indeed, depending on the case, the sensor works either all the time, either sporadically. Moreover, the information from the sensor must sometimes be sent entirely whereas, at some other time, the microcontroller can process it, e.g. it could just send an alert when a problem is detected. Let's consider two examples. In [40], the authors present a system using a temperature sensor. They consider a typical sensing application in which the sensor take measurements once every 10 minutes with a resolution of 8 bits, giving a data-rate of $0.0133b/s$. In [39], the authors consider a 18-channel EEG monitoring system and compare the cases of local biomarker extraction to complete wireless EEG transmission. In the case of wireless EEG without processing, the radio transmitter power dominates

while the data rate reaches $43.2kb/s$. They reduce this transmission data-rate by a factor of over forty by proceeding local feature extraction. The achieved data-rate is $1kb/s$ and the remaining radio power is therefore no longer dominant.

Considering the sensor bandwidth, we impose a use-time of the radio equal to $t_{use} = 5ms$, so, the charge time must be smaller than $t_{charge} < t_{use} \cdot \beta = 500ms$. Working at a data rate of $200kb/s$, the radio can send up to around $\frac{200kb/s}{\beta} = 2kb/s$; this limits the practical applications of the converter. A timing scheme of the power consumption of the system is presented in Figure 2.2. The active period of the radio is limited to $5ms$. During this period $1kb$ can be sent. If all the information of the sensor must be sent out, this means that it can work up to $18ms$ per radio use-cycle of about $500ms$, i.e. until the sum of its use times equal $18ms$. So, in this case, the sensor can operate more than 3% of the time. By processing this information, one can reduce the use-time of the radio and/or increase the use-time of the sensor.

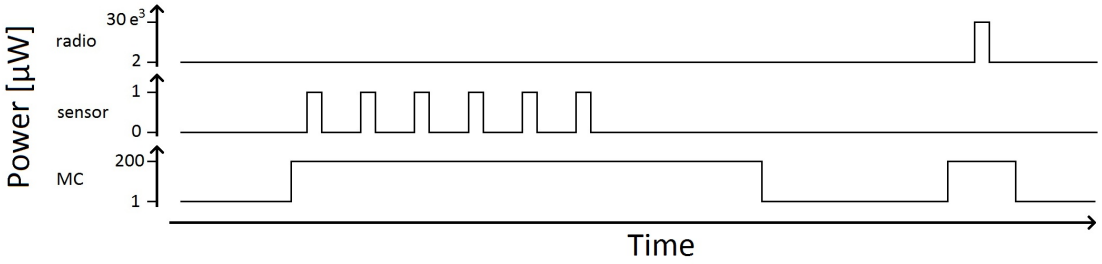


Figure 2.2 - Timing scheme

2.3 Single Output Converters : 3Conv

Many solutions are conceivable to supply different outputs, the simplest one is to use one converter per output. Figure 2.3 depicts a system that supplies three outputs with three converters. Those converters can be of the same type, i.e. three Single Inductor (SI) converters or three Switched Capacitor (SC) converters, or one can combine SI converters and SC converters in the system. All the converters work separately and so do their control circuits. The control scheme is then very simple but the consumed area is quite important. This solution does not allow the system to take advantage of the fact that some outputs are in sleep mode when others are in active mode. In the following, more elaborate solutions will be presented while keeping this solution as a reference.

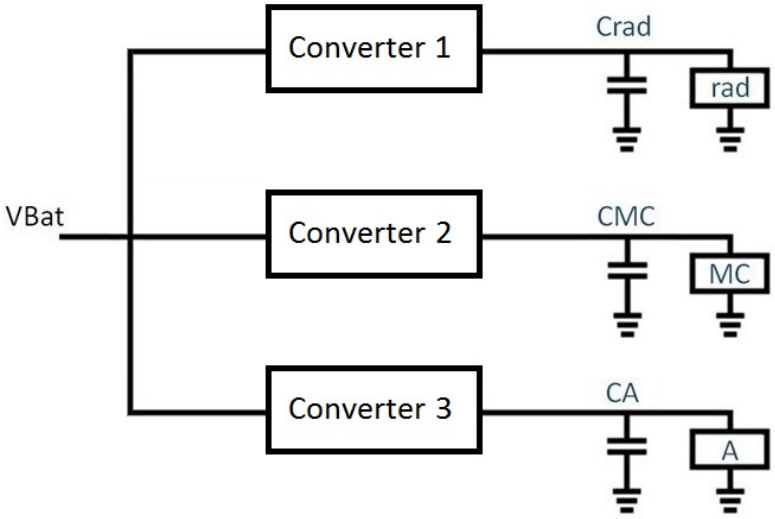


Figure 2.3 - 3Conv : One converter is used per output.

2.4 Single Inductor Converters

Two interesting implementations using an inductor will be studied in this section. The first one only uses the inductor to power the three outputs whereas the second one combines the inductor with a capacitor network.

2.4.1 One Inductor Solution : 1I

Figure 2.4 presents a solution using one inductor to power the three outputs. This circuit includes both a boost converter and two buck converters that all share the same inductor. The buck and boost converters were presented in section 1.2.1. The boost converter uses switches 1, 3, 5 and the diode 1 to supply the radio at a higher voltage. The buck converters use switches 1, 2, 4 and the diode 1 to supply the microcontroller and the analogical sensor at a lower voltage than that of the battery.

This regulator should work in DCM to decrease the cross regulation, as explained in section 1.2.1. It means that the inductor current must return to zero before a new pulse is generated so that the output supplied at the previous step does not influence the current power transfer.

- ⊕ Simplicity of the converter : it only uses one transfer component and 6 switches.
- ⊖ Complexity of the control circuit that must avoid cross regulation.

In spite of the converter simplicity, its size remains rather large. Concerning C_{MC} and C_A, the voltage ripple is critical whereas the stored energy is critical for C_{rad},

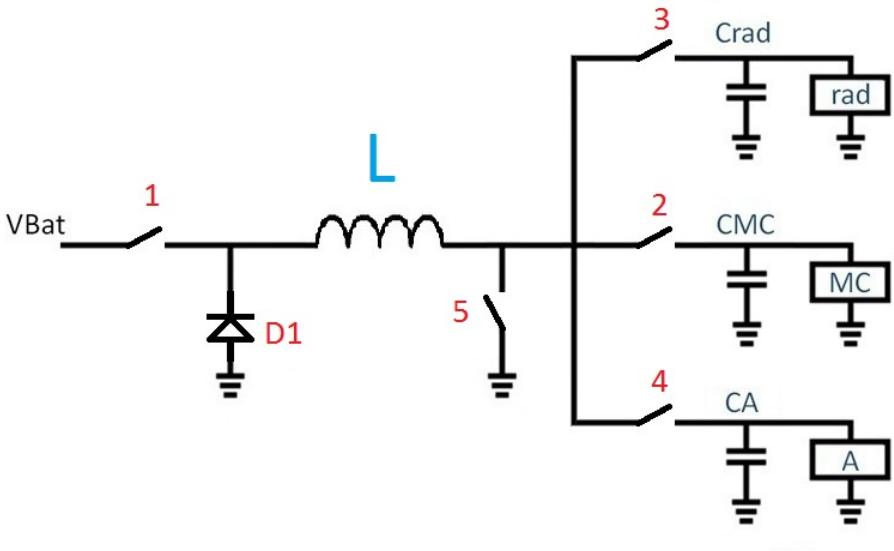


Figure 2.4 - 1I : The inductor supplies the three outputs.

that will be explained in section 3.2.1. In consequence, a higher power transfer means that a lower C_{rad} but larger C_{MC} and C_A are required. In other words, the more power the converter can transfer, the less energy C_{rad} must store.

- ⊕ C_{rad} ↘
- ⊖ C_{MC} and C_A ↗
- ⊖ Low quality factor of the inductor : consumed area ↗

2.4.2 Switched Capacitor with Inductor : Cap-Ind

As the radio has a far higher consumption than the other consumers, it seams interesting to use an inductor to supply it in active mode whereas a Switched Capacitor Network (SCN) is used to supply the microcontroller (MC), the sensor (A) and the radio when the latter is in sleep mode, cf. Figure 2.5. Concerning the power supply of the MC and the sensor, the operating principle is the same as that of the switched capacitor proposed in section 2.5.1. Concerning the supplying of the radio, the SCN maintains the output voltage in sleep mode, i.e. when the power consumption is low, while the inductor is used to raise this voltage and to provide the radio during its active phase, i.e. when the the power consumption is high.

As the power transferred to the radio is higher, C_{rad} must store less energy before the radio enters in active mode. The charge time of this capacitor is accordingly smaller. As the transfer capacitor C_{T1} does not have to supply both the MC and the radio in active mode, it can be smaller. The ripple induced on C_{MC}

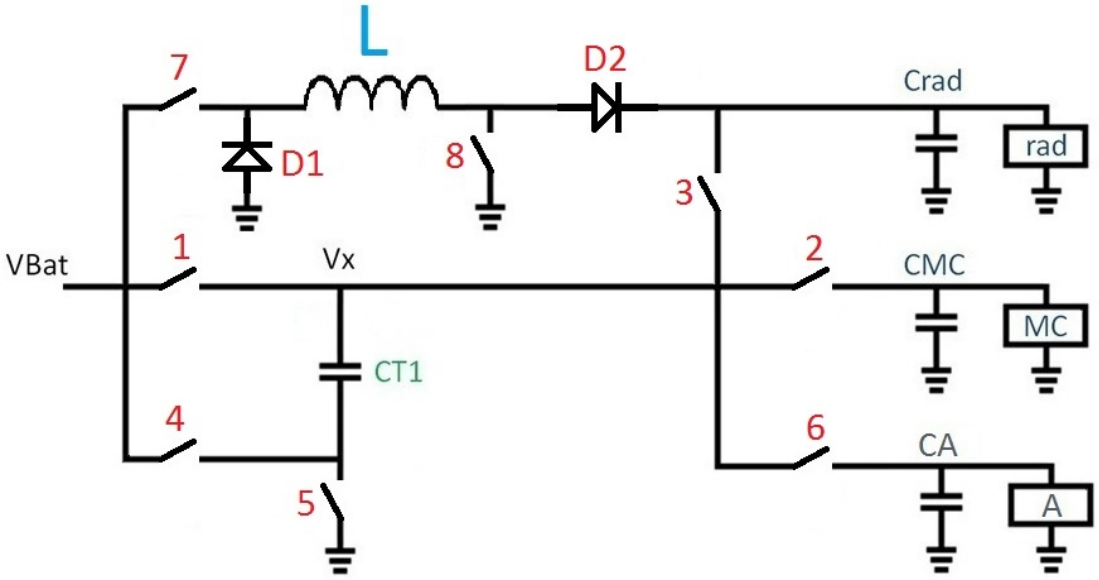


Figure 2.5 - Cap-Ind : The inductor supplies the radio in active mode.

and C_A is then reduce so that they can be smaller, too. Since two different transfer devices are used in this solution, the complexity of the control system is higher.

⊕ C_{rad} ↘ and t_{charge} of C_{rad} ↘

⊕ C_{T1}, C_{MC} and C_A ↘

⊖ Complexity of the circuit and of the control system ↗

⊖ Low quality factor of the inductor : consumed area ↗

2.5 Inductorless Converters

There are also many way to build a converter without any inductor. In this section, we will compare different switched capacitor circuits that power the radio, the microcontroller and the sensor. The simplest way is again to use one transfer capacitor converter for each output. The control circuitry is accordingly quite simple, but the consumed area is important. As stated in Equation 1.5, the power transferred to the output can be modulated by varying the transfer frequency or the total transfer capacitor. We will therefore consider two circuits that use one of these methods.

2.5.1 Switched Capacitor Converter with Three Outputs : 1CT

The converter presented in Figure 2.6 uses one transfer capacitor C_{T1} to power the three outputs. The microcontroller (MC) and the analogical sensor (A) both require a voltage lower than V_{bat} whereas the radio (rad) require a higher voltage, so, we can distinguish two different ways to operate the charges transfer. When supplying the microcontroller or the analogical sensor, the bottom plate of C_{T1} is connected to the ground, i.e. switch 5 is passing whereas switch 4 is blocking. Then, when switch 1 is passing, C_{T1} is charged and it gives its charges to the output when switch 2 or switch 7 is passing. When supplying the radio, C_{T1} is first charged, i.e. switches 1 and 5 passing. Second, all the switches but switch 4 are blocking which means that the bottom plate capacitance of C_{T1} is raised to V_{bat} so that V_x raises to two times V_{bat}. Third, the charges are transferred from C_{T1} to C_{rad} through switch 3.

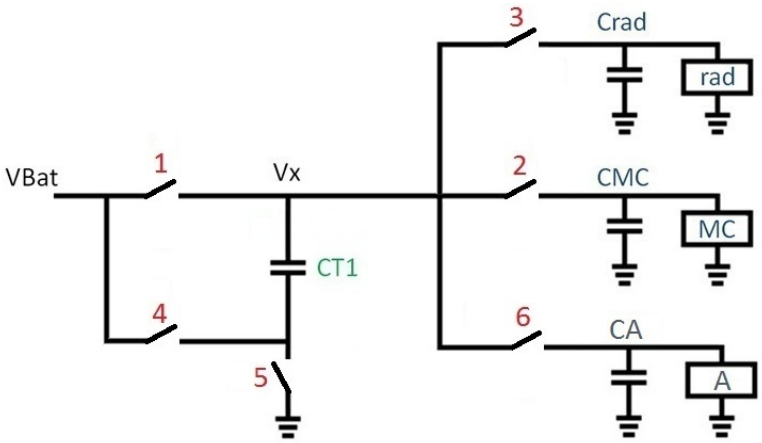


Figure 2.6 - 1CT : One transfer capacitor is used to supply the three outputs.

As this solution does not use any inductor, on chip integration is facilitated. However, this also implicates that a bigger capacitor is required to store the energy that is consumed by the radio in active mode. The control of this circuit is relatively simple insofar there is only one transfer device and few switches.

- ⊕ Simplicity of the converter : it only uses one transfer component and 6 switches.
- ⊕ Relatively easy control : According to Equation 1.5, the transferred power can be regulated by varying the frequency of the charges transfers.
- ⊕ Good on chip integration.
- ⊖ C_{rad} ↗ and t_{charge} of C_{rad} ↗
- ⊖ Loss in switches ↗ ???

2.5.2 Switched Capacitor Converter with parallel transfer capacitors : 3CT

The switched capacitor converter presented in Figure 2.7 uses three transfer capacitors to supply the outputs. The number of transfer capacitors N could be different : $N = 3$ is just taken as an example. As in the previous solution, charges are transferred to the outputs using transfer capacitors. The mean difference resides in the fact that the power is now regulated by changing this transfer capacitor instead of varying the frequency. The transfer capacitor is split in smaller ones and the control system must specify the number of capacitors to use depending on the output power to deliver : $C_T = \sum_i C_{Ti}$.

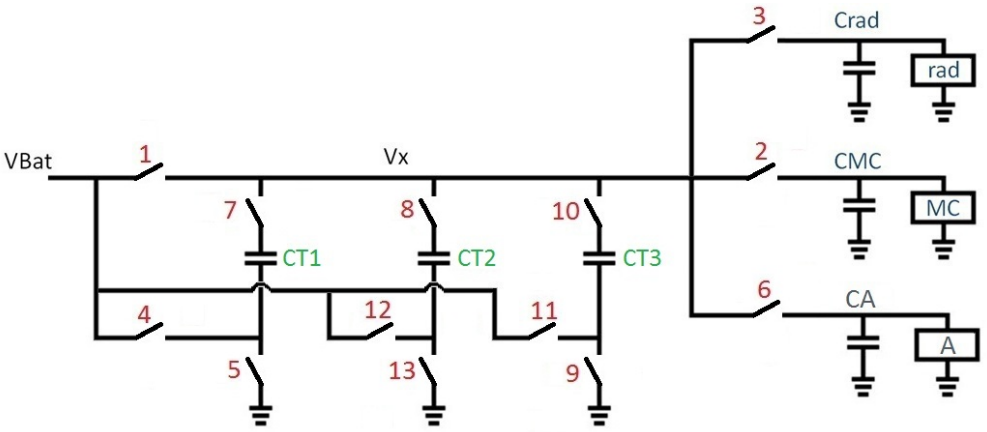


Figure 2.7 - 3CT : The control circuitry determines the number of capacitors to use.

The total transfer capacitor C_T will be the same as the unique transfer capacitor of the previous solution so that the system is still operational in the worth case, i.e. when the required output power is the highest. The size of the switches is also divided so that the global size of this converter slightly larger.

This technique aims at keeping switching losses proportional to the output current I_{out} without modifying the switching frequency. The conduction losses are unchanged. As the control circuit selects just the appropriate transfer capacitor, the amount of bottom-plate losses as well as driving losses, scale with the output power. This results in an increased efficiency.

- ⊕ Switching losses proportional to the output current.
- ⊕ Good on chip integration.
- ⊖ C_{rad} ↗ and t_{charge} of C_{rad} ↗
- ⊖ Control complexity ↗ : number of switches and of transfer elements ↗

We can imagine to extend this concept by splitting the entire SC converter into smaller ones sharing the same input and output capacitors. This way, by using them separately, we combine the transfer capacitor size modulation and the power switches size modulation. A further extension should be to use phase shifted clocks to command each small SC converter. The main purpose of this is to reduce ripple magnitude on the output voltages. In fact, the charge packets sent to the output are smaller and more equally distributed on time allowing one to reduce the size of the output capacitors for an equivalent ripple. Furthermore, the ripple induced on the input current becomes smaller, too.

2.6 Comparison of the Proposed Converters

Main advantages of solutions with inductor are the diminution of the radio output capacitor and that of its charge time. However, it requires an inductor that is difficult to integrate on chip. Moreover, the current flowing through that inductor increases the ripple on C_{rad} and, this way, the radio consumption.

size, efficiency, complexity, quality (ripple etc.)

Comparison of the converters					
Figure of merit	3Conv	1I	Cap-Ind	1CT	3CT
Efficiency	0				+
Size	0	+	+	+++	++
Complexity	0	+	-	++	-
Output range	0	+	+	-	-
Output quality	0	- -	-	+	++

Table 2.2 - The solution using three separate converters is taken as a reference.

2.7 Conclusion of the chapter

In this chapter we have investigated different energy management solutions applicable in EASs. This analysis of the different alternatives has allowed us to imagine the circuit proposed in this work.

Full integration is the main advantage of inductorless solutions because of the volume constraints in EASs. Higher charge time and higher losses in the switches due to the more frequent switching are contrariwise drawbacks that must

be considered.

It is clear from this study that the interest of combining converters grows as the number of outputs increases. This is especially interesting in systems where the outputs are not used at the same time, e.g. in multi-sensor nodes where the sensors operate successively. The worth case that determines the size of the transfer devices is indeed less constraining if the outputs do not require power simultaneously.

In the next chapter, ...

CHAPTER 3

Design of the Proposed Solution

The converter has to provide power to a microcontroller (MC), a radio (rad) and an analogical sensor (A). Both the MC and the radio can operate in active or in sleep mode. The sensor is in active mode or shut down. The consumers follow the specifications given in section 2.2. The assumption is made that an external clock close to $20MHz$ and the reference voltages used by the comparators are available.

Based on the comparison presented in section 2.6 we chose to study a switched capacitor DC-DC converter. The good on-chip integration of these converters allows us to limit the consumed area. As the transferred power varies between the different outputs, we decided to work with two transfer capacitors as explained in section 3.2.

We want to design a power management system that exploits idleness in an efficient way by shutting down the idle devices and by keeping them in a state where the power dissipations are as low as possible. Whenever the device exits its idle state, the transition from shut down to active should be both efficient and fast.

3.1 Operating principle

Figure 3.1 introduces the topology of the proposed Switched Capacitor Network (SCN) DC-DC converter. The capacitor network connects the battery to the three outputs. Each output voltage is compared to a reference voltage by a comparator. Those reference voltages depend on the operating mode chosen by the MC. The control circuitry generates the gate signals (GS_x) of the switches of

the capacitor network depending on the output of each comparator. The capacitor network and the control system will be detailed in sections 3.2 and 3.3 respectively.

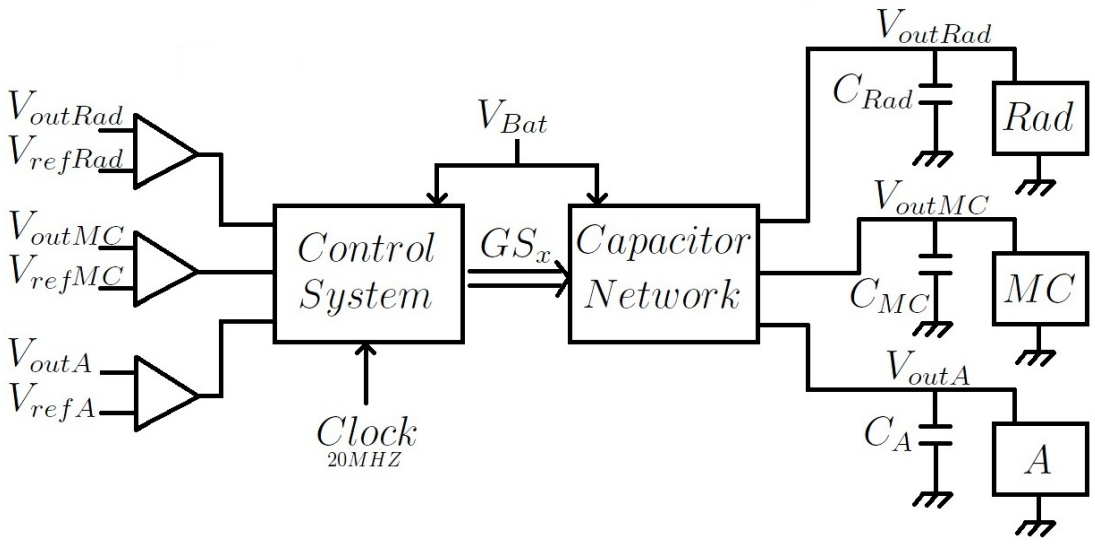


Figure 3.1 - The control system takes the information from the comparators to generate the command signals of the capacitor network that links the battery to the consummers.

3.2 Capacitor network

The capacitor network shown in Figure 3.2, includes 2 transfer capacitors, C_{T1} and C_{T2}, and 8 switches to activate the pathways through which the charges will pass. C_{T1} supplies the microcontroller (MC) in active mode and the radio (rad) whereas C_{T2} supplies the microcontroller in sleep mode and the sensor (A). The operations executed in each of the modes will be detailed in section 3.3.

C_{T1} is charged when transistors 1 and 5 are made passing. It can then transfer its charges either to the MC, either to the radio. To supply the MC, transistor 2 is opened and transistor 5 stays open. The radio requires a voltage higher than the input voltage, the charges stored on C_{T1} are therefore mounted up by opening transistor 4 after closing transistor 5. Afterward, transistor 3 let pass the charges toward C_{rad}.

C_{T2} is charged when transistor 7 is passing. In a second time, it can transfer the charges either to the sensor, either to the MC. The power transfered by this capacitor is just sufficient to power the MC in sleep mode, through transistor 8. If the MC is in sleep mode, C_{T1} just has to supply the radio : the charge time is therefore reduced in this case. As C_{T2} is smaller, the charge packets sent to the sensor are also smaller, which helps limit the voltage variations on C_A.

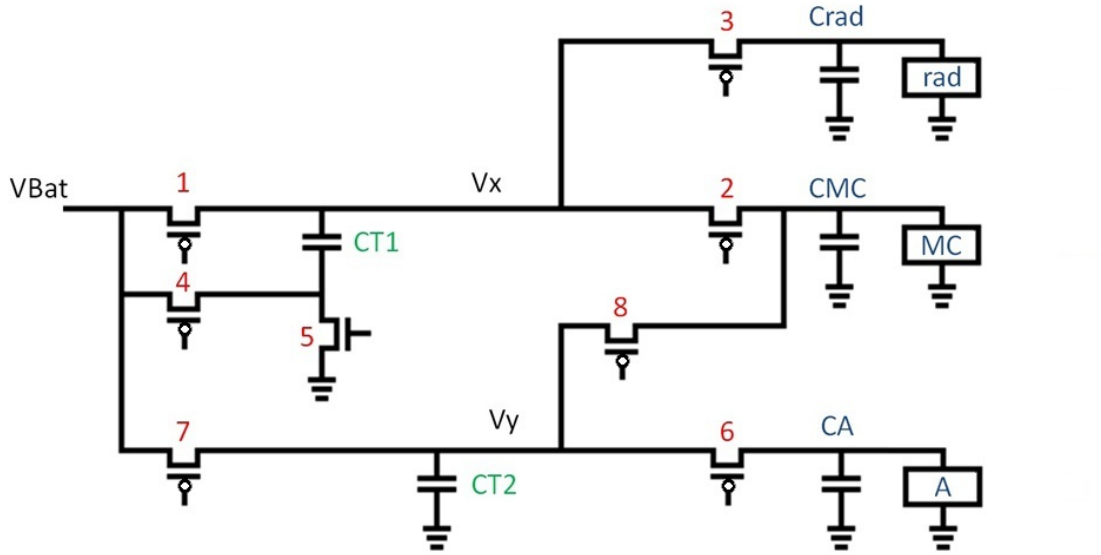


Figure 3.2 - Capacitor network

3.2.1 Design of the switches and capacitors

All the capacitors and switches must be designed so that the specifications are respected, e.g. the output voltage ripple. A rough sizing of those components is presented in this section. The corresponding Matlab code is provided in appedix C.

VOIRE PRESENTATION 2 POUR IDEES SUPPLEMENTAIRES.

Output capacitors

The output capacitors must be large enough to limit the voltage ripples. In other words, they must be able to store enough energy to supply their respective output before the next charges supply. Table 3.1 shows the output capacitors in parallel with the voltage ranges for each output.

Calculation of the output capacitors				
		V_{begin} $[V]$	V_{end} $[V]$	C_{out} $[pF]$
Radio		2.5	2	$160e^6$
MC	high ripple	1.2	1	200
	low ripple	1.02	1.00	$3e3$
Sensor	high ripple	0.75	0.7	5
	low ripple	0.71	0.7	22

Table 3.1 - Output capacitors depending on the tolerated ripple

C_{rad} is much more bigger than the two others because it has to store more energy to supply the radio. Because of its size, that capacitor will not be integrated on-chip. Concerning the microcontroller and the sensor, two values for the output capacitors were presented depending on the tolerated ripples. To meet the ripples specifications, one needs either a large enough output capacitor or a voltage stabilizer as a low-dropout regulator (LDO). A larger capacitor requires a longer charge-time and consumes more area whereas a LDO presents static power consumption ($0.25\mu W$, [31]) and an efficiency limited to the ratio $\frac{V_{out}}{V_{in}}$. Furthermore, a LDO can only stabilize a higher voltage to V_{ref}. We thus chose to work without LDO and to use capacitors of $C_{rad} = 160\mu F$, $C_{MC} = 3nF$ and $C_A = 22pF$.

Transfer capacitors

The total transfer capacitor C_T is designed to achieve the desired transferred power P_{load} as explained by Equation 1.5 in section 1.2.2 :

$$C_T = \frac{P_{load}}{f_s V_{out} \Delta V} \tag{3.1}$$

The minimum transfer capacitors are calculated for each possible operating condition and the results are presented in Table 3.2. The MC and the radio are either in active or in sleep mode. The sensor is either in active mode or shut down. A duty cycle represents the proportion of time alloted to each output; it takes into account that the other outputs also require charges or not. A duty cycle of 1 means that only one output needs to be supplied, so, the capacitor network devotes 100% of its time to power this output. A duty-cycle of 2 means that two of the outputs require charges, so, the system alternatively supplies each one of the two, and so on.

Calculation of the transfer capacitors				
Duty Cycle	Mode	C_{TMC} $[pF]$	C_{Trad} $[pF]$	C_{TA} $[pF]$
1	Active	33.3	16.9	0.0893
	Sleep	0.166	0.050	0
$\frac{1}{2}$	Active	**66.6**	**33.8**	0.179
	Sleep	0.333	0.100	0
$\frac{1}{3}$	Active	100	50.7	0.268
	Sleep	0.500	0.150	0

Table 3.2 - Transfer capacitors must ensure sufficient power transfer.

With the chosen topology, the mode with a duty-cycle of $\frac{1}{3}$ is never used as the sensor was placed on another path than the radio one. Moreover, we

impose that the radio and MC are always in sleep and active mode respectively when the sensor is working. On the one hand, the MC has to read the data from the sensor and on the other, the radio in active mode has the largest power use, so, to avoid inflating the peak power, the sensor is used at another time.

Based on these results, we chose to work with two different transfer capacitors in our network : one capacitor $C_{T1} = 70pF$ that supplies the MC and the radio and one smaller capacitor $C_{T2} = 0.4pF$ that supplies the sensor and the MC. The critical values are enclosed into framed boxes. It seems from Table 3.2 that C_{T2} is sufficient to power the MC in sleep mode.

Power switches

The switches should be as small as possible while enabling the transfer of 90% of the charges within the allotted time; bigger switches would let pass more charges but one would lose this advantage by charging and dicharging bigger grids, leading to higher switching losses.

3.3 Control system

Depending on the tasks to be accomplished, the microcontroller defines the reference voltages, from Table 3.3. It will for example, order the charge of C_{rad} when data must be sent. The reference voltages are chosen into the ranges presented in section 2.2, they are presented in Table 3.3. The reference voltage of the MC is taken relatively low to limit its consumption while conserving the wished performances. However, the active mode reference voltage of the radio is higher due to the compromise with the size of C_{rad} calculated in section 3.2.1 : a lower reference voltage would beget a larger output capacitor.

Reference Voltages		
Mode	Active	Sleep
Radio	$2.5V$	$2V$
MC	$1V$	$1V$
Sensor	$0.75V$	$0V$

Table 3.3 - The reference voltages are chosen by the microcontroller.

The different operating modes of the capacitor network are presented in Table 3.4 while the operations done in each mode are explained later in this section.

MC	Radio	Sensor	V_{rad}-V_{ref}	V_{MC}-V_{ref}	V_A-V_{ref}	Modes
A	A	S	$<$	$<$	-	1
				$>$	-	2
			$>$	$<$	-	3
				$>$	-	4
	S	A	$<$	$<$	$<$	5
					$>$	6
				$>$	$<$	7
					$>$	8
			$>$	$<$	$<$	9
					$>$	10
				$>$	$<$	11
					$>$	12
		S	$<$	$<$	-	13
				$>$	-	14
			$>$	$<$	-	15
				$>$	-	16
S	A	S	$<$	$<$	-	17
				$>$	-	18
			$>$	$<$	-	19
				$>$	-	20
	S	S	$<$	$<$	-	21
				$>$	-	22
			$>$	$<$	-	23
				$>$	-	24

Table 3.4 - Modes of the capacitor network. The devices are either in active (A) or in sleep (S) mode and the voltage across their capacitor is either higher ($>$) or lower ($<$) than the corresponding reference voltage.

There are 24 different modes, including 10 from the viewpoint of the capacitor network, which has as consequence that the control circuitry is not simple at all. In order to explain how the converter works, we will detailed the operations performed in each of the modes by giving the roles of both transfer capacitors.

- modes 1, 6, 13 : C_{T1} provides power to the MC and the radio alternatively.
- modes 2, 8, 14, 18, 22 : C_{T1} provides power to the radio.
- modes 3, 10, 15 : C_{T1} provides power to the MC.
- modes 4, 12, 16, 20, 24 : stand-by.
- mode 5 : C_{T1} provides power to the MC and the radio alternatively. C_{T2} provides power to the sensor.
- mode 7 : C_{T1} provides power to the radio. C_{T2} provides power to the sensor.
- mode 9 : C_{T1} provides power to the MC. C_{T2} provides power to the sensor.
- mode 11 : C_{T2} provides power to the sensor.
- modes 17, 21 : C_{T1} provides power to the radio. C_{T2} provides power to the MC.
- modes 19, 23 : C_{T2} provides power to the MC.

Modes 1, 5, 6 and 13 are critical concerning the size of C_{T1} as the capacitor must power both the MC and the radio. Concerning C_{T2}, the supply of the MC is the critical case, i.e. modes 17, 19, 21, and 23. In stand-by, the system charges the transfer capacitors. In mode 5, all the consumers are powered.

Mode 17 allows a faster charge of C_{rad} by putting the MC in sleep mode. This way, C_{T1} is entirely dedicated to the radio, allowing a faster charge of C_{rad}. At the same time, it decreases the period during which we put a higher voltage across C_{rad} and thus the radio consumption.

The implementation of this control system is too complex to let us perform a full custom design. On the same time, the design kit of the technology is not completely installed, making the integration in the layout of a *verilog* code impossible. The *verilog* implementation of the control circuit is nevertheless presented in appendix C. Owing to this mishap, we decided to study in detail a simplified circuit. That is the topic of the next two chapters.

3.4 Area of improvement

The power management method could be extended to be based on the status of the battery and on the current harvested energy. The microcontroller could take this information into account in its choice of the operating mode. It could for example promote power-hungry tasks as RF communication when the battery is fully charged and the system is harvesting energy.

The proposed system is a switching regulator that introduces noise on the output voltages. If one load requires a more stable voltage, with less switching noise, it is possible to increase the size of the corresponding output capacitor or to insert a voltage stabilizer. This system will however not suit for loads requiring a too high stability voltage source because in these cases, the size of the output capacitors as well as their charge time would be too large.

The system must stay operational even when the battery is fully charged. It would therefore be interesting to study the influence of a diminution of V_{bat}, say from 1.5 to $1.2V$, due to the discharge of the battery.

(Cmt amlior le systme ? rseau de caps plus complexe, freq variable, ...) : interleaving (phase differentes) for example :)

As an improvement, we could dynamically adapt the size of the power switches to reduce the gate-drive or the conduction losses. The control circuitry could, for example, take into account the fact that the radio is in sleep or in active mode, and activate the right amount of power switches in consequence.

3.5 Conclusion of the chapter

In this chapter, we investigated the ... ce qu'il faut retenir de ce chapitre.

CHANGER :) The control of the circuit presented in this chapter was too complicated to produce the layout of the system in the alloted time of this Master thesis due to missing tools in the design kit. Because of that, we will study a simplified circuit in next chapter. In that simplified circuit, we only consider a MC and a radio as energy consumers. The conclusions of this simplified study are nevertheless extensible to the complete circuit of this chapter.

CHAPTER 4

Implementation

on mets d'abord ce qui est commun aux deux types (avec et sans ULP). Puis on mets ce qui est propre chaque circuit. On fait 1 layout : si on fait le layout du circuit sans ULP, il faut faire le level shifter. methodologie de test s'applique aux 2.

The realization of the designed circuit with its control circuit will allow us to validate experimentally the concept.

As explained in the previous chapter, the design kit of the technology was not completely installed. It was then not possible to integrate a *verilog* code in the layout, forcing us to draw a full custom circuit. Therefore, we chose to study a simplified scheme for the realization part. The corresponding control circuitry is accordingly more simple to design. That will allow us to realize a layout in order to establish a test methodology to measure the performances of the proposed system.

In this chapter, we will present the simplified topology that will be studied as well as the design methodology of the different parameters used in the circuitry. Then, two implementations of the SC circuit will be investigated and compared; the first one uses classical transistors whereas in the second one, some switches were replaced by Ultra-Low-Power (ULP) transistors. These transistors are introduced in section 4.2.2.

4.1 Operating principle

The operating principle is the same as the one presented in section 3.1 except that we only consider two outputs : the microcontroller (MC) and the radio (rad). The topology of the simplified system is presented in Figure 4.1. In this chapter, we will also consider that the microcontroller always stays in active mode whereas the radio can still be in active or in sleep mode.

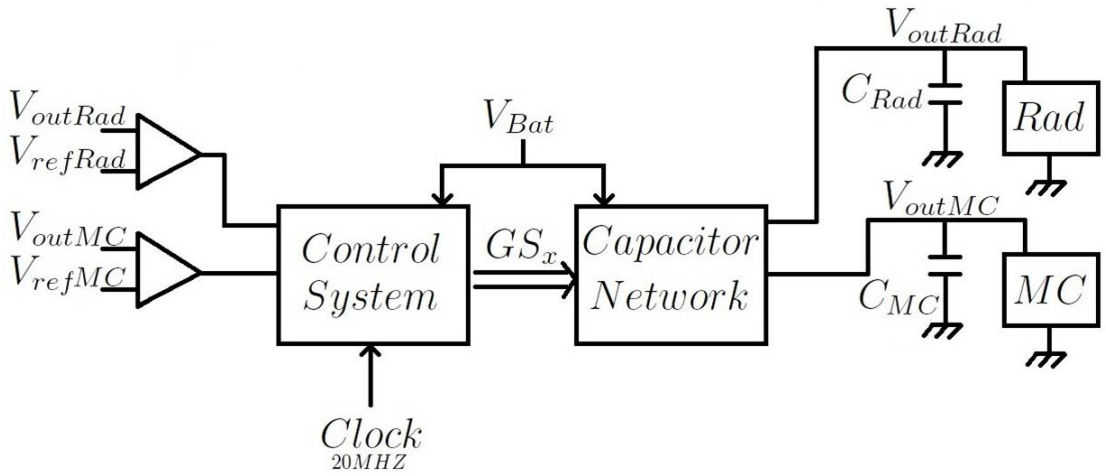


Figure 4.1 - In the simplified system, we only consider the MC and the radio as outputs.

4.1.1 SC network

The circuit of the capacitor network that will be used in the simplified system is shown in Figure 4.2. It employs one transfer capacitor $C_{T1} = 70pF$ to supply both the MC and the radio. For each of the two implementations of this capacitor network that will be studied in this chapter, an implementation has to be chosen for the switches. In section 4.2, various classical MOS transistors as well as ULP transistors will be presented.

4.1.2 Control

The different operating modes are listed in Figure 4.3. The two left blocs represent the modes of the MC and the radio imposed by the microcontroller. The two central blocs summarize the trigger signals, i.e. the comparators outputs. Depending on the mode of the radio and on the comparators outputs, there are eight different modes to consider, they are presented in the right bloc. The reference voltages were defined in Table 3.3 while the operations performed in

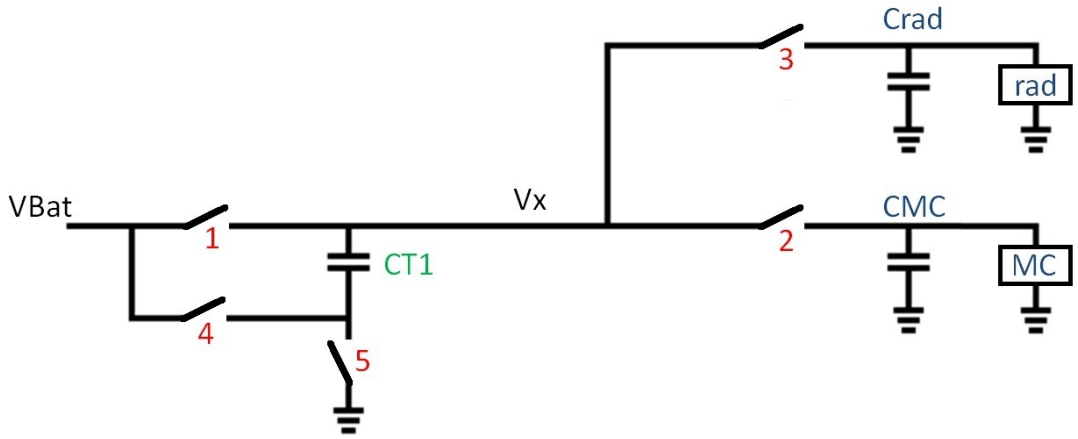


Figure 4.2 - Capacitor network of the simplified system.

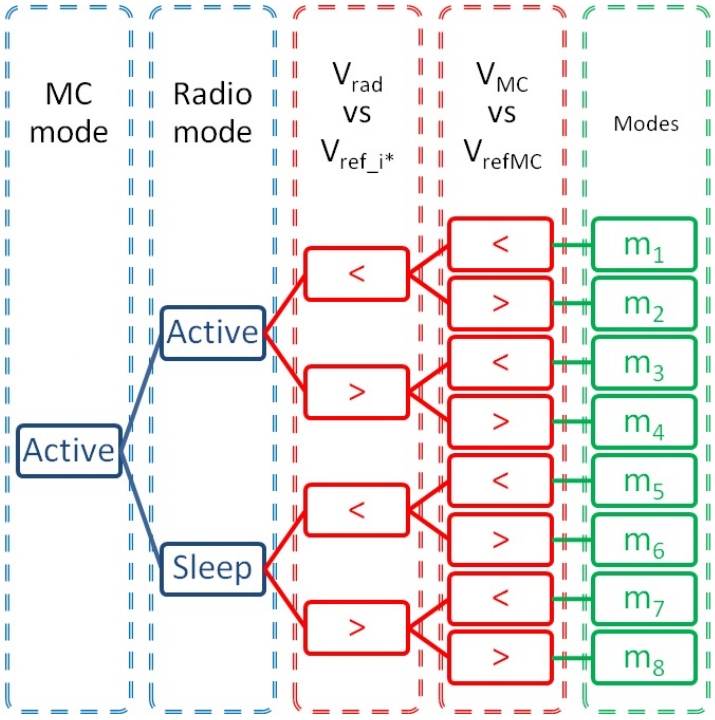


Figure 4.3 - The system will be in one of eight possible modes depending on the modes imposed by the MC and on the triggers from the comparators. $^*V_{ref\_i}$ is the reference when the radio is in mode i.

each mode were explained in section 3.3.

The comparators will provide a trigger signal of 1 if $V_{out} < V_{ref}$. From the SC network point of view, there are actually only four different modes to consider, depending on the trigger signals, as presented in Table 4.1. The SC network just takes the trigger signals into account, i.e. the fact that an output requires charges, but it does not need to know the mode in which is the corresponding device. In mode 1, both the radio and the MC require energy. In mode 2 and 3, the management system has respectively to provide the MC or the radio. In mode 4, the system is in stand-by and no energy is transferred.

ENMC	ENRX	m_1	m_2	m_3	m_4
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table 4.1 - Four different modes depending on the trigger signals.

In the control part, we will use non-overlapping clock generators and comparators. They are defined as per the following.

Non-overlapping clock generator

A Non-Overlapping Clock (NOC) bloc, as shown in Figure 4.4, takes a clock signal as input and returns this signal and its inverse without overlapping. The non-overlapping period is determined by the delay introduced by the inverter chain. This chain must be composed of an even number of inverters. The more inverters are used, the longer will be the delay, but this also means that one loses a greater part of the useful time. The NOC bloc is used in the control circuits to prevent some switches from switching at the same time, as explained in sections 4.3.2 and 4.4.2.

Comparators

Comparators capable of detecting relatively small voltage differences are needed in order to maintain the ripples on the output capacitors in the alloted ranges. Two different implementations were studied : one based on a clocked comparator and the other using a double stage amplifier.

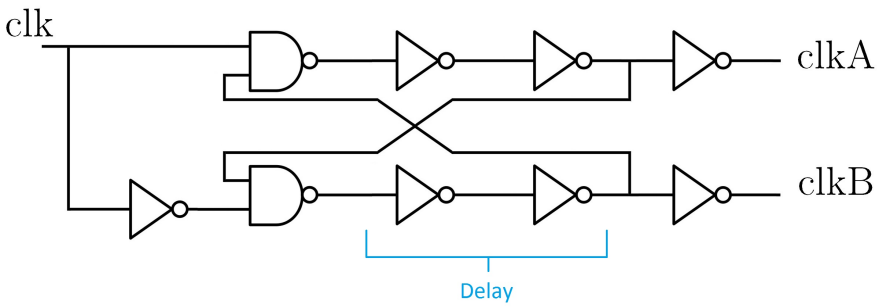


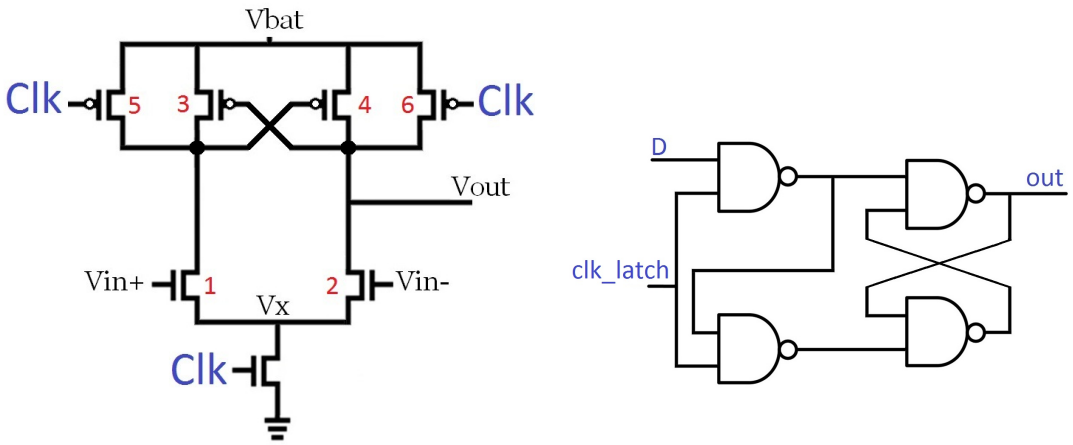
Figure 4.4 - A non-overlapping clock generator (NOCG) generates two non-overlapped clock signals.

The first solution to limit the power consumption is to use a clocked comparator, as presented on figure 4.5(a). In this case, the comparison is performed at a given time controlled by the clock signal clk. During the $\overline{clk}$ phase, transistors 5 and 6 precharge the output at the desired logic signal V_{bat}. During the clk phase, a positive feedback is enabled and the output reaches a stable state. This stable state depends on the unbalanced currents flowing in transistors 1 and 2 as explained below :

$$(V_{in-} > V_{in+}) \Rightarrow (I_2 > I_1) \Rightarrow V_{out} \searrow \Rightarrow I_3 \nearrow \Rightarrow V_{G4} \nearrow \Rightarrow I_4 \searrow \Rightarrow V_{out} \searrow \ldots \quad (4.1)$$

$$(V_{in-} < V_{in+}) \Rightarrow (I_2 < I_1) \Rightarrow V_{out} \nearrow \Rightarrow I_3 \searrow \Rightarrow V_{G4} \searrow \Rightarrow I_4 \nearrow \Rightarrow V_{out} \nearrow \ldots \quad (4.2)$$

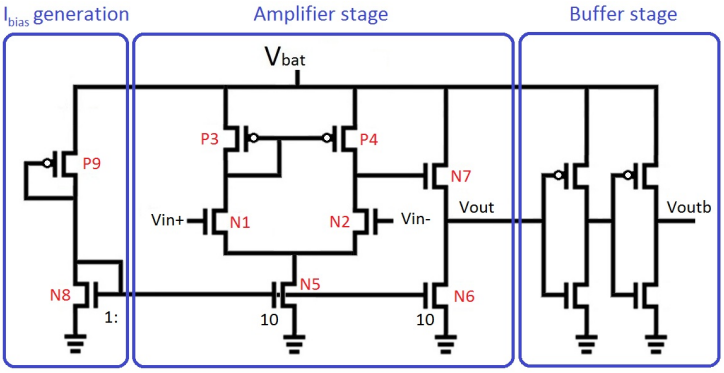
Thanks to the positive feedback loop, the response time is very short even with small input signals. The output of the comparator is discontinuous because it is precharge at each $\overline{clk}$ phase. A latch must be used to keep the signal continuous which complicates the system. The circuit of the designed clocked comparator is shown in Figure 4.5(a) and the circuit of its latch in Figure 4.5(b).



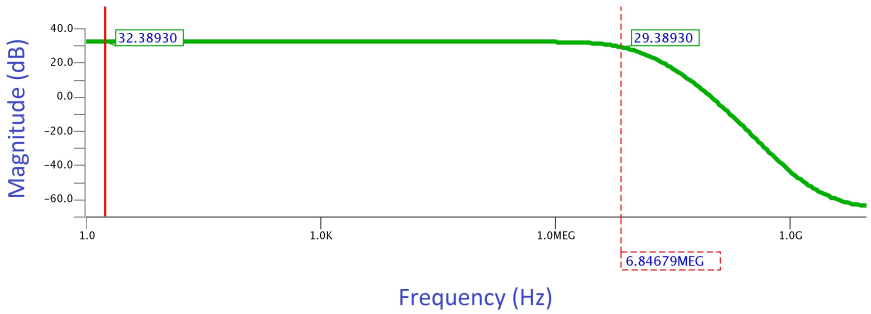
(a) Clocked comparator. (b) Latch.

Figure 4.5 - The clocked comparator is combined to a latch so as to have a continuous output.

An alternative is to use a double stage amplifier, cf. Figure 4.6(a). The voltage difference between the inputs is amplified with a certain gain :the frequency characteristic is presented in Figure 4.6(b).



(a) Double stage amplifier with I_{bias} generation and buffer stage.



(b) Frequency characteristics of the comparator : $V_{out}(f)$

Figure 4.6 - A double stage amplifier is used as comparator.

The current source is composed of a long PMOS transistor and of a long NMOS transistor. Transistors 5 and 6 are 10 times shorter than transistor 8 in order to consume more power in the useful part of the comparator. The current imposed in the first two stages is approximately equal to $180nA$ at $25C$. The DC gain of the comparator reaches $32.39dB$ and its bandwidth exceeds $6.8MHz$ for a consumption of $0.6\mu W$. Moreover, the outputs of the comparators are passed into buffers in order to ensure a clean logic signal. The transistors that compose each buffer have a relatively high length so as to reduce their power consumption. Indeed, their input voltage is generally close to the middle of the dynamic because the compared voltages are not far from each other, leading to static consumption in the output buffer. So, to mitigate this consumption we use longer transistors in the buffer.

For an equivalent resolution, the designed clocked comparator with its latch requires a higher power than the double stage amplifier with its buffer. The last one will then be used in the following.

4.1.3 Clock generation

In this section, we will explain how the clocks used in the control circuit are generated from the external $20MHz$ clock. The clock generation is depicted in Figure 4.7. In this bloc, we use two Non-Overlapping Clock generators and frequency divider that will be presented in the following.

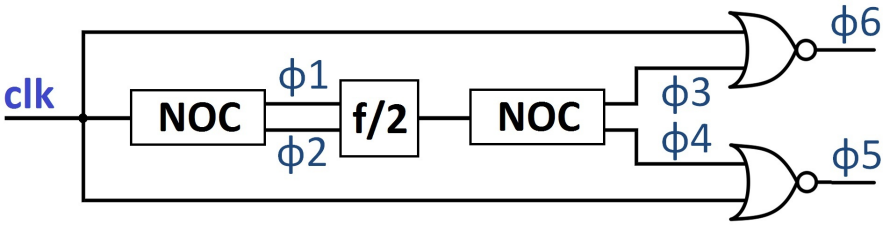


Figure 4.7 - Generation of the clocks.

The generated clocks are shown in Figure 4.8. Clock signals Φ1, Φ5 and Φ6 will be used in the control circuitries presented in sections 4.3.2 and 4.4.2. The others are just intermediary signals used to generate them.

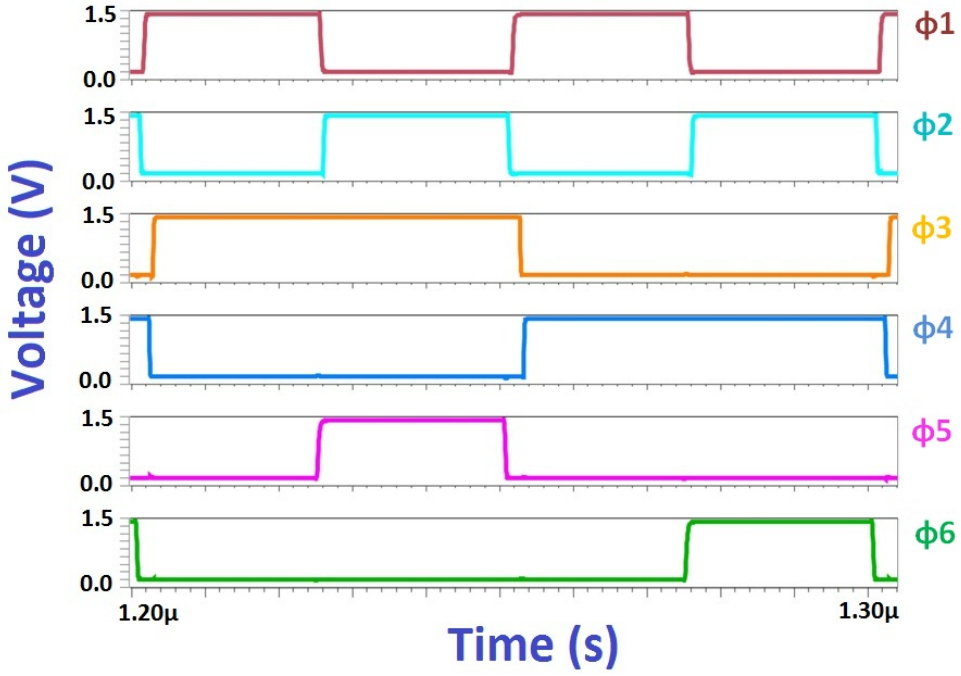


Figure 4.8 - Clocks generated from the $20MHz$ clock.

Frequency divider

Signals of half-frequency are required to generate clock signals Φ5 and Φ6. As presented in Figure 4.9, the frequency divider is composed of a register combined to an inverter. It takes a clock (clk) as input and returns another clock (Q) of half the frequency. The value of Q is indeed inverted at each rising edge of clk.

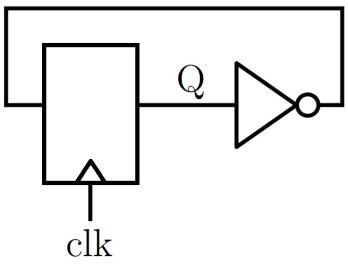


Figure 4.9 - The frequency divider bloc returns a clock signal with half the original frequency.

The scheme of the used register is presented in Figure 4.10 while the layouts are presented in Appendix D.

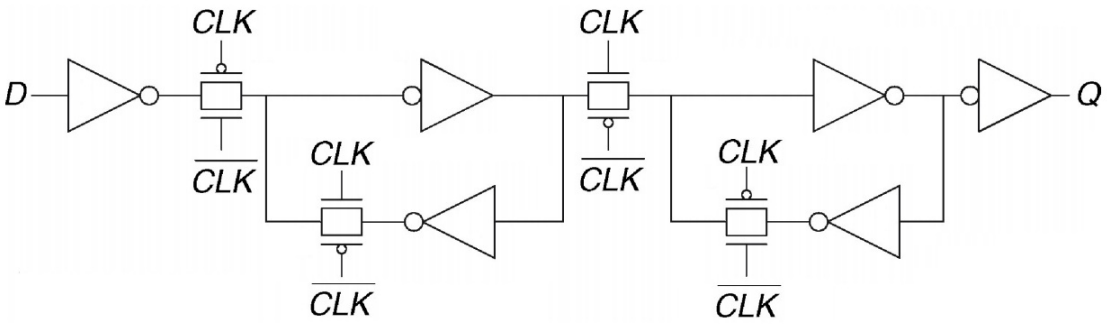


Figure 4.10 - Scheme of the register used in the frequency divider.

4.2 Choice of the Transistors

In this section, we will compare the different transistors proposed in the design kit of the TSMC 250 technology. In addition, we will introduce the Ultra-Low-Power (ULP) transistors.

4.2.1 Classical transistors

Various transistors, of different sizes and voltage limits, are available in the $TSMC$ 250 technology. Table 4.2 and Table 4.3 compare the transistors that could be used for the logic and power parts of the circuit respectively. In this technology, there are different types of $2.5V$ transistors but only one type of $5V$ transistors, which will therefore be used when voltage differences greater than

$2.5V$ must be supported. $5V$ transistors present a thicker gate, a higher threshold voltage and their minimum length is longer. Concerning the other switches, a comparison of the different types of $2.5V$ transistor is necessary. The results are presented in Figures 4.11 and 4.12 and in Tables 4.2 and 4.3.

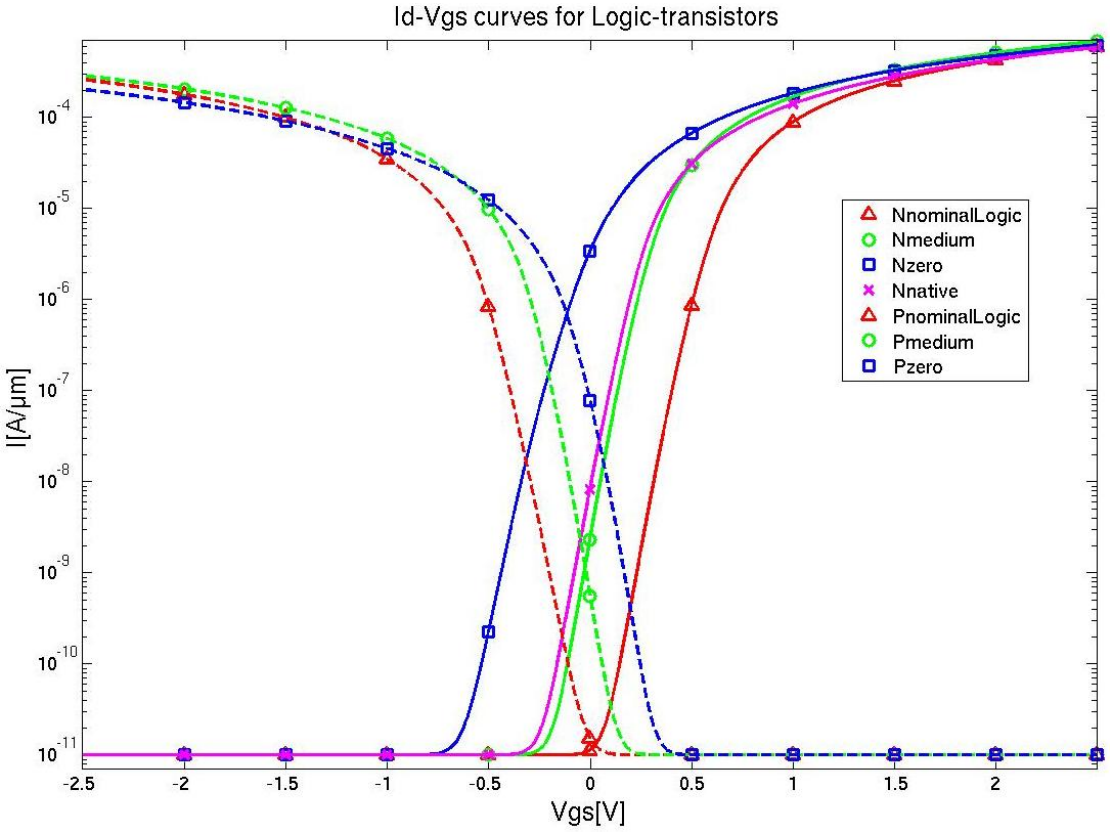


Figure 4.11 - $I_d - V_{gs}$ characteristics for $W = 0.5\mu m$, $L = L_{min}$, $T = 25°C$, $V_G = [-2.5; 2.5V]$, $V_{Dn} = 2.5V$, $V_{Sn} = 0V$, $V_{Bn} = 0V$, $V_{Dp} = -2.5V$, $V_{Sp} = 0V$, $V_{Bp} = 0V$. The solid lines represent the N-MOS transistors whereas the dashed lines represent the P-MOS transistors.

Of all the transistors that could be used in the logic part of the circuit, the nominal V_T transistor presents the best $\frac{I_{ON}}{I_{OFF}}$ ratio.

Of all the transistors that could be used in the power part of the circuit, it is again the nominal V_T transistor that presents the best $\frac{I_{ON}}{I_{OFF}}$ ratio.

The power switches and some transistors of the control circuitry have a size greater than the maximum width. To build such big transistors, we employ the functions *mult* and $nfing$. It allows to put transistors of limited size in parallel to form a large equivalent transistor on the layout as depicted in Appendix **??**.

Comparison of logic transistors								
Name	L_{min} $[\mu m]$	L_{max} $[\mu m]$	W_{min} $[\mu m]$	W_{max} $[\mu m]$	Type	I_{ON} $[\mu A]$	I_{OFF} $[pA]$	$\frac{I_{ON}}{I_{OFF}}$
Nominal V_T	0.24	0.5	0.3	0.6	nch.9 pch.9	300 132	5.7 6.7	$5.3e^7$ $1.97e^7$
Medium V_T	0.34	20	0.3	10	mnch2 mpch2	343 143	1200 267	$2.86e^5$ $5.36e^5$
Native	0.5	20	0.3	10	lnch2 -	293 -	4241 -	$6.9e^4$ -
Zero V_T	0.6	20	0.3	10	znch2 zpch2	313 101	$1.7e^6$ $3.8e^4$	$1.84e^2$ $2.6e^4$

Table 4.2 - The nominal V_T transistors present the best $\frac{I_{ON}}{I_{OFF}}$ ratio.

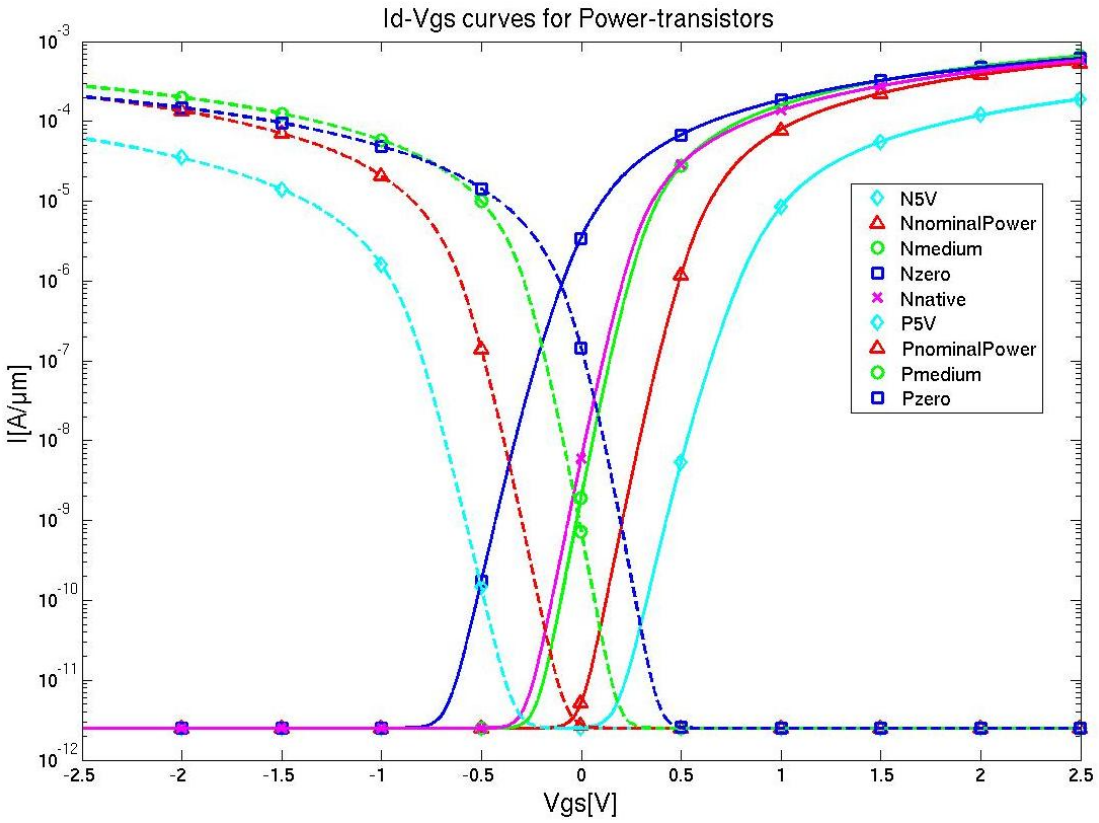


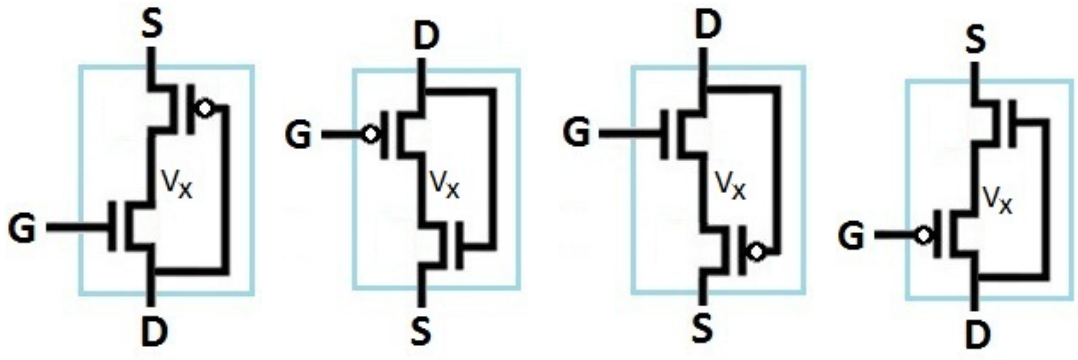
Figure 4.12 - $I_d - V_{gs}$ characteristics for $W = 2\mu m$, $L = L_{min}$, $T = 25°C$, $V_G = [-2.5; 2.5V]$, $V_{Dn} = 2.5V$, $V_{Sn} = 0V$, $V_{Bn} = 0V$, $V_{Dp} = -2.5V$, $V_{Sp} = 0V$, $V_{Bp} = 0V$. The solid lines represent the N-MOS transistors whereas the dashed lines represent the P-MOS transistors.

Comparison of power transistors								
Name	L_{min} $[\mu m]$	L_{max} $[\mu m]$	W_{min} $[\mu m]$	W_{max} $[\mu m]$	Type	I_{ON} $[mA]$	I_{OFF} $[pA]$	$\frac{I_{ON}}{I_{OFF}}$
Nominal V_T	0.24	0.5	1.2	100	nch.3 pch.3	1.2 0.52	13.5 6.7	$8.8e^7$ $7.7e^7$
$5V$	0.5	0.8	1.23	100	nch5.3 pch5.3	0.407 0.13	10.1 10.0	$4.05e^7$ $1.3e^7$
Medium V_T	0.34	20	0.3	10	mnch2 mpch2	1.3 0.55	3944 1406	$3.29e^5$ $3.93e^5$
Native	0.5	20	0.3	10	lnch2 -	1.14 -	$1.2e^4$ -	$9.5e^4$ -
Zero V_T	0.6	20	0.3	10	znch2 zpch2	1.2 0.4	$6.9e^6$ $2.9e^5$	$1.74e^2$ $1.4e^3$

Table 4.3 - The nominal V_T transistors present the best $\frac{I_{ON}}{I_{OFF}}$ ratio.

4.2.2 ULP transistors

The Ultra-Low-Power (ULP) concept is based on self-biased multi-threshold voltage CMOS transistors [42]. Typical uses of this concept are ULP voltage reference [43], ULP diode [44] or ULP SRAM [45]. Moreover, the ULP concept was extend to ULP transistors [46] on the basis of which ULP inverters and ULP logic circuits were developed. ULP transistors are obtained by the series connection of an NMOS and a PMOS device, which can be arranged so as to build either P-type or N-type transistors [37], as depicted in Figure 4.13. The internal devices are connected through their source.



(a) N-type passing. (b) P-type passing. (c) N-type blocked. (d) P-type blocked.

Figure 4.13 - ULP transistors.

In the N-type case, an NMOS device is stacked upon a PMOS device. NMOS gate is the gate (G) of the entire N-type transistor while PMOS gate

is connected to NMOS drain. The two other external accesses are : drain (D) conneted to NMOS drain and source (S) connected PMOS source. The body connexions are discussed in section 4.4.1.

The principle is similar in the P-type case. NMOS gate is connected to PMOS drain. The structure behaves externally as a PMOS transistor with three accesses : gate (G) connected to PMOS gate, drain (D) connected to PMOS drain and source (S) connected to NMOS drain. The body connexions are again discussed in section 4.4.1.

Due to the leakage reduction mechanism base on self-biased negative V_{gs} of the internal NMOS and PMOS devices, the ULP transistors have an ultra-low off-current I_{off} in the blocking-mode. However, in passing-mode, their current I_{on} is limited to subthreshold current, i.e. no saturation. Therefore, to reach a higher I_{on}, one can use zero-V_T devices.

ULP applications mentioned above use the ULP concept to reduce the power consumption, at room- as well as at high-temperature or for its good noise robustness. As explained in section 4.4.1, we will use ULP transistors in a new way : as power transistor. In addition to low leakage, they also allow us to get ride of the $3V$ supply voltage required in the classical implementation.

The I_d/V_{gs} characteristics of the ULP transistors of N- and P-types are depicted in Figure 4.14 and in Table 4.5.

	V_D $[V]$	V_S $[V]$
NMOS Nominal V_T	2.5	0
PMOS Nominal V_T	-2.5	0
NULP forward	0	2.5
NULP reverse	2.5	0
PULP forward	-2.5	0
PULP reverse	0	2.5

Table 4.4 - Conditions of the simulation depicted in Figure 4.14

4.3 Classical implementation

For both the logic and power parts, we will use transistors with nominal V_T because they present low leakage currents and a good I_{ON}/I_{OFF} ratio. In the capacitor network, we will use PMOS transistors where high voltages are to be

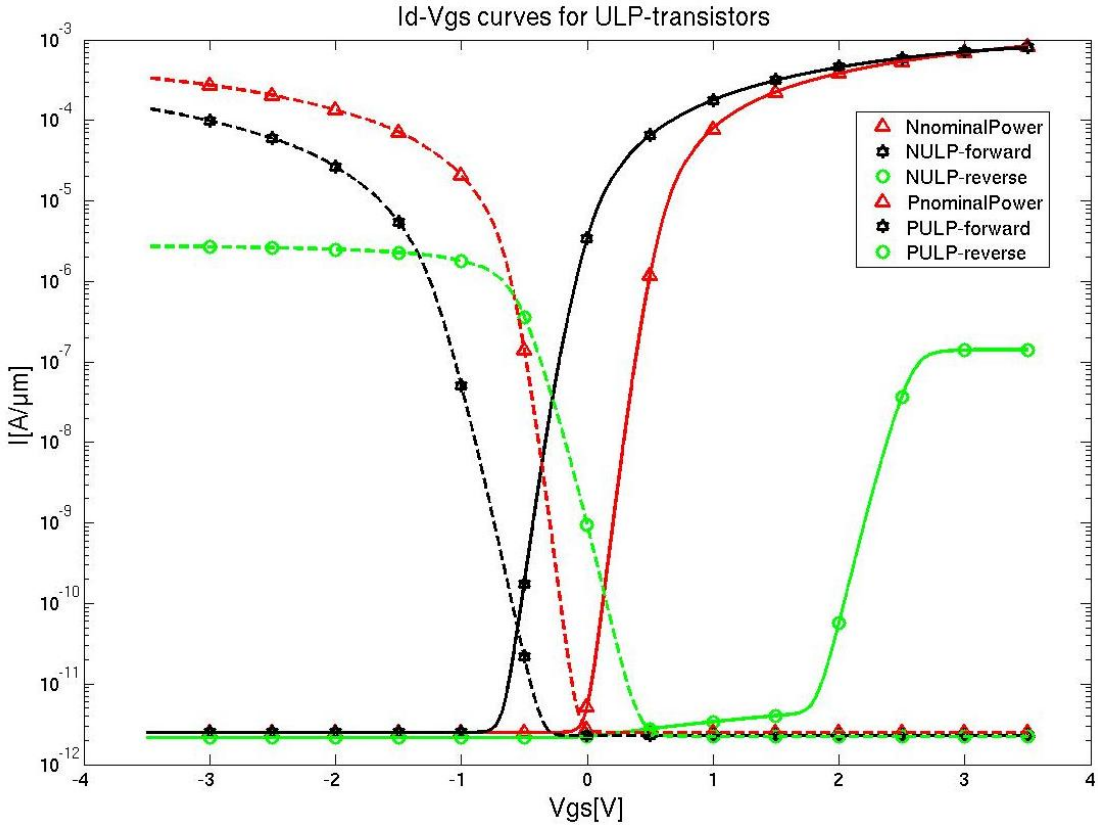


Figure 4.14 - $I_d - V_{gs}$ characteristics - For all the transistors : $L = L_{min}$, $T = 25°C$, $V_{Bn} = 0V$, $V_{Bp} = V_x$, $Wn = 2\mu m$, $Wp = 2\mu m$. The other conditions are given in Table 4.4. The solid lines represent the N-MOS transistors whereas the dashed lines represent the P-MOS transistors.

Name	Type	I_{ON} $[\mu A]$	I_{OFF} $[pA]$	$\frac{I_{ON}}{I_{OFF}}$
Nominal V_T	nch.3	$8.35e^2$	5.31	$1.57e^8$
	pch.3	$3.37e^2$	2.76	$1.22e^8$
NULP	forward	$7.97e^2$	$6.9e^6$	115
	reverse	0.142	2.23	$6.36e^4$
PULP	forward	$1.4e^2$	$3.46e^6$	41
	reverse	2.73	$9.43e^2$	$2.9e^3$

Table 4.5 - ULP transistors characteristics

delivered : transistors 1, 2, 3 and 4.

At some places we will need transistors able to support voltage differences of $3V$. However, the technology TSMC 250 does not make it possible to combine $5V$ transistors and zero V_T (ZVT) transistors on a same chip, so the ZVT transistors are not available for this implementation.

4.3.1 Capacitor network

The capacitor network of the system is presented in Figure 4.15. With the exception of switch 5 which is an NMOS transistor, all the switches are PMOS transistors as they can more easily pull up a voltage.

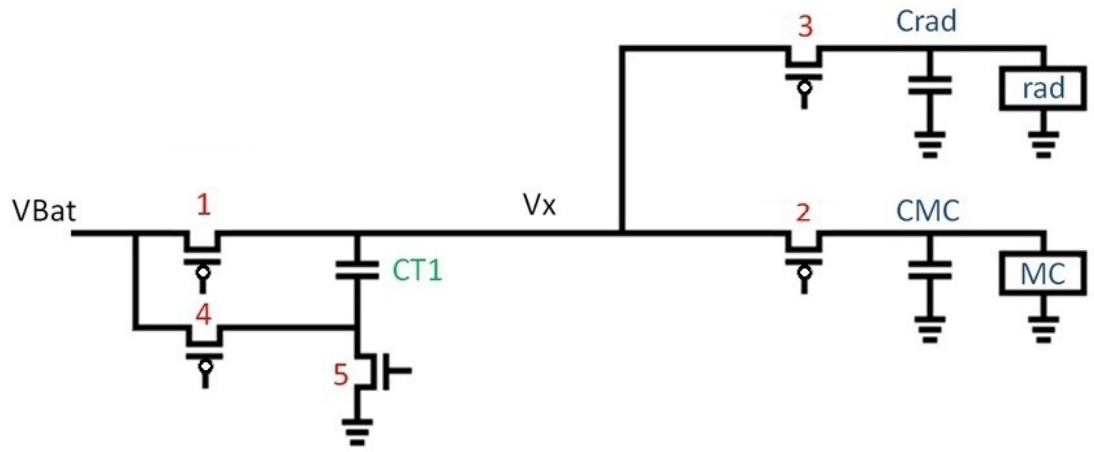


Figure 4.15 - All switches are PMOS transistors except switch 5 which is an NMOS transistor.

Transistors 1, 2 and 3 are connected to node V_X whose voltage rises to $3V$ when transferring charges to the radio. Because of that, those three transistors must be commanded by gate signals with an amplitude of $3V$; otherwise, they would also be passing in the reverse direction. As the control circuit operates at $1.5V$, they need level shifters, as shown in Figure 4.16, to generate their gate voltage. On the contrary, transistors 4 and 5 can be commanded in $1.5V$, i.e. the battery voltage.

Although transistors 1, 2 and 3 can be subjected to a voltage difference of $3V$ between two of their terminals, e.g. at startup, we chose to use $2.5V$ transistors instead of $5V$ transistors. That provides us an important gain in terms of consumed area.

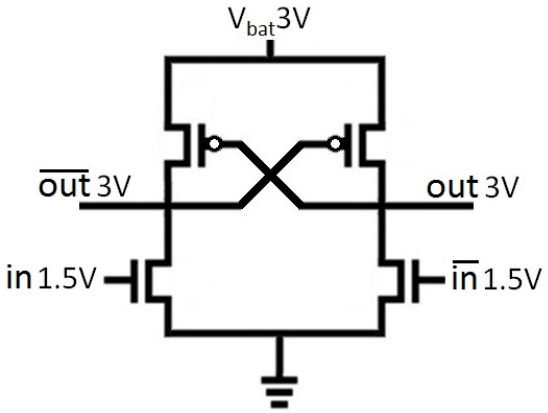


Figure 4.16 - Level shifters are required to convert the $1.5V$ logic signal into a $3V$ signal.

4.3.2 Control circuitry

The control circuitry that generates the gate signals of the switches in each of the four modes is represented in Figure 4.17. The circuit first determines in which mode it stands. Second, it generates the gate signals from the clocks. The generation of those clocks from the available $20Mhz$ clock was discussed in section 4.1.3. Third, the power bloc ensures that the gate signals are powerful enough to activate the switches and it also manages the delays between the different signals. The delays, introduced on the signal after the NOC blocs, are of primary importance as explained below.

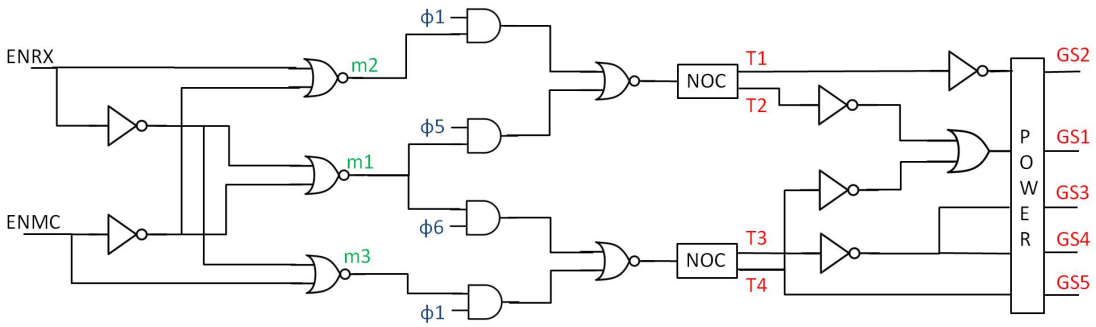


Figure 4.17 - Control circuit of the simplified circuit

The three modes for which the network is active are represented in green : $m1$, $m2$ and $m3$. The clocks are represented in blue : $\Phi 1$, $\Phi 5$ and $\Phi 6$. The NOC blocs are non-overlapping clock generators, they where detailed in section 4.1.2. Finally, each GSx signal is the gate signal of the switch of subscript x.

By default, the transistors of the control circuitry are set to the minimal size. For the components that come after the NOC blocs, care has been taken to impose

an appropriate delay on each signal. Otherwise, power consumption and operation issues would occur. Some examples of critical delays are presented below :

1. Delay between $GS1$ and $GS2$, Figure 4.18(a). Switch 1 must be blocked when switch 2 is passing.

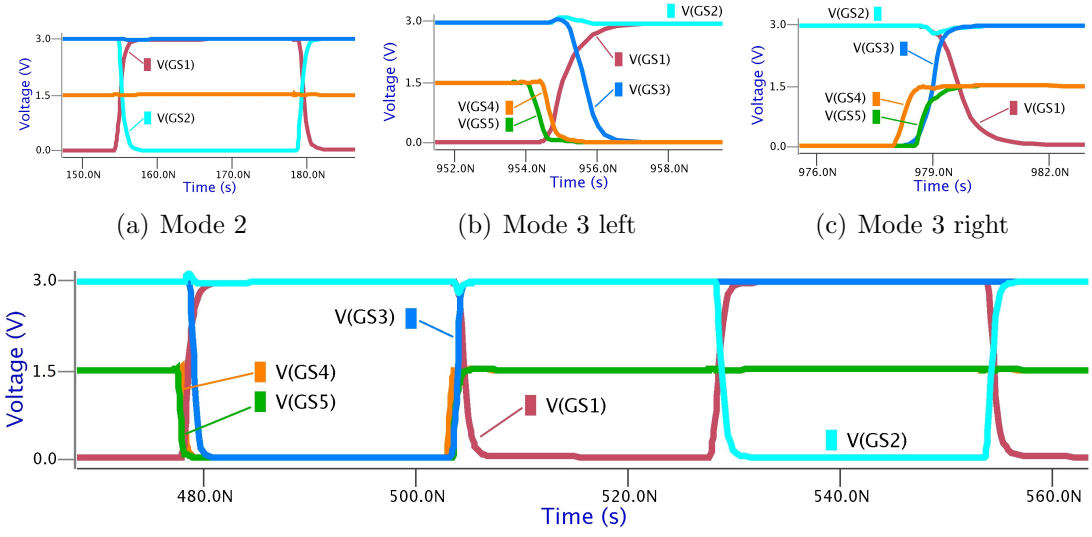
2. Delay between $GS1$ and $GS3$, Figures 4.18(b) and 4.18(c). Switch 1 must be blocked when switch 3 is passing.

3. Delay between $GS1$ and $GS4$, Figures 4.18(b) and 4.18(c). If both switches 1 and 4 are passing together, the transfer capacitor will be discharged and this will prevent the voltage V_X from rising sufficiently to be able to deliver its charges to C_{rad}.

4. Delay between $GS5$ and $GS4$, Figures 4.18(b) and 4.18(c). If at any time, switch 5 is passing along with switch 4, there will be a short circuit between power and ground. The corresponding power losses are unacceptable.

5. Delay between $GS3$ and $GS4$, Figures 4.18(b) and 4.18(c). If switch 3 becomes passing before switch 4 or stays passing after switch 4, then C_{rad} will transfer charges to C_T. The discharge of C_{rad} in C_T gives obviously rise to a loss of efficiency.

To manage the delays, we mainly use series of buffers of minimal size. The obtained control signals are presented in Figure 4.18.



(a) Mode 2 (b) Mode 3 left (c) Mode 3 right

(d) Mode 1

Figure 4.18 - Critical delays in the classical solution

4.3.3 Power consumption

In this section, the power consumption of each bloc will be studied in order to determine the global efficiency.

Control circuitry

Gate signals generation : the control circuitry that generates the gate signals of the power switches has a mean power consumption of $25\mu W$??. Besides that, one must add the power consumed in the relatively big inverters and buffers that allow those signals to attack the switch gates; the order of magnitude of this power is xxW.

As mentioned in section 4.1.2, each comparator consumes about $0.6\mu W$. The generation of the reference voltage was not taken into account but its consumption should be orders of magnitude lower [47].

Capacitor network

The consumption in the capacitor network is dominated by the charge and discharge losses of the transfer capacitors and by conduction losses.

Global efficiency

The global efficiency is calculated as follows :

$$\eta = \tag{4.3}$$

In terms of the operating mode, ...

That efficiency is (not) good ... :p why ? how to overcome this ?

To give an order of magnitude, the system would require a solar cell surface of $xxmm^2$ to be entirely supplied. Feasible or not ?(tenir compte du rendement du redresseur etc. ?)

4.4 ULP implementation

In this section, we propose an implementation that does not require the $3V$ voltage source. To achieve this, we suggest to use ultra-low-power (ULP) transistors commanded by gate signals of amplitude $1.5V$. Those transistors were presented in section 4.2.2.

4.4.1 Capacitor network

The capacitor network is represented in Figure 4.19.

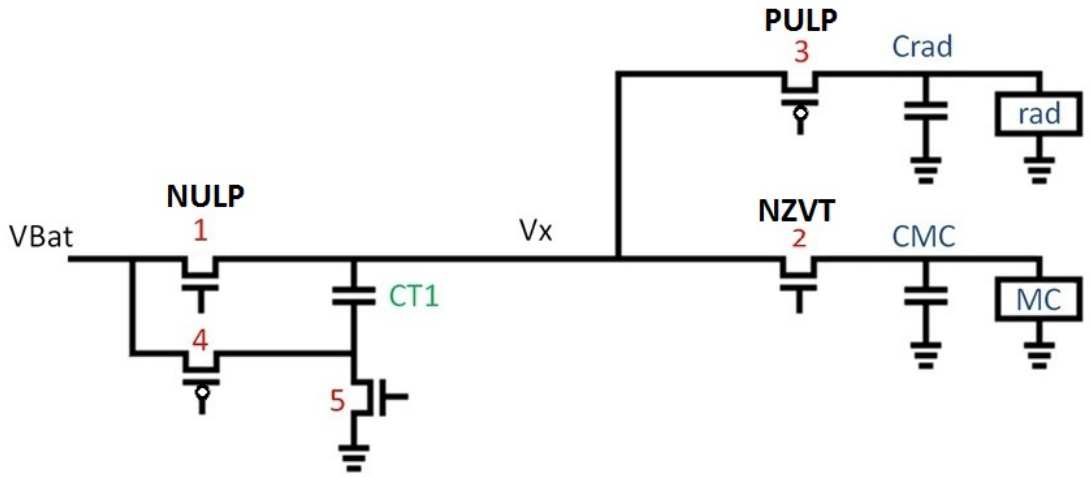
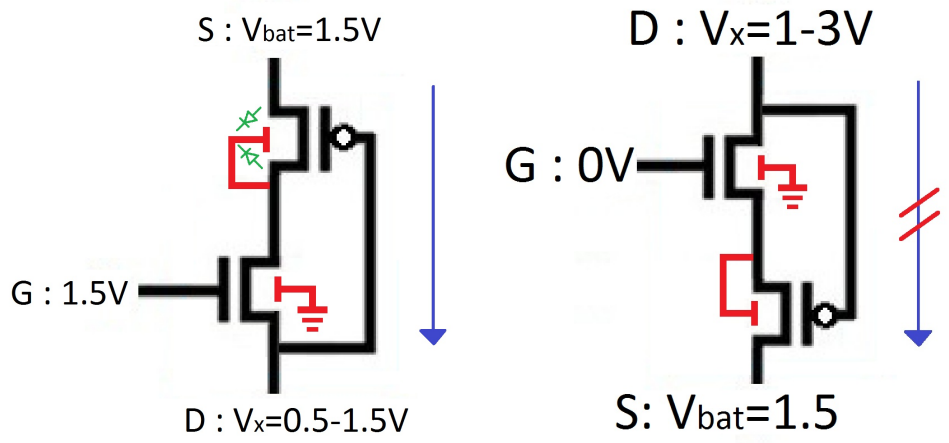


Figure 4.19 - Capacitor network for the ULP implementation. Switch 1 is a ULP transistor of N-type (NULP) while switch 3 is a ULP transistor of P-type (PULP). NZVT means N-type zero V_T transistor.

Switch 1 is a ULP transistor of type N (NULP), as depicted in Figure 4.20. Through this configuration, the switch is blocking with its gate at $0V$ even when V_X is at $3V$. The body of the internal PMOS is connected to the internal node. The NULP transistor presents de facto a better I_{on} current in passing mode. Indeed, as represented in Figure 4.20(a), the current can flow either through the PMOS channel or through the diode to its body and the connection towards the internal node. Both the internal NMOS and PMOS transistors are zero V_T transistors. The ULP transistor also presents the advantage that it allows us to better isolate the battery from the rest of the system in the case of everything being switched off : the leakage current towards the circuit is indeed limited in comparison with a classical transistor.

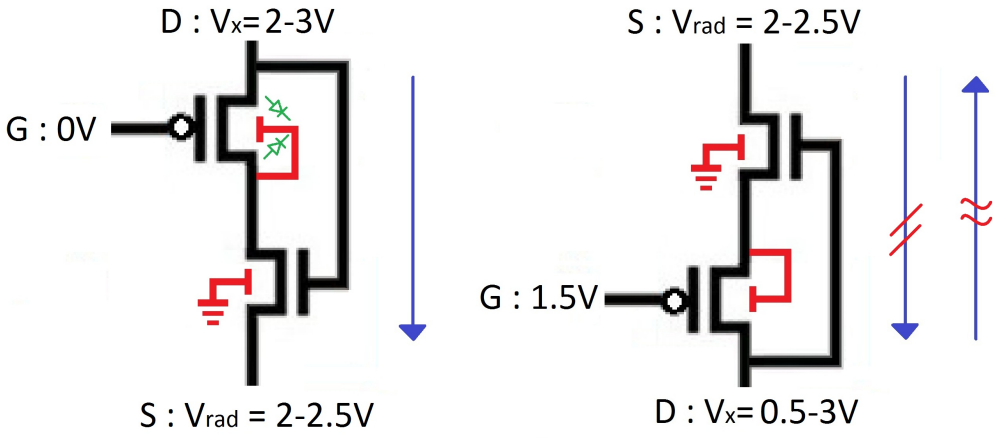
Switch 3 is a ULP transistor of type P (PULP), as depicted in Figure 4.21. The internal PMOS transistor is a nominal V_T transistor and the internal NMOS transistor is again a ZVT transistor in order to allow a maximum charge



(a) Passing mode (b) Blocking mode

Figure 4.20 - N-type ULP transistor

transfer from C_{T1} to C_{rad} : a ZVT transistor let V_x drop to V_{rad}. The body of the internal PMOS is again connected to the internal node to favour the I_{on} current, as represented in Figure 4.21(a). The switch is passing with its gate at $0V$ while it connects V_X $(3-2V)$ and C_{rad} $(2.5-2V)$. In that case a simple PMOS transistor commanded in $1.5V$ is unable to block the current. The ULP transistor blocks the current coming from its source because the internal NMOS transistor is blocking. However, it lets charges pass trough when V_X is higher than V_{rad}. This is undesirable but not critical; nevertheless, we have to consider this while designing this switch because it could prevent V_X from rising correctly.



(a) Passing mode (b) Blocking mode

Figure 4.21 - P-type ULP transistor

4.4.2 Control circuitry

The control circuitry that generates the gate signals of the switches is represented in Figure 4.22. It is the same circuit as in Figure 4.17 except that the gate signals generation from the output of the NOC blocs is different; switches 1 and 3 are now made of NMOS transistors instead of PMOS transistors. Furthermore, the power bloc is different because, in this solution, the switches are bigger and the delay constraints have changed.

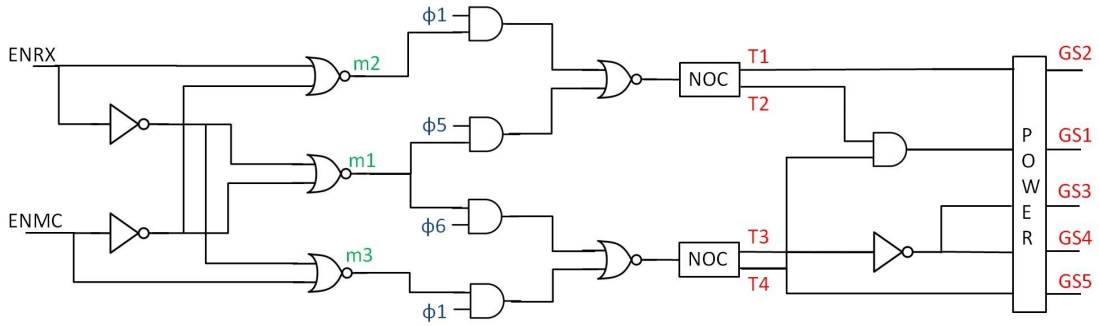
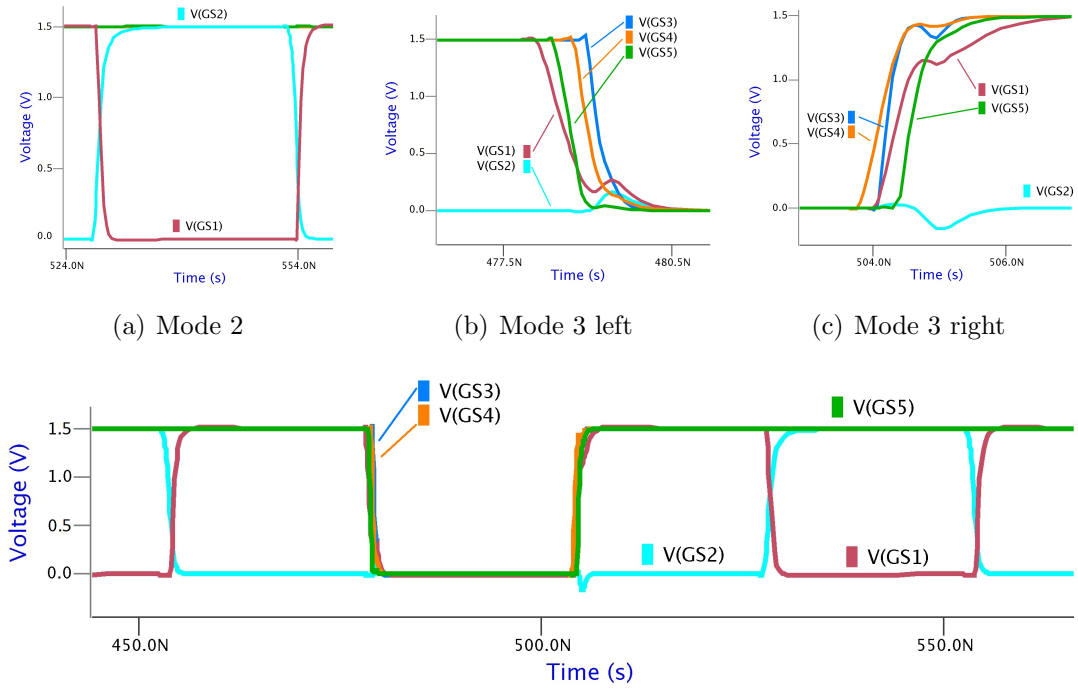


Figure 4.22 - Control circuit for the ULP implementation.

As explained in section 4.3.2, appropriate delays must be introduced after the NOC-blocs. Otherwise, power consumption and operation issues occur. Some examples of critical delays are presented below :

1. Delay between $GS1$ and $GS2$, Figure 4.23(a). Switch 1 must be blocked when switch 2 is passing.
2. Delay between $GS1$ and $GS3$, Figures 4.23(b) and 4.23(c). Switch 1 must be blocked as long as switch 3 is passing.
3. Delay between $GS1$ and $GS4$, Figures 4.23(b) and 4.23(c). Switch 4 must become passing after switch 1 becomes blocking to avoid discharging C_T.
4. Delay between $GS3$ and $GS4$, Figures 4.23(b) and 4.23(c). Switch 4 must become passing before switch 3, i.e. when V_x has risen to two times V_{bat}.
5. Delay between $GS4$ and $GS5$, Figures 4.23(b) and 4.23(c). Switch 5 must be blocked before switch 1 becomes passing. Otherwise, there will be a short circuit to the ground.

To manage the delays, we mainly use series of buffers. The obtained control signals are presented in Figure 4.23.



(a) Mode 2 (b) Mode 3 left (c) Mode 3 right

(d) Mode 1

Figure 4.23 - Critical delays in the ULP solution

4.5 Simulated efficiency

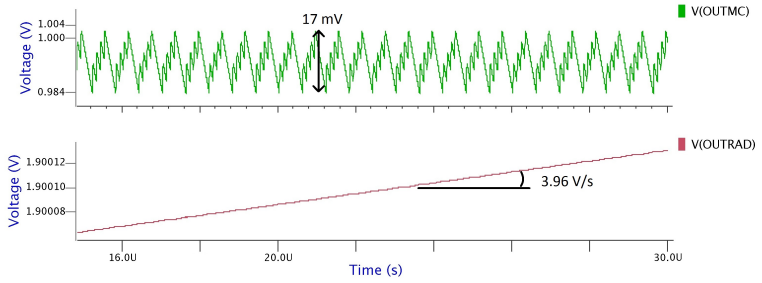
It would have been interesting to simulate the system on an operation period which would include several charges and uses of the radio among other things. This would however require a huge simulation time as well as huge storage capacity : the server returns an error when the storage capacity is exceeded while trying to allocate 131334144 bytes. This simulation is thus not feasible with the available resources.

Simulations in the different operating phases were executed : rising, dropping or regulation of the output voltage for both the MC and the radio. For each simulation, the overriding powers will be specified. Three simulations are presented in this section whereas the others are given in Appendix B.

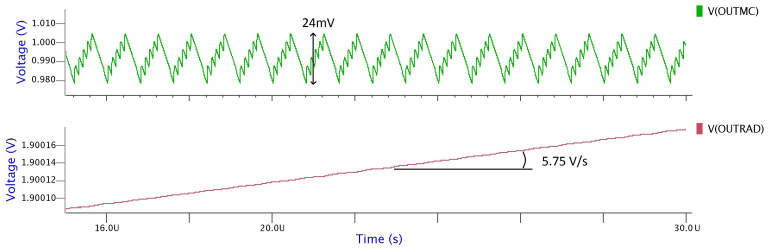
Charge of C_{rad} and regulation of C_{MC}

		ULP	Classic
t_{meas}	$[\mu s]$	15	15
$P_{comparators}$	$[\mu W]$	1.94	1.86
$P_{power-buffers}$	$[\mu W]$	256	216
$P_{control}$	$[\mu W]$	8.8	7.26
P_{outRad}	$[\mu W]$	1312	1904
P_{outMC}	$[\mu W]$	204	205
P_{in}	$[\mu W]$	2725	3586
P_{out}	$[\mu W]$	1517	2110
η	[%]	55.7	58.8

Table 4.6 - Charge of C_{rad} and regulation of C_{MC}



(a) ULP



(b) Classical

Figure 4.24 - Charge of C_{rad} and regulation of C_{MC}

When the output capacitor of the radio is charged, the efficiency is better in the classical implementation. There are two reasons for that. Firstly, the ULP transistor are bigger than the classical power switches as they are composed of two transisors in series and because of their lower forward current. The second reason is related to the non-blocking behavior of the PULP transistor as explained in section 4.4.1.

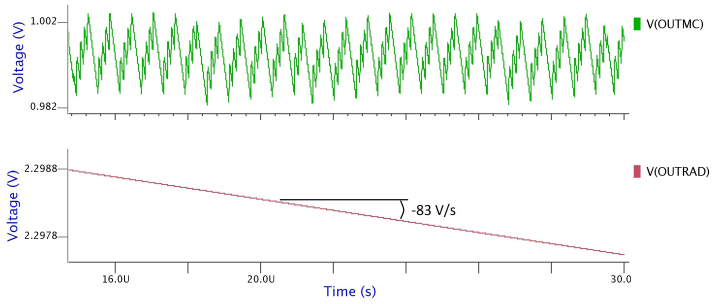
As depicted in Figure 4.24, the measured ripple on the MC output voltage is lower than $17mV$ in the ULP case and lower than $24mV$ in the classical case, so, it stays in the acceptable range fixed in Section 3.2.1. The growth rates of the

radio's output voltage reach $3.96V/s$ and $5.75V/s$ respectively, this means that $126ms$ or $87ms$ are necessary to charge C_{rad} from $2V$ up to $2.5V$.

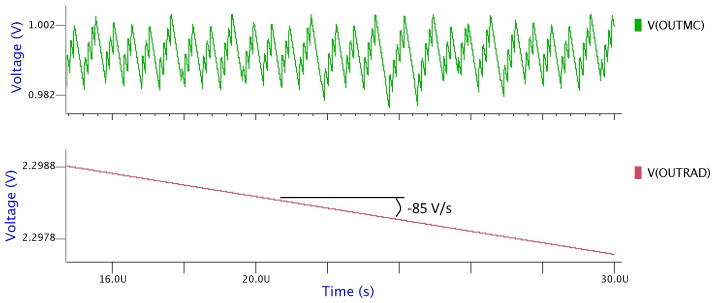
Use of C_{rad} and regulation of C_{MC}

		ULP	Classic
t_{meas}	$[\mu s]$	15	15
$P_{comparators}$	$[\mu W]$	1.94	1.91
$P_{power-buffers}$	$[\mu W]$	257	218
$P_{control}$	$[\mu W]$	8.8	7.26
P_{outRad}	$[\mu W]$	897	1504
P_{outMC}	$[\mu W]$	208	208
P_{in}	$[\mu W]$	1960	2717
P_{out}	$[\mu W]$	1106	1711
η	$[\%]$	56.5	63

Table 4.7 - Use of C_{rad} and regulation of C_{MC}



(a) ULP



(b) Classical

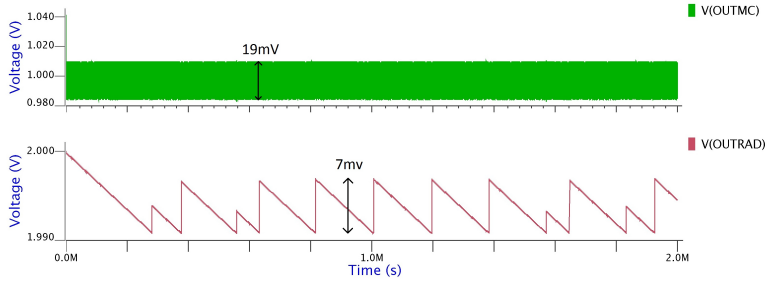
Figure 4.25 - Use of C_{rad} and regulation of C_{MC}

Figures 4.25(a) and 4.25(b) illustrate the period where the radio is in active mode. The growth rate are in this case equal to $-83V/s$ and $-85V/s$. The radio can accordingly be used during $6ms$ and $5.8ms$, respectively, and this correspond again with the specification of $5ms$ of use-time imposed in section 2.2.

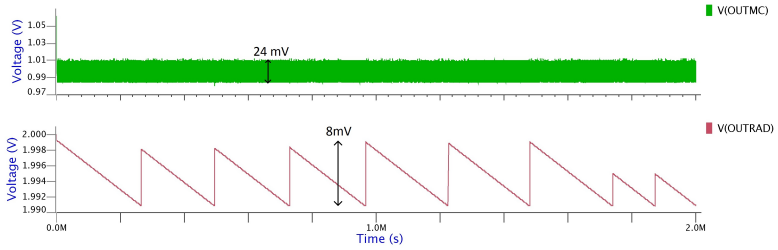
Regulation of C_{MC} and of C_{rad}

		ULP	Classic
t_{meas}	$[\mu s]$	$1e^3$	$1e^3$
$P_{comparators}$	$[\mu W]$	2.36	2.28
$P_{power-buffers}$	$[\mu W]$	27	82
$P_{control}$	$[\mu W]$	2.8	2.4
P_{outRad}	$[\mu W]$	1.15	0.9
P_{outMC}	$[\mu W]$	206	207
P_{in}	$[\mu W]$	356	413
P_{out}	$[\mu W]$	207	208
η	$[\%]$	58.1	50.3

Table 4.8 - Regulation of C_{MC} and of C_{rad}, for $C_{rad} = 16nF$



(a) ULP



(b) Classical

Figure 4.26 - Regulation of C_{MC} and of C_{rad}, for $C_{rad} = 16nF$

Because of the simulation time and of the amount of memory space required, a simulation long enough to illustrate the regulation of the radio was not feasible with the available resources. That is due to the fact that the charge time of C_{rad} is very high in comparison with the clock period used in the circuitry. In order to estimate the efficiency when both the voltages across C_{MC} and C_{rad} are kept constant, a simulation was executed with a smaller output capacitor : $C_{rad} = 16nF$ instead of $160\mu F$. This allows us to validate the regulation system and it gives us an estimate of the comparator resolution : the simulated ripple on V_{rad} is lower than $10mV$ for both implementations, cf. Figures 4.26(a) and 4.26(b). The power consumed by the radio does not depend on C_{rad}, so the energy

transferred toward the output is the same for $C_{rad} = 16nF$ and $C_{rad} = 160\mu F$. However, the charge packets will be differently spread out in time : as C_{rad} is actually larger, its discharge will be longer before the voltage V_{outRad} goes under the comparator detection threshold. Reciprocally, more charge packets are needed to return above the upper detection threshold. Thus, the system will let C_{rad} discharge longer ($\sim 2000s$) before it send a larger group of charge packets. The results should be verified by experimenting on the chip. The test methodology will be explained in chapter 5.

Comparison of the ULP and Classical Implementations

COMPARER LES 2 SOLUTION ULP Classique :surtout bas sur le rendement et les diffrentes pertes dans chaque cas.

The efficiency of the ULP implementation is lower than that of the classical one when lots of charges must be send to the radio, i.e. when charging or using the radio. To a large extent, that is due to the fact that the ULP switches are bigger than the classical switches. The required buffers and, so, their power consumption are then bigger, too, explaining the lower efficiency.

When the radio is in sleep mode, the power management unit just keeps the microcontroller and radio output voltages close to their respective reference. As the radio consumption is around $1\mu W$ in this case, only few charge packets must be send and the buffer consumption of switch 3 (PULP) is not critical anymore. It is now the fact that switches 1, 2 and 3 must be commanded in $3V$ that principally impacts the efficiency. The ULP implementation presents therefore a higher efficiency in this mode.

4.6 Area of improvement

Amlioration pour le rendement et la surface consomme ?

An important part of the losses occurs in the tapered buffers that drive the power switches. Consequently, the power switches should be co-designed with their corresponding drivers so that those losses are minimized.

The accuracy of the clock was not taken into account. However, the frequency of the clock could vary significantly from a device to another and its stability over time could also be poor. (Julien : variation PVT, WID ??)

It should be interesting to study the impact of variation of the input voltage V_{bat} both on the efficiency and on the output power.

4.7 Conclusion of the chapter

the power consumption and are compared in Table **??**

Both implementations give satisfactory results. They are good candidates among others for this type of application. Nevertheless, some improvement could still be brought in terms of efficiency and consumed area.

The efficiency of the ULP implementation is higher than that of the classical implementation when the system maintain the output voltages of the microcontroller and of the radio. Given that this is the most used mode, the ULP solution presents a higher global efficiency. A layout were therefore designed for this implementation so as to realized a prototype of the circuit on which the simulation results can be verified. That is the topic of the next chapter.

CHAPTER 5

Experimental Validation

In the previous chapters, we investigated ...

In this chapter, the layout realization and the test methodology will be presented for the implementation with ....ULP or not.....??.

In this chapter, the test methodology will be studied.

5.1 Layout

The criteria that characterize a good chip are [32]: the fabrication costs, proportional to the consumed silicon area; the speed performances and the power consumption. Those design intent constraints defined the way we have designed our system and must be kept in mind when drawing the layout. In addition, we must of course respect all the design rule constraints of the TSMC $0.25\mu m$ technology [48].

For each part of the circuit, we designed the different cells such that they all present the same row height, power rails V_{dd} and gnd, Nwell zone etc. This way we can assemble them in row organization which is much more simple. The sizing of the power rails is made in such a way as to limit the voltage drop due to the resistance and the instantaneous mean current. A trade-off between narrow rails and low voltage drop has to be done. In our case, with a length of ... and a width of ..., we come to a voltage drop of ... (Calculer avec le DRM).

Interconnection length minimization is important for speed and power concerns. The parasitic capacitances between the neighboring nets must be limited, too. That is especially important for the clock nets and other nets with high activity factor, as crosstalk noise could cause glitches or delays could be introduced during transitions. In addition, these nets are also subject to power losses due to parasitic capacitors. For these reasons, the clock rails are drawn as narrow and short as possible.

As routing layers, metal 1 is used for the basic cells, metal 2 for the horizontal connexions and metal 3 for the vertical connexions.

The gate signals of the power switches are passed into inverters in series with a fan-out of 4, in order to make the switch commute fast enough while minimizing the introduced delays.

Figure **??** presents the layout of the whole simplified circuit with its control bloc. More detailed views are available in appendixes **??**.

fig:layout total

It is clear in Figure **??** that the most space consuming components are the transfer capacitors, and, to a lesser extent, the power switches.

There are different ways to built a capacitor on an integrated circuit. For the transfer capacitors, we chose to work with Metal-Insulator-Metal (MIM) capacitors because they present less bottom plate-parasitic capacitance ($\sim 1\%$) and also less leakage current. That is due to the fact that they are located farther from the substrate. However, they require extra masks and their capacitive density ($1??fF/\mu m^2$) is lower; so, due to exta area and process option, they are more expensive. For the global circuit of chapter 3, we would have taken a MOS capacitor for C_A, the sensor capacitor. It uses the gate capacitance of MOS transistors. This capacitor type is more compact because of its higher capacitive density ($4upto12??nF/mm^2$). Its disadvantages are a more important bottom-plate capacitor ($\sim 10\%$), but this is not critical applied on an output capacitor as its bottom plate voltage is kept to ground, and, as second disadvantage, it presents higher leakage currents. They are however not critical applied on C_A because the sensor is just used occasionally.

Figure **??** presents the capacitor $CT1$. This capacitor was divided into many small capacitors for releasing the stress of wide metal area.

The approximate percentage of space occupied by each bloc of the management system is presented in Table **??**.

table:percentSpace

More than ...% of the area is occupied by the capacitors.

5.2 Measurement on a similar converter

Because of the time constraints, the circuit proposed in this Master thesis was not sent in fabrication. The measurements presented in this section were done on the dual-mode switched-capacitor DC-DC converter presented in [41]. The architecture of that converter is depicted in Figure 5.1. It operates either in high power mode (HP) with an output power up to $100\mu W$ or in low power mode with output power between $0.4nW$ and $250nW$. In low power mode, a clock with a lower frequency (f_{LP}) is generated in order to accommodate the ultra-low load in this mode.

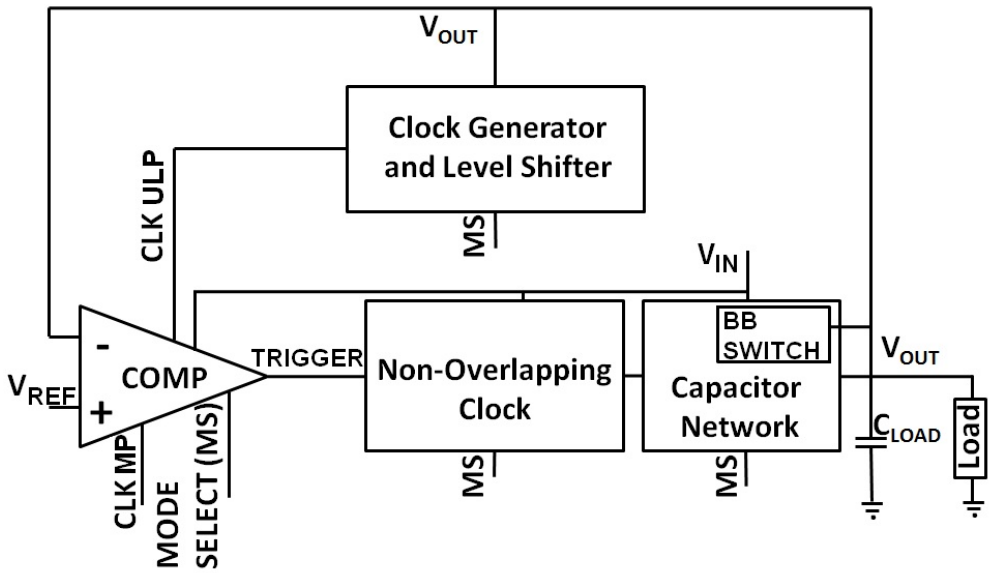


Figure 5.1 - Architecture fo the measured SC DC-DC converter [41].

That converter must be able to operate on a large range of temperature. To verify this, its efficiency in both modes was tested for various load powers at $-40°C$. Then the efficiency was tested for typical loads over a range of temperature from $-40°C$ to $70°C$.

5.2.1 Materials

The temperature and humidity chamber ESPEC SH-261 [49] was used so as to create the measurements conditions.

The Keithley K236 Source-Measure Unit (SMU) [50] is capable of sourcing and measuring voltage or current simultaneously. It was used to impose the output current while measuring the input current with high precision.

Keithley K2400i sources [51] were employed to generate the input and reference voltages and to measure the delivered currents.

The Agilent MSO810AA $1GHz$ real-time oscilloscope were used to measure both the output voltage and the low-power clock.

5.2.2 $-40°C$ Operation

Figure 5.2 shows the output voltage in high power (HP) mode while the circuit is working at $-40°C$. The output voltage is well regulated and the voltage ripple is of about $20mV$.

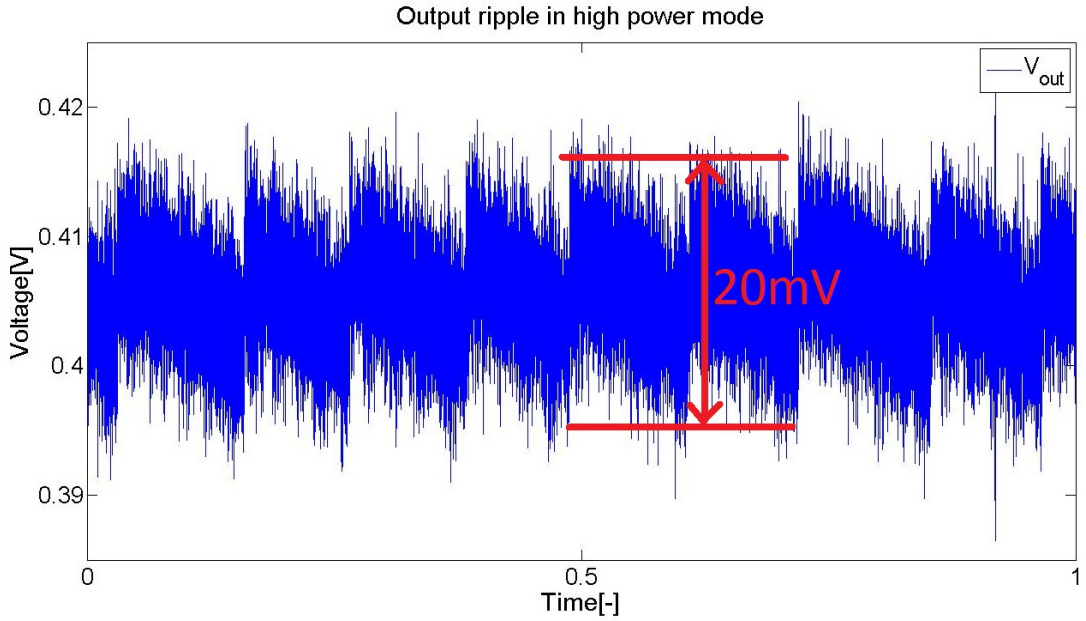
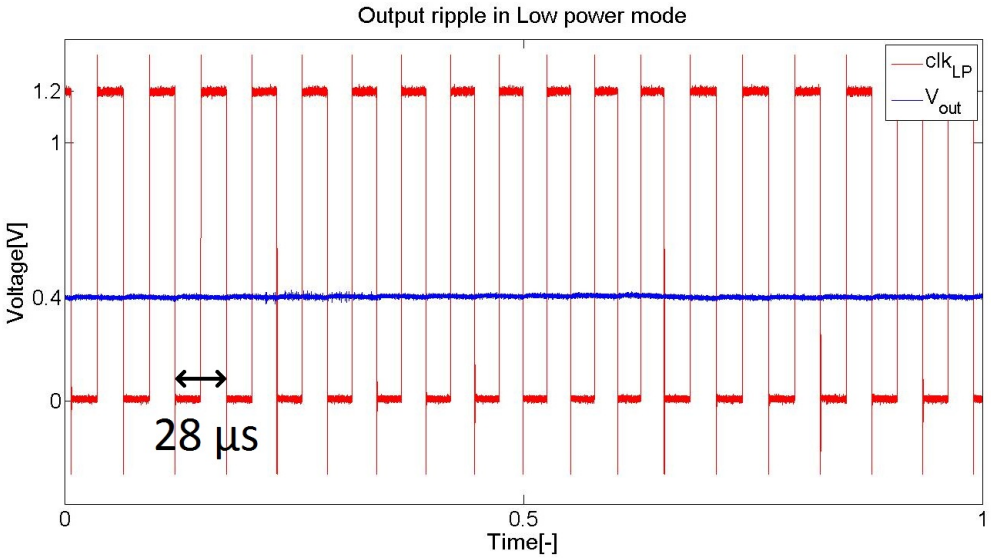


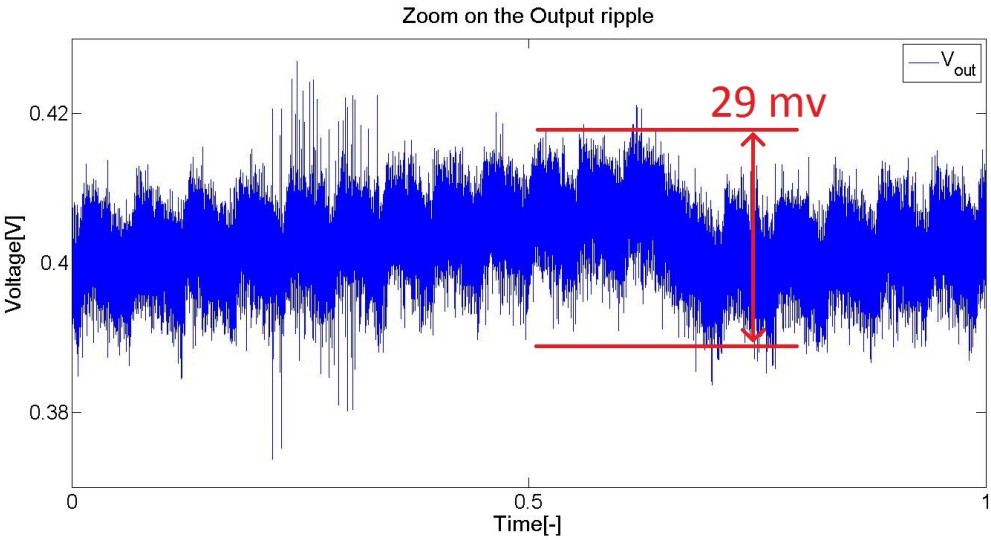
Figure 5.2 - The output ripple in high power mode is limited to $20mV$.

Figure 5.3(a) shows the output voltage in low power mode while the circuit is working at $-40°C$. A zoom of the same plot is shown in Figure 5.3(b). The output voltage has a sawtooth shape due to the charges packets sent by the circuit. The system sometimes misses a step as can be observed for $x = 0.7$. That can simply be explained by the fact that the clocked comparator orders the converter to send charges to the output if the output voltage is lower than the reference voltage. As this comparison is discrete, a step is *missed* when it occurs while the

output voltage is just above the reference one. Missed steps will thus come about periodically. The output ripple is on the same order as in the high power case.



(a) Low power clock (clk_{LP}) and output voltage.



(b) The output ripple in low power mode is limited to $30mV$.

Figure 5.3 - Low power mode.

The measured values of the output current and voltage and of the input current are presented in Table 5.0(b) in low power (LP) mode and in Table 5.0(a) for the system is working in high power mode. Those two experimentations were operated for the conditions : $T = -40°C$, $V_{ref} = 0.4V$ and $V_{in} = 1V$. Then, Figure 5.4 shows the efficiency in function of the load power at that temperature.

(a) High power mode

I_{out} $[\mu A]$	V_{outHP} $[V]$	I_{inHP} $[\mu A]$
$50e^{-3}$	0.402	$760e^{-3}$
$100e^{-3}$	0.4018	$788e^{-3}$
$300e^{-3}$	0.4011	$897e^{-3}$
$600e^{-3}$	0.4	1.06
1	0.4	1.27
3	0.399	2.33
6	0.399	3.934
10	0.3989	6.05
30	0.398	16.66
60	0.398	32.55
100	0.397	53.7
300	0.394	160
350	0.385	186
375	0.378	198
400	0.371	211
450	0.357	236
500	0.343	261
550	0.330	286
650	0.301	336
750	0.273	386

(b) Low power mode

I_{out} $[nA]$	V_{outLP} $[V]$	I_{inLP} $[nA]$
1	0.394	7.6
5	0.3938	9.6
10	0.3934	12.1
30	0.4026	24
60	0.404	39.4
100	0.404	60
200	0.402	111
300	0.401	163
500	0.399	265
600	0.397	316
610	0.396	321
625	$FAIL$	–

Table 5.1 - Measurements for different output currents at $T = -40°C$.

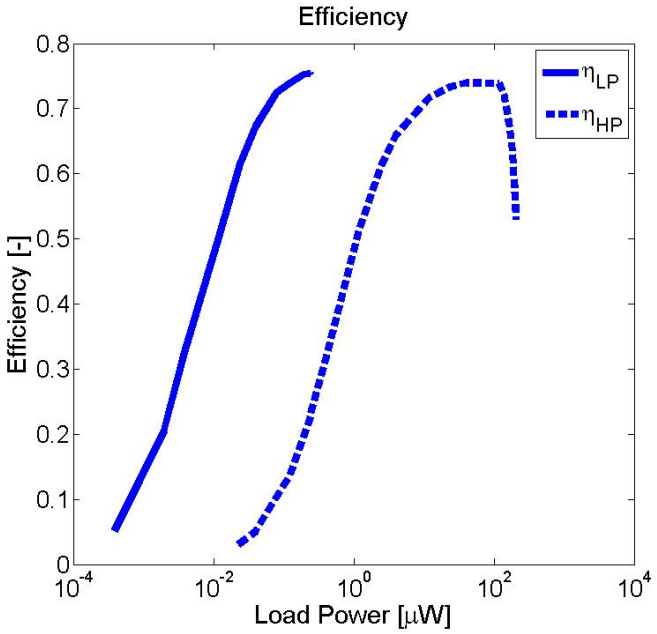


Figure 5.4 - Effiency at $-40°C$.

5.2.3 Sweep in Temperature

Table 5.2 presents a sweep in Temperature in the conditions : $I_{outLP} = 250nA$, $I_{outHP} = 250\mu A$, $V_{ref} = 0.4V$ and $V_{in} = 1V$. Those conditions correspond to output powers of $P_{loadLP} = 100nW$ and $P_{loadHP} = 100\mu W$, respectively in low power (LP) and in high power (HP) modes. Figure 5.5 shows the evolution of the efficiency in function of the temperature for these typical loads. Figure 5.6 depicts the change of the low power frequency (f_{LP}) with the temperature.

T [°C]	mean f_{LP} [kHz]	V_{outLP} [V]	I_{inLP} [nA]	V_{outHP} [V]	I_{inHP} [μA]
−40	36	0.403	137	0.394	133
−30	40	0.402	138	0.394	133
−20	45	0.402	140	0.394	133
−10	49.2	0.402	143	0.394	133
0	54.2	0.402	146	0.393	133
10	58	0.402	150	0.393	133
20	–	0.402	156	0.394	133
30	67.7	0.403	166	0.395	134
40	72.3	0.403	180	0.395	134
50	77.7	0.403	200	0.395	134
60	81.5	0.403	226	0.394	134
70	86.3	0.403	264	0.395	134

Table 5.2 - Sweep in Temperature.

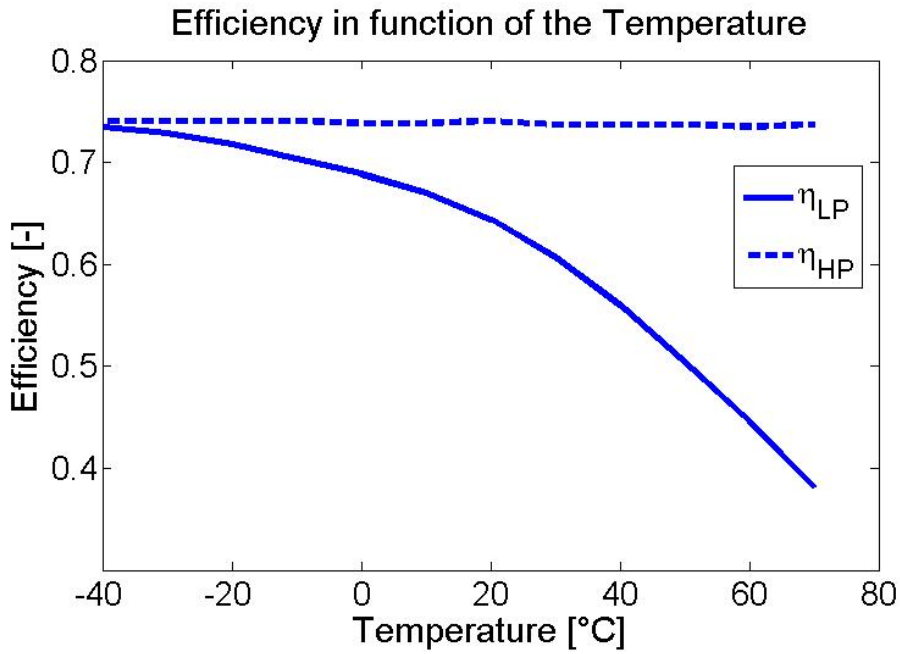


Figure 5.5 - In low power mode, the efficiency is better at low temperature.

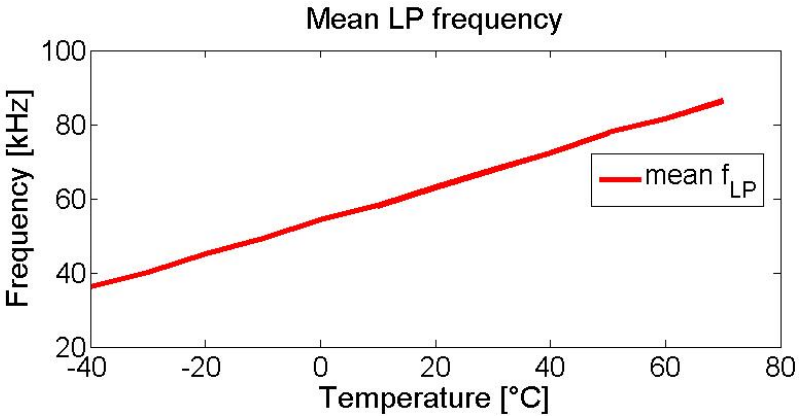


Figure 5.6 - The low power frequency increases with the temperature.

5.3 Area of improvement

5.4 Conclusion of the chapter

Conclusion and Perspectives

This Master thesis proves that, with a single converter, it is possible to supply several devices presenting quite different voltage and power levels. This is essential for Energy Autonomous Systems (EASs) as they are subject to severe volume constraints. In the next few years, these systems will take advantage of their reduced size and costs to spread to new applications. One can imagine using them in the industry in order to take measurements of some physical quantities, e.g. in hard to access places. Even through obstacles such as perceived value or compatibility must still be addressed, the use of EASs will also become widespread in healthcare, fitness and entertainment.

Achieving extended lifetime of several years is a significant challenge in view of the fact that these systems are often capable of storing only small amounts of energy. Therefore, EASs resort to harvesting energy from their immediate environment. However, this leads to new difficulties related to the source variability. These constraints motivate the development of converters, both power- and space-saving, to manage the energy transfers in the system. The main role of the power management unit is to provide suitable voltage levels to the system outputs.

The converter proposed in this work supplies three outputs with the help of a capacitor network : a microcontroller ($1V$) that consumes $200\mu W$ in active mode and $1\mu W$ in sleep mode; a radio ($2 - 2.5V$) whose consumption reaches $30mW$ in active mode and is lower than $4\mu W$ in sleep mode; and a sensor ($0.7V$) that is either active with a consumption close to $1\mu W$ or shut down with a null consumption. A converter that provides power to the microcontroller and the radio, presents an efficiency of 57% on a typical use period. The consumed area of this converter is lower than $1.5mm^2$.

+ Perspectives ...

Bibliography

[1] D. Flandre, *Circuits Intégrés Analogiques, ELEC 2650*. Université catholique de Louvain.

[2] C.L. Wei, C.H. Wu, L.Y. Wu and M.H. Shih, *An Integrated Step-UP/Step-Down DC-DC Converter Implemented With Switched Capacitor Circuits*. IEEE transactions on circuits and systems-II : express briefs, VOL. 57, NO. 10, october 2010.

[3] Y. K. Ramadass and A. P. Chandrakasan, *Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications*. in Proc. Power Electronics Specialists Conf., 2007, pp. 23532359.

[4] D. Maksimovic and S. Dhar, *Switched-Capacitor DC-DC converters for Low-Power On-Chip Applications*. IEEE PESC, 1999 Record, pp. 54-59.

[5] M. Belloni, E. Bonizzoni and F. Maloberti, *Single-Inductor Multiple-Output DC-DC Converters*. University of Pavia - Italy.

[6] Ma, D., Ki, W., and Tsui, C. *A pseudo-CCM/DCM SIMO switching converter with freewheel switching*. in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2002, pp. 390391.

[7] M. Belleville, E. Cantatore, et al., *Energy Autonomous Systems: Future Trends in Devices, Technology, and Systems*. Report, CATRENE Working Group on Energy Autonomous Systems, 2008, pg. 5.

[8] M. Belleville, et al., *Energy Autonomous Sensor Systems: State and Perspectives of a Ubiquitous Sensor Technology*. in Advances in sensors and interfaces IWASI, 2009, pp. 134-138.

[9] E.O.Torres, et al., *Hybrid supplies for wireless micro-systems*, the electrochemical society: Interface, pp.57-60, Fall 2008.

[10] M.A. Hanson, H.C. Powell Jr., et al., *Body Area Sensor Networks: Challenges and Opportunities*. IEEE Computer, 58-65, January 2009.

[11] Semtech, *SX1212 Transceiver datasheet : Ultra-Low Power Integrated 300-510MHz Transceiver*.

[12] Texas Instrument, *Enhanced CC1100 datasheet : Low-Power Sub-1 GHz RF Transceiver*.

[13] M. S. Makowski and D.Maksimovic, *Performance limits of switchedcapacitor DC-DC converters*, in Power Electronics Specialist Conference PESC, 1995, pp. 1215-1221, vol. 2.

[14] H. Shao, C. Y. Tsui and W. H. Ki, *A Single Inductor Dual Input Dual Output DC-DC Converter with Hybrid Supplies for Solar Energy Harvesting Applications*, International Symposium on Low Power Electronics and Design, pp. 69-74, 2009.

[15] M. Chen, et al., *Single inductor, multiple input multiple output (SIMIMO) power mixer-charger-supply system*, Proc. of Int. symposium on low power electronics and design, pp.310-315, 2007.

[16] N.M.Sze, et al., *Integrated single-inductor dual-input dual-output boost converter for energy harvesting applications*, IEEE Int. Symposium on circuits and systems, pp.2218-2221, 2008.

[17] C. Lu, V. Raghunathan, K. Roy, *Micro-Scale Energy Harvesting: A System Design Perspective*, ASPDAC '10, Automation Conference IEEE Press Piscataway, NJ, USA 2010.

[18] Sana Ullah, et al., *A Comprehensive Survey of Wireless Body Area Networks*, Journal of Medical Systems, July 2010.

[19] C. Vigorito, D. Ganesan, and A. Barto, *Adaptive Control for Duty-Cycling in Energy Harvesting-based Wireless Sensor Networks*, Proc. IEEE Communications Society Conference on Sensor, Mesh, and Ad Hoc Communications and Networks (SECON) 2007.

[20] J. Hsu, S. Zahedi, A. Kansal, M. Srivastava, and V. Raghunathan, *Adaptive duty cycling for energy harvesting systems*, Proc. ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), pp. 180-185, 2006.

[21] T.A. Pering, T.D. Burd, and R. W. Brodersen, *The simulation and evaluation of dynamic voltage scaling algorithms.*, in Proc. ACM ISLPED, pp. 76-81, 1998.

[22] M. Gorlatova, P. Kinget, et al., *Challenge: ultra-low-power energy-harvesting active networked tags (EnHANTs)*, in Proc. ACM MobiCom09, Sept. 2009.

[23] J. Zheng and T. Jow, *High energy and high power density electrochemical capacitors,* J. Power Sources, vol. 62, no. 2, pp. 155159, 1996.

[24] V. Raghunathan and P. H. Chou, *Design and power management of energy harvesting embedded systems*. In ISLPED '06: Proceedings of the 2006 international symposium on Low power electronics and design, pages 369–374, New York, NY, USA, 2006. ACM Pres.

[25] V. Raghunathan, A. Kansal, et al., *Design considerations for solar energy harvesting wireless embedded systems*, Proc. ACM/IEEE International Conference on Information Processing in Sensor Networks (IPSN), pp. 457-462, 2005.

[26] C. Lu, V. Raghunathan and K. Roy, *Maximum Power Point Considerations for Micro-Scale Solar Energy Harvesting Systems*, IEEE International Symposium on Circuits and Systems, 2010.

[27] X. Jiang, J. Polastre, D. Culler, *Perpetual Environmentally Powered Sensor Networks,* International Symposium on Information Processing in Sensor Networks, pp. 463-468, 2005.

[28] J. P. Recas, C. Bergonzini, et al., *Prediction and management in energy harvested wireless sensor nodes*, 1st International Conference Wireless Vitae on Wireless Communications, Vehicular Technology, Information Theory and Aerospace & Electronic Systems Technology, 2009.

[29] L. Mateu and F. Moll, *Review of Energy Harvesting Techniques and Applications for Microelectronics,* the Proceedings of the SPIE Microtechnologies for the New Millennium, pp. 359-373, 2005.

[30] R. F. Yazicioglu, T. Torfs, et al., *Ultra-low-power biopotential interfaces and their applications in wearable and implantable systems*, Microelectronics Journal, vol. 40, No. 9, pp. 1313-1321, 2009.

[31] G. Gosset, D. Bol, G. Pollissard-Quatremre, B. Rue, D. Flandre, *Disruptive ultra-low-power SOI CMOS circuits towards μW medical sensor implants*, in SOI Conference (SOI), 2010 IEEE International.

[32] D. Bol, J-D Legat, *Implementation of Digital Electronics Systems, ELEC 2570.* Université catholique de Louvain.

[33] V. Leonov, et al., *Wearable self-powered wireless devices with thermoelectric energy scavengers*, Smart Syst. Integration Conf. 2008.

[34] T. T. Le, *Efficient Power Conversion Interface Circuits for Energy Harvesting Applications*, Ph.D. thesis, Oregon State University, 2008.

[35] Y. Ammar, S. Basrour, *Conception de systmes de gestion d'énergie pour microsystmes autonomes*, Ph.D. thesis, Université Joseph Fourier, 2006.

[36] G. Villar Piqué, Henk Jan Bergveld, *State-of-the art of integrated switching power converters*, NXP Semiconductors, 20th Workshop on Advances in Analog Circuit Design (AACD), 2011.

[37] D. Bol, D. Flandre, J.-D. Legat, *Ultra-Low-Power Circuit*, U.S. Pat. Appl. Publ., 2010, US 2010/0134149 A1.

[38] D. Bol, C. Hocquet, D. Flandre and J.-D. Legat, *Robustness-Aware Sleep Transistor Engineering for Power-Gated Nanometer Subthreshold Circuits*, in Proc. IEEE ISCAS, 2010, pp. 1484-1487.

[39] N. Verma, et al., *Data-Driven Approaches for Computation in Intelligent Biomedical Devices: A Case Study of EEG Monitoring for Chronic Seizure Detection.*, Journal of Low Power Electronics and Applications, April 2011.

[40] S. Hanson, et al., *A low-voltage processor for sensing applications with picowatt standby mode*, in IEEE J. Solid-State Circuits, vol. 44 (4), pp. 1145-1155, 2009.

[41] J. De Vos, D. Bol, D. Flandre, *Dual-Mode Switched-Capacitor DC-DC Converter for Subthreshold Processors with Deep Sleep Mode*, ICTEAM institute, Université catholique de Louvain, Belgium, 2010.

[42] V. Dessard, *SOI Specific Analog Techniques for Low-Noise, High-Temperature or Ultra-Low Power Circuits*, Ph.D dissertation, Université catholique de Louvain, 2001.

[43] A. Adriaensen V. Dessard and D. Flandre, *25 to* $300°C$ *ultra-low-power voltage reference compatible with standard SOI CMOS process*, in Electronics Letters, vol. 38, no. 19, pp. 1103-1104, Sep. 2002.

[44] D. Levacq, C. Liber, V. Dessard and D. Flandre, *Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology*, in Solid-State Electronics, vol. 48, no. 6, pp. 1017-1025, Jun. 2004.

[45] J. De Vos, *Développement de circuits mémoire ultra-basse consommation pour applications portables en technologie bulk 130nm*, Mémoire, Université catholique de Louvain, 2008.

[46] D. Bol, *Pushing Ultra-Low-Power Digital Circuits into the Nanometer Era*, Thesis, Université catholique de Louvain, december 2008.

[47] M. Seok, G. Kim, et al., *A 0.5V 2.2pW 2-transistor voltage reference,* Proceedings of the IEEE Custom Integrated Circuits Conference, pp.577-580, September 2009.

[48] Taiwan Semiconductor Manufacturing Co., *TSMC 0.25 UM CMOS LOGIC/MS DESIGN RULE (CL025G, CM025G, CR025G)*, 2010.

[49] ESPEC, *Bench-Top Type Temperature (& Humidity) Chamber*, March 2010.

[50] Keithley, *Model 236, 237 and 238 Source-Measure Units, Operator's Manual*, 1989.

[51] Keithley, *Model 2400 Series SourceMeter, User's Manual*, 1998.

APPENDIX A

Single Inductor Converter

Circuit SC + 1 inductance

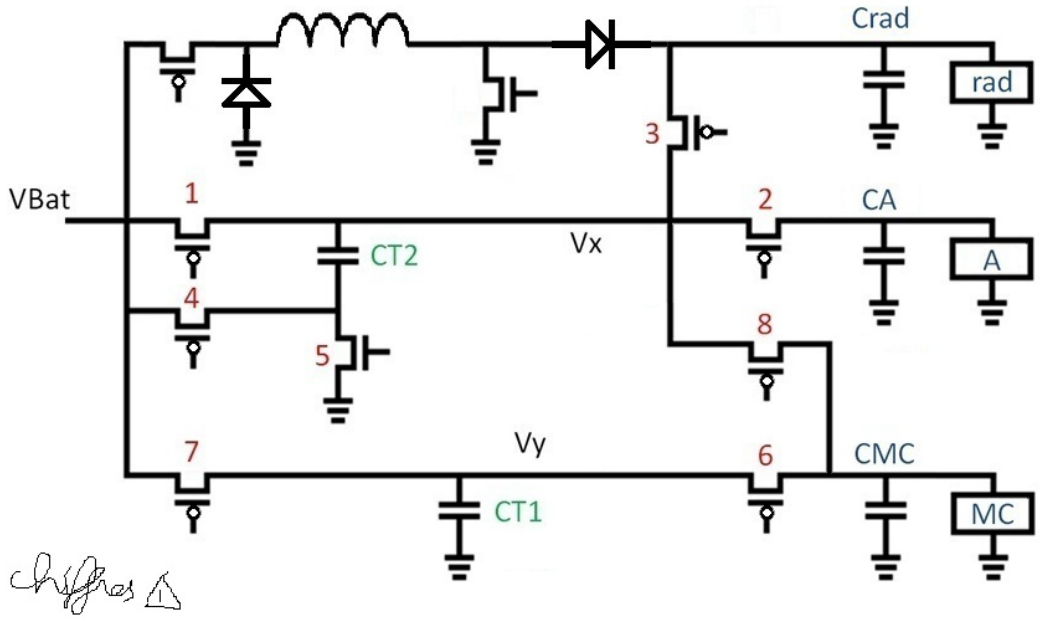


Figure A.1 - The inductor supplies the radio in active mode.

The transistor $M9$ must be large enough to keep V_X close to 0 when the maximum current is flowing into it.

$\oplus$ C_{rad} $\searrow$

- $\oplus$ t_{charge} of C_{rad} $\searrow$
- $\oplus$ switching losses $\searrow$
- $\ominus$ complexity of the circuit and of the control system $\nearrow$
- $\ominus$ low quality factor of the inductor.
- $\ominus$ consumed area $\nearrow$
- $\ominus$ C_{MC} and C_A $\nearrow$

A.1 Design of the inductor

As announced in section 2.2, the use-time of the radio is limited to : $t_{use} = 5ms$ whereas the start up time is : $t_{startup} = 240\mu s$. We also impose that the voltages at the beginning and the end of the use are $2.5V$ and $2V$ while the available battery provides $1.5V$.

As a compromise between the size of the inductor L and the output capacitor C_{rad}, we impose the ratio of the energy provided by the inductor over the overall energy consumed by the radio (POURQUOI ce choix ??):

$$rap = \frac{\text{energy provided by the inductor}}{\text{energy provided by (inductor + } C_{rad})} = \frac{3}{5} \tag{A.1}$$

As the energy stored in L and C_{rad} are

and

respectively, we obtain :

$$L_{rad} \approx 80mH \tag{A.2}$$
$$C_{rad} \approx 70\mu F \tag{A.3}$$

The current that flowing through the inductor to store the needed energy is :

$$I_L \approx 55mA \tag{A.4}$$

The voltage difference imposed by this current on C_{rad} when the radio is active is :

$$\Delta V_{rad} \approx 0.5V \tag{A.5}$$

To obtain a current of $55mA$ in the inductor of $80mH$, we need to apply the voltage $V_{bat} = 1.5V$ during a charge time of : $t_{charge} = 3ms$. The micro-processor must therefore foresee the use of the radio $3ms$ earlier.

APPENDIX B

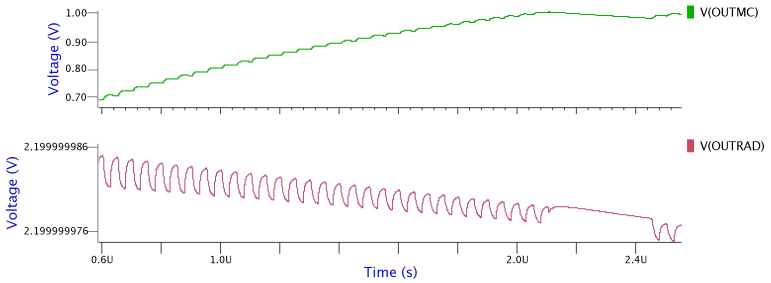
Simulated Efficiency

In this appendix, the rest of the operating phases are presented. This is a complement related to section 4.5.

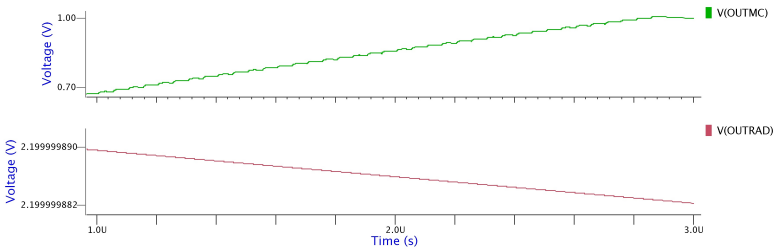
Charge of C_{MC} and discharge of C_{rad}

		ULP	Classic
t_{meas}	$[\mu s]$	2	2
$P_{comparators}$	$[\mu W]$	1.3	1
$P_{power-buffers}$	$[\mu W]$	71	81
$P_{control}$	$[\mu W]$	7.1	6.6
P_{outRad}	$[\mu W]$	-0.257	$-2.5e^{-2}$
P_{outMC}	$[\mu W]$	586	653
P_{in}	$[\mu W]$	1113	1326
P_{out}	$[\mu W]$	586	653
η	[%]	52.7	49.3

Table B.1 - Charge of C_{MC} and discharge of C_{rad}



(a) ULP



(b) Classical

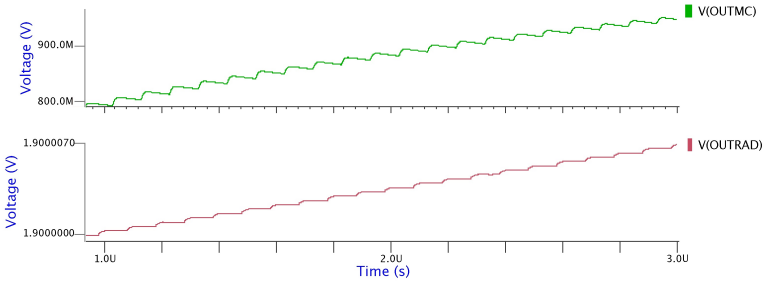
Figure B.1 - Charge of C_{MC} and discharge of C_{rad}

There is a ripple induced on V_{outRad} when the microcontroller receives charges. That is due to the fluctuation of V_x. The ripple that is visible in Figure B.1 is caused by the charge and discharge of the parasitic capacitance C_{gd} of the internal NMOS transistor of the PULP switch, cf. Figure 4.21. This ripple is negligible compared to the comparator resolution.

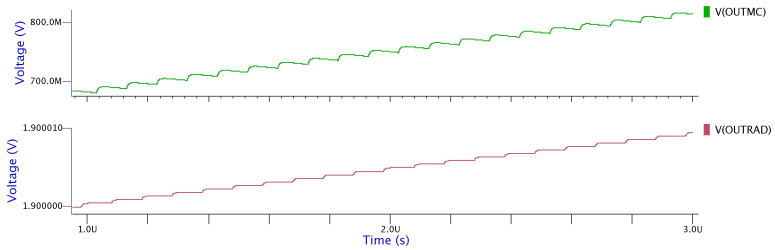
Charge of C_{MC} and C_{rad}

		ULP	Classic
t_{meas}	$[\mu s]$	2	2
$P_{comparators}$	$[\mu W]$	1.36	1.35
$P_{power-buffers}$	$[\mu W]$	191	210
$P_{control}$	$[\mu W]$	8	6.5
P_{outRad}	$[\mu W]$	1039	1425
P_{outMC}	$[\mu W]$	352	272
P_{in}	$[\mu W]$	2548	3152
P_{out}	$[\mu W]$	1391	1698
η	$[\%]$	54.6	54

Table B.2 - Charge of C_{MC} and C_{rad}



(a) ULP



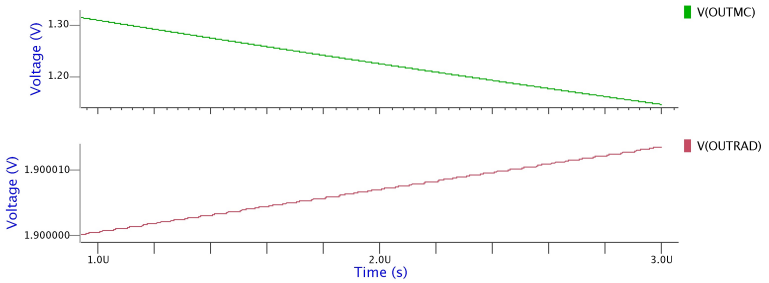
(b) Classical

Figure B.2 - Charge of C_{MC} and C_{rad}

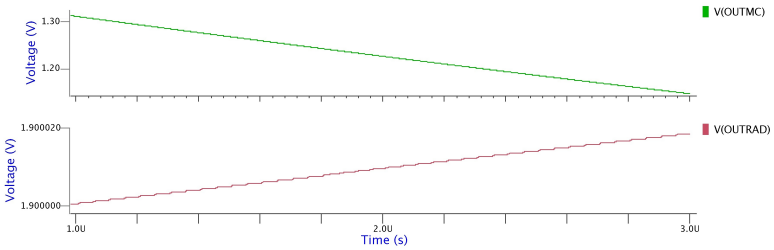
Charge of C_{rad} and discharge of C_{MC}

		ULP	Classic
t_{meas}	$[\mu s]$	2	2
$P_{comparators}$	$[\mu W]$	1.2	1.2
$P_{power-buffers}$	$[\mu W]$	300	183
$P_{control}$	$[\mu W]$	8	6.8
P_{outRad}	$[\mu W]$	2029	2836
P_{outMC}	$[\mu W]$	$7.7e^{-3}$	$9.2e^{-2}$
P_{in}	$[\mu W]$	3756	4927
P_{out}	$[\mu W]$	2029	2836
η	[%]	54	57.6

Table B.3 - Charge of C_{rad} and discharge of C_{MC}



(a) ULP



(b) Classical

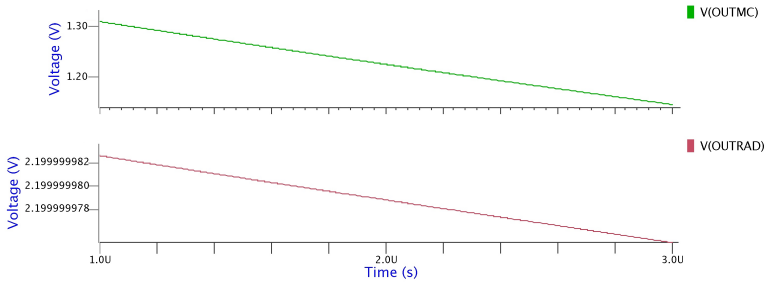
Figure B.3 - Charge of C_{rad} and discharge of C_{MC}

When the converter must send charges to C_{rad} but not to C_{MC}, i.e. when $V_{outRad} < V_{refRad}$ and $V_{outMC} < V_{refMC}$, it can devote 100% of its time to the charge of C_{rad}. By putting the MC in sleep mode, we can reduce its consumption. This means that it will require less charge packets, letting the converter in the state depicted in Figure B.3. In this manner, it is possible to reduce the charge time of the radio capacitor, reducing at the same time the radio consumption.

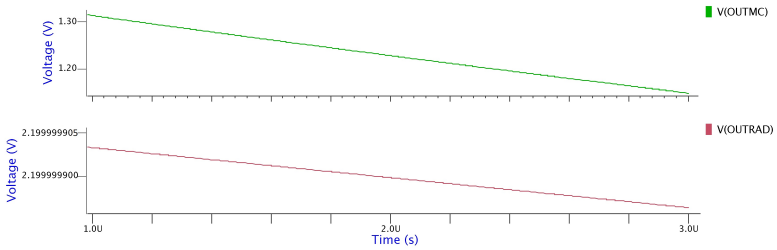
Discharge of C_{MC} and of C_{rad}

		ULP	Classic
t_{meas}	$[\mu s]$	2	2
$P_{comparators}$	$[\mu W]$	1	1
$P_{power-buffers}$	$[\mu W]$	$-6.2e^{-4}$	0.1
$P_{control}$	$[\mu W]$	$-2.7e^{-3}$	$-2.9e^{-3}$
P_{outRad}	$[\mu W]$	$-9.9e{-}2$	$-2.6e^{-2}$
P_{outMC}	$[\mu W]$	$1.3e^{-2}$	$5e^{-2}$
P_{in}	$[\mu W]$	8.6	8.7
P_{out}	$[\mu W]$	$-8.6e{-}2$	$2.48e^{-3}$
η	$[\%]$	–	–

Table B.4 - Discharge of C_{MC} and of C_{rad}



(a) ULP



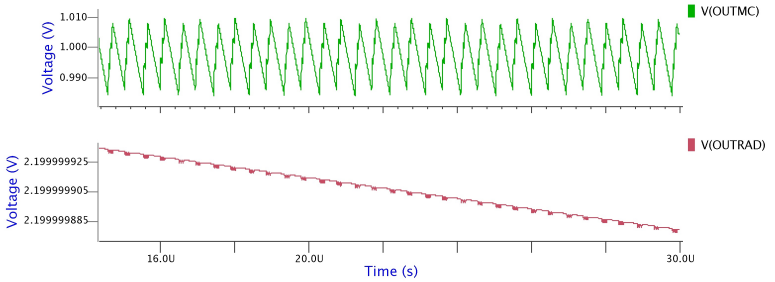
(b) Classical

Figure B.4 - Discharge of C_{MC} and of C_{rad}

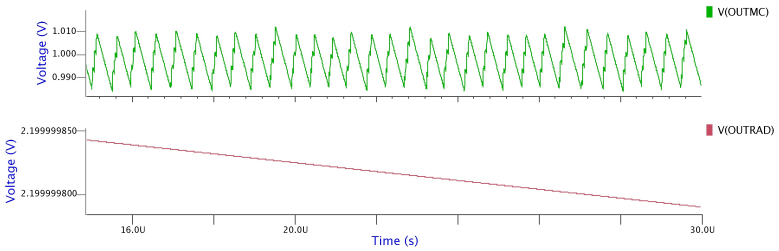
Regulation of C_{MC} and discharge of C_{rad}

		ULP	Classic
t_{meas}	$[\mu s]$	15	15
$P_{comparators}$	$[\mu W]$	1.63	1.6
$P_{power-buffers}$	$[\mu W]$	27.2	81
$P_{control}$	$[\mu W]$	2.79	2.3
P_{outRad}	$[\mu W]$	$-2.3e^{-2}$	$-2.66e^{-2}$
P_{outMC}	$[\mu W]$	208	206
P_{in}	$[\mu W]$	358	409
P_{out}	$[\mu W]$	208	206
η	[%]	58.2	50.4

Table B.5 - Regulation of C_{MC} and discharge of C_{rad}



(a) ULP



(b) Classical

Figure B.5 - Regulation of C_{MC} and discharge of C_{rad}

APPENDIX C

Contents of the CD-ROM

Matlab : - transfer capacitors - output capacitors

APPENDIX D

Layout

Components design

The transfer capacitor was designed in section 3.2.1.

The size of each switch is determined so that the switch is able to let the current flow in the worst case. The worst case depends on the voltages across the switch and on the period available to complete the transfer.

The sizes of the different components are summed up in Table **??**

TABLE AVEC TOUTES LES TAILLES : capas(valeur+surface) + switch(W,L)

D.1 Base Cells

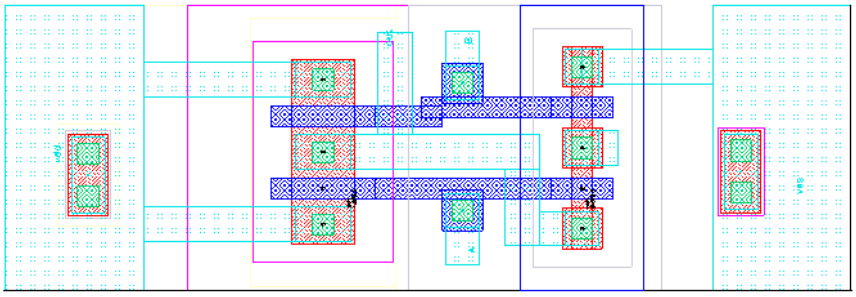


Figure D.1 - NAND

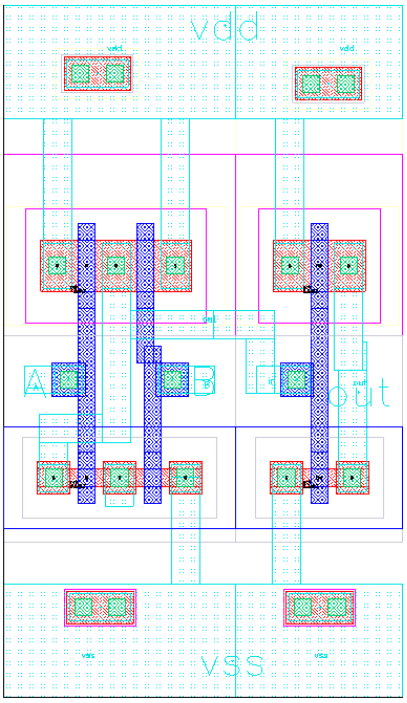


Figure D.2 - AND

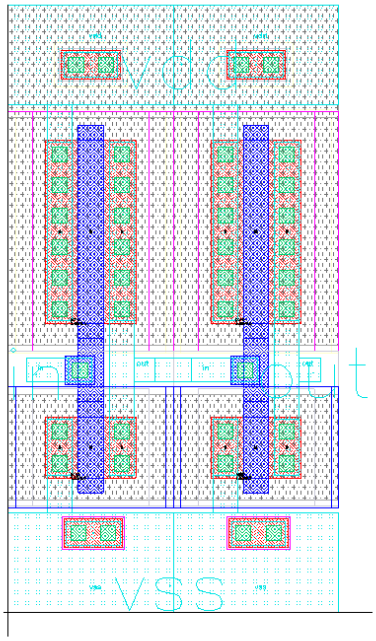


Figure D.3 - BUF5VX1

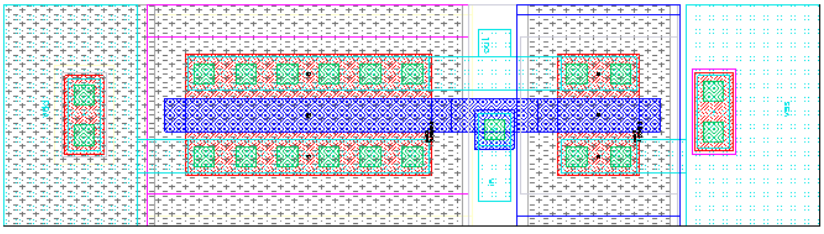
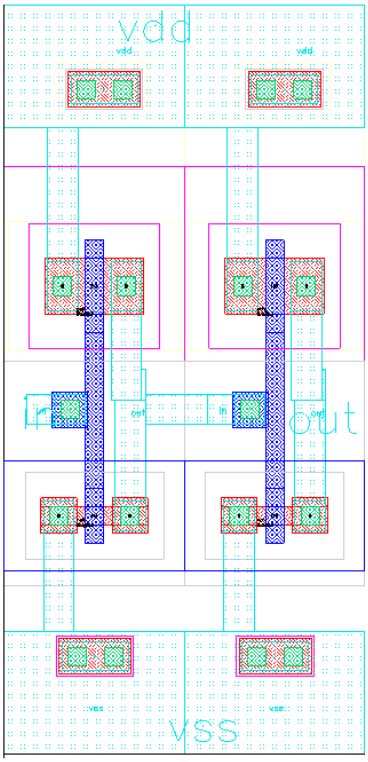
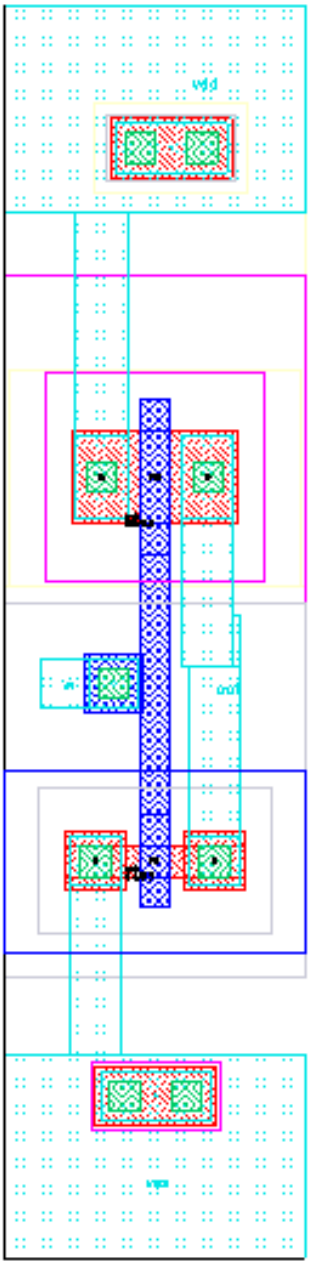


Figure D.4 - INV5VX1



(a) BUFX1



(b) INVX1

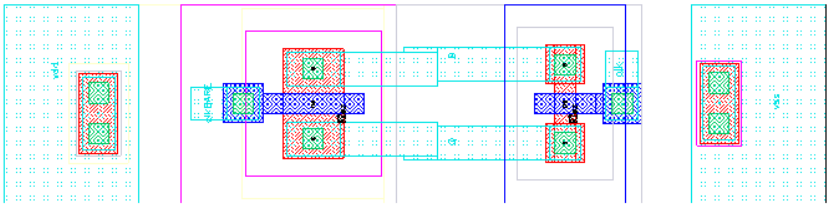


Figure D.5 - Mypassant

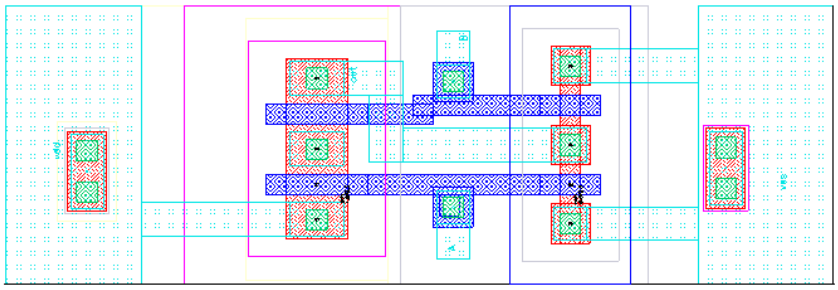


Figure D.6 - NOR

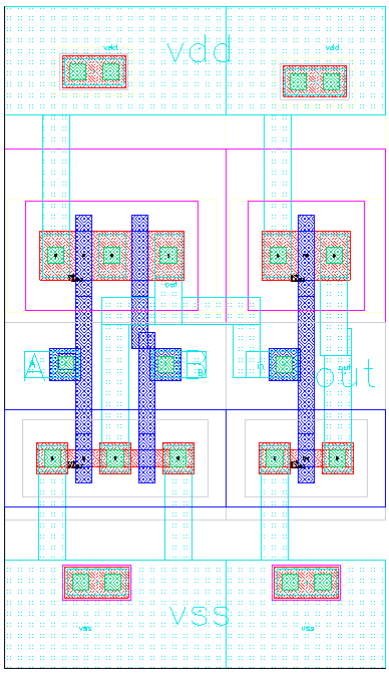


Figure D.7 - OR

D.2 Clock generation

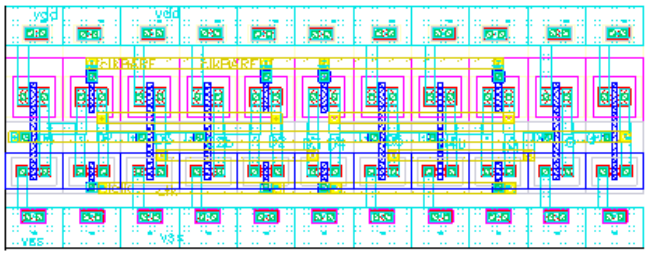


Figure D.8 - Mydivf2

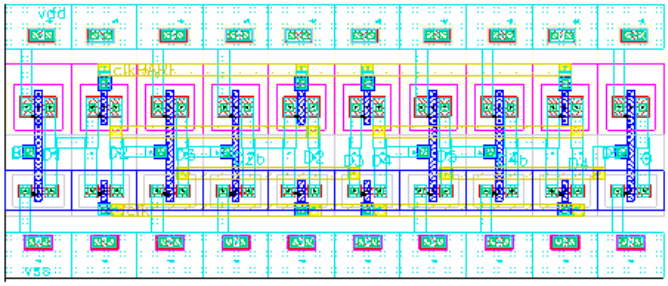


Figure D.9 - Myreg

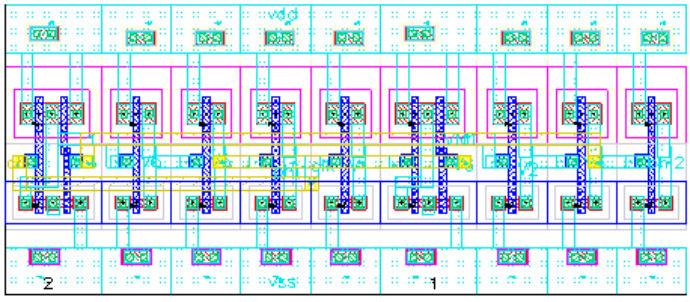


Figure D.10 - NOCG

D.3 Comparator

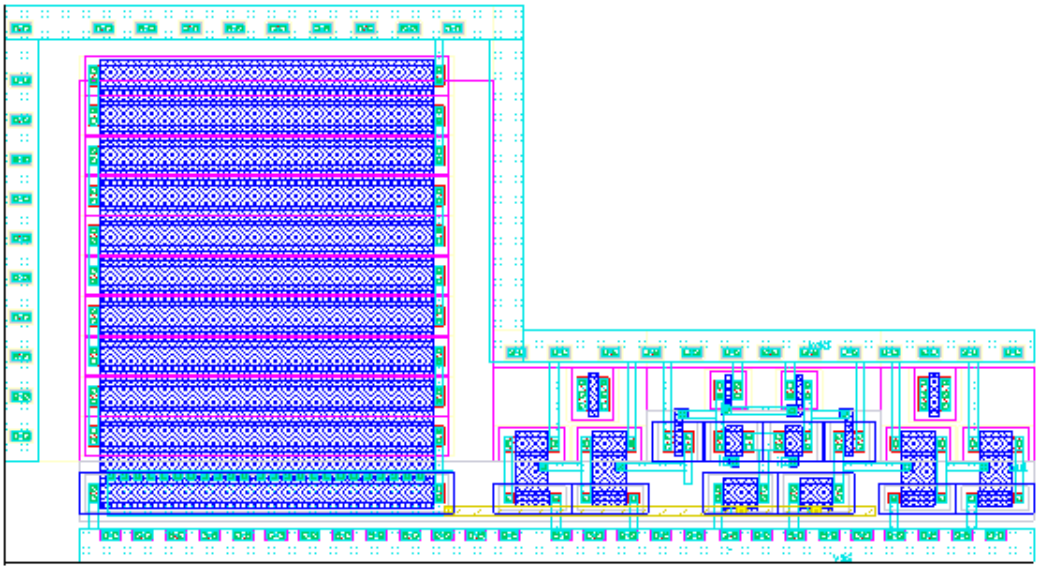


Figure D.11 - comparator

D.4 Control

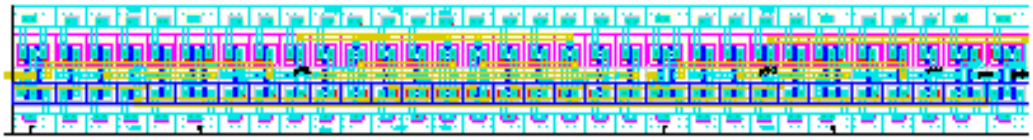


Figure D.12 - clkgenerator

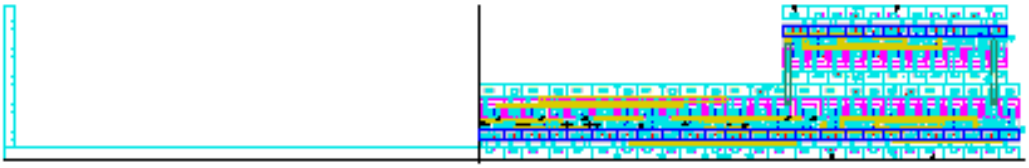


Figure D.13 - controlCircuitULP

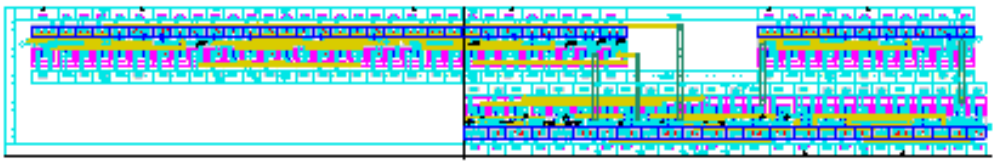
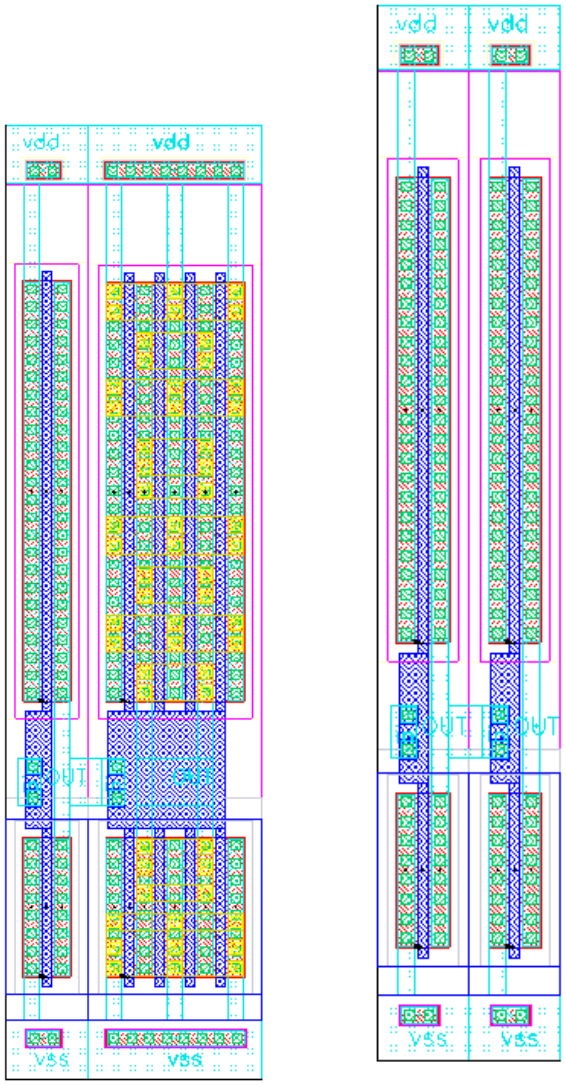


Figure D.14 - controlClkULP

D.5 Power Blocs



(a) Pbloc1ULP (b) Pbloc2ULP

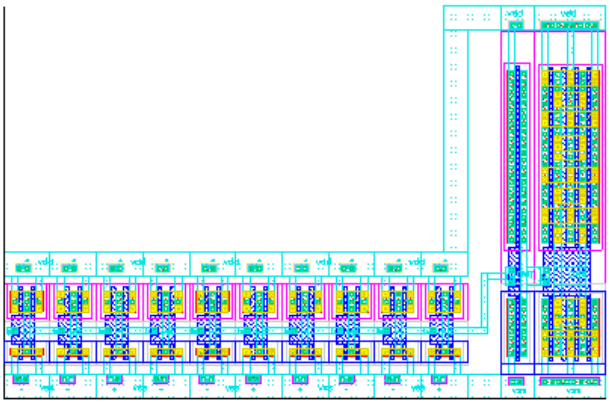


Figure D.15 - Pbloc3ULP

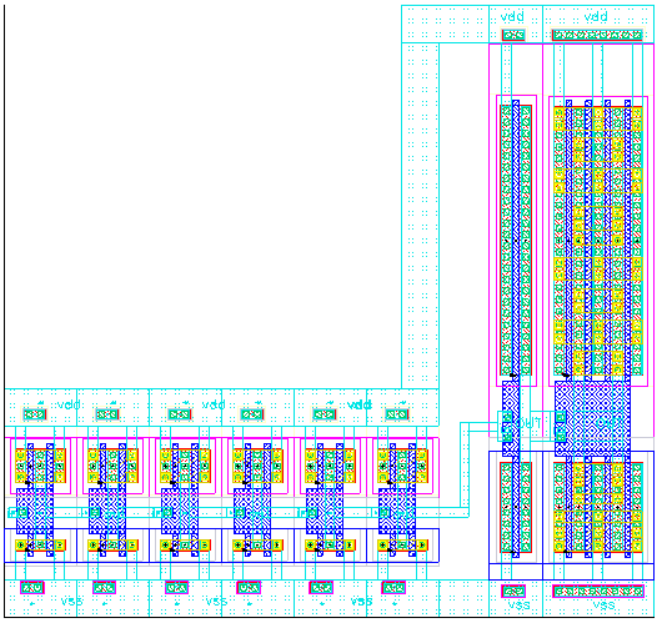


Figure D.16 - Pbloc4ULP

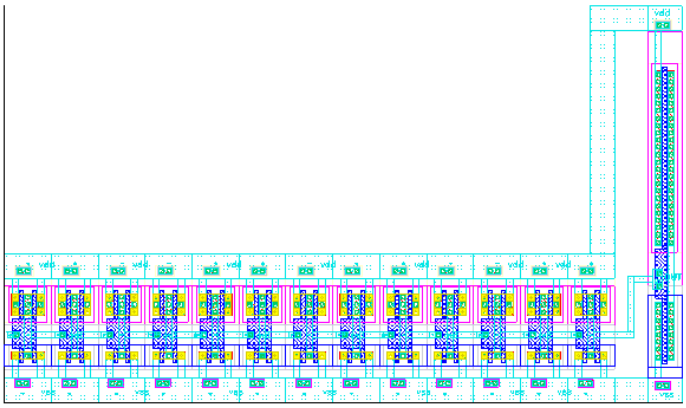


Figure D.17 - Pbloc5ULP

D.6 Netlist

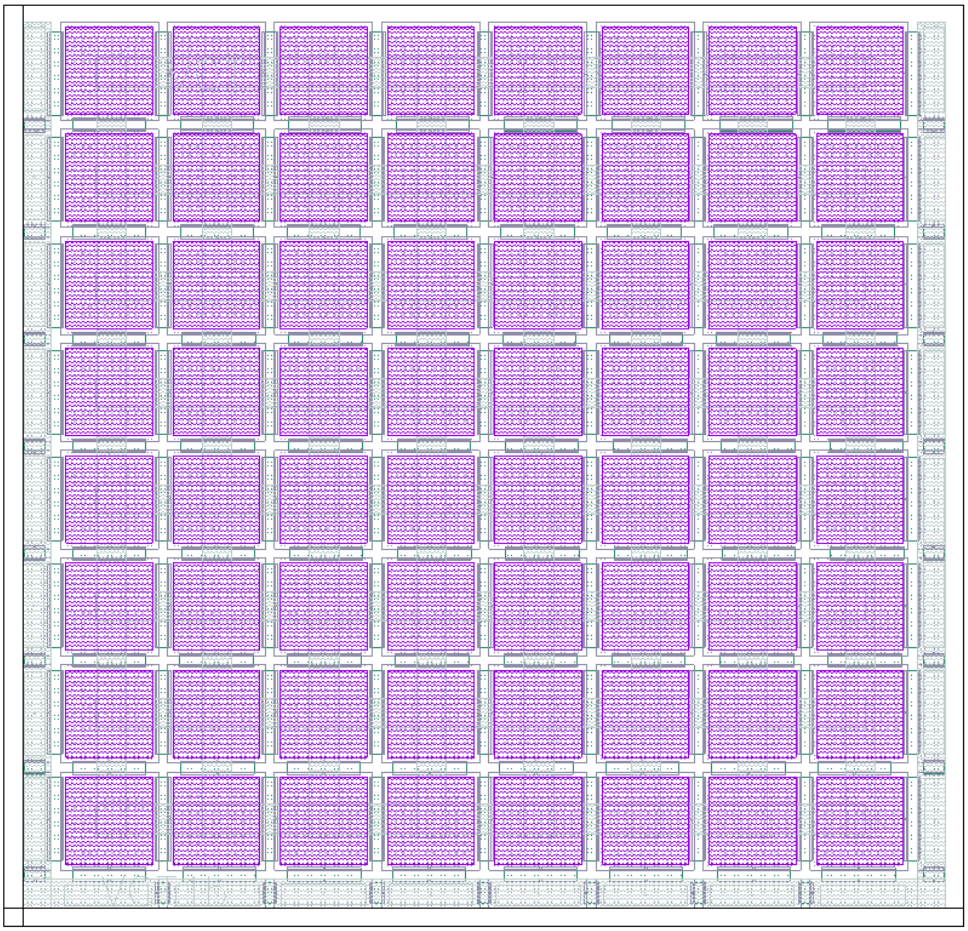


Figure D.18 - CT1

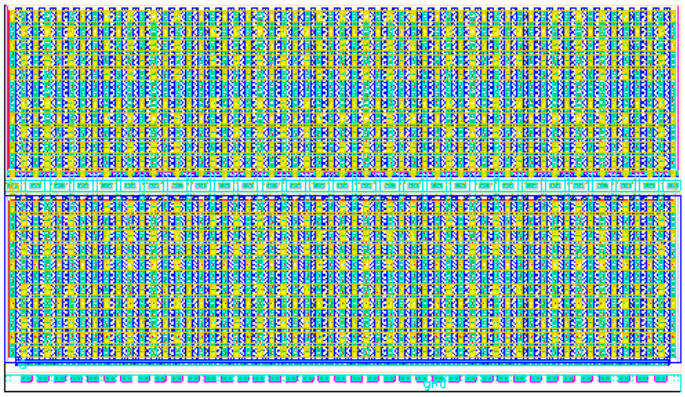


Figure D.19 - NULP1

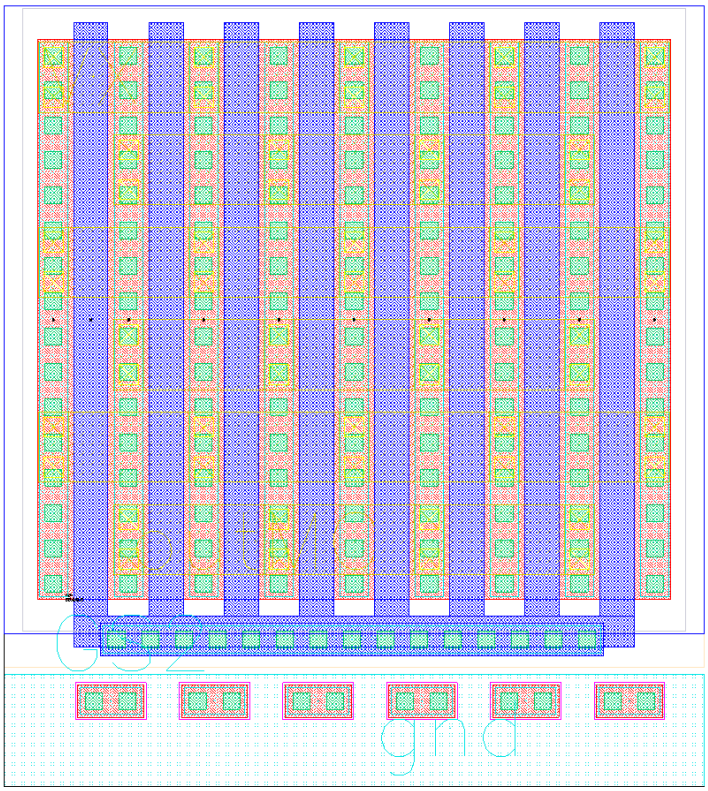


Figure D.20 - M2

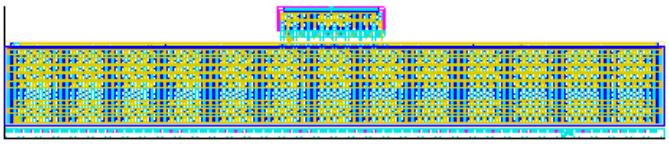


Figure D.21 - PULP3

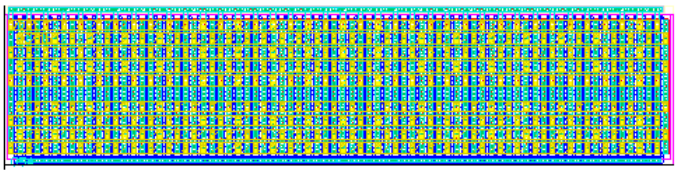


Figure D.22 - M4

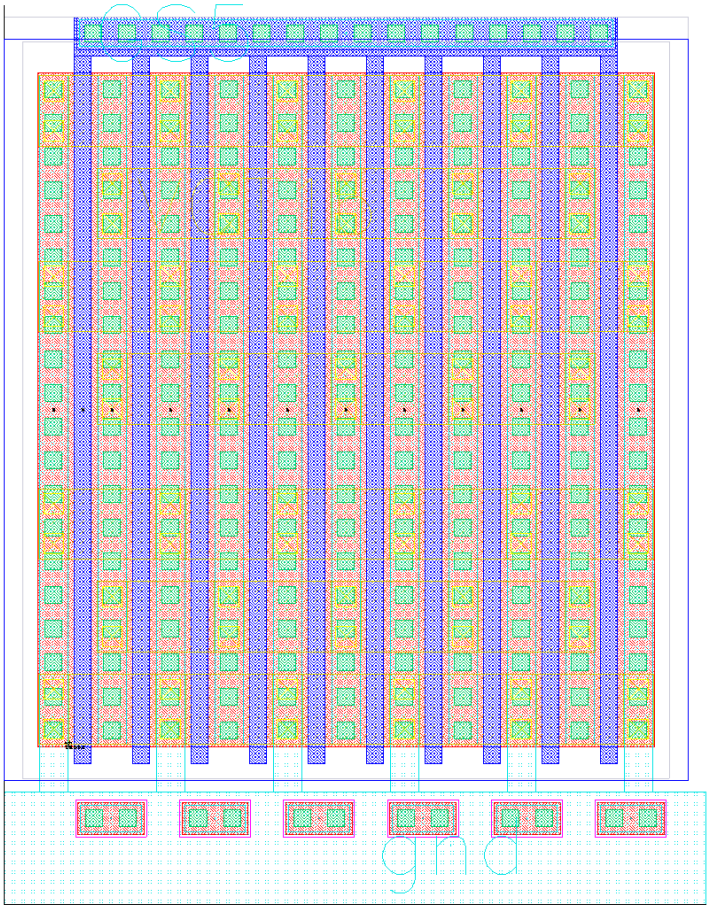


Figure D.23 - M5