

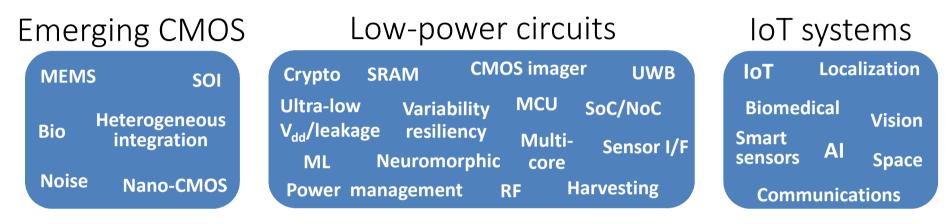
Electronic circuits & systems (ECS) research group introduction

Prof. David BOL & Prof. Denis Flandre





Research scope of ECS group



Level of abstraction

Professors:

- Prof. David Bol
- Prof. Denis Flandre
- Prof. Jean-Didier Legat
- 10+ researchers

Industrial collaborations:

ST-Micro, IMEC, e-peas, EADS, ACIC, Thales, Cissoid, CEA-Leti, AMS, iStar, Deltatec, Samsung, Honeywell, TowerJazz, intoPix, Siemens, nSilition, Infineon, Synergiam, ...

Last 10 years:

- 5 patents
- 150+ papers
- 3 awards
- 3 spin-off launched
- 10+ PhD graduation

2

Within UCL ICTEAM institute...

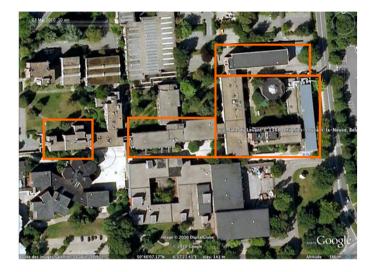
https://uclouvain.be/fr/node/1991 🛛 🚳





ICTEAM institute

- Three research divisions
 - Electrical Engineering (ELEN)
 - Computing Science Engineering (INGI)
 - Mathematical Engineering (INMA)
- About
 - 40+ professors
 - 200+ researchers
 - 20 computer scientists and technicians
 - 150+ publications per year
- WELCOME technology platform
 → measurement facility
- Full access to the WINFAB platform
 → nanofabrication facility









Research directions at ICTEAM

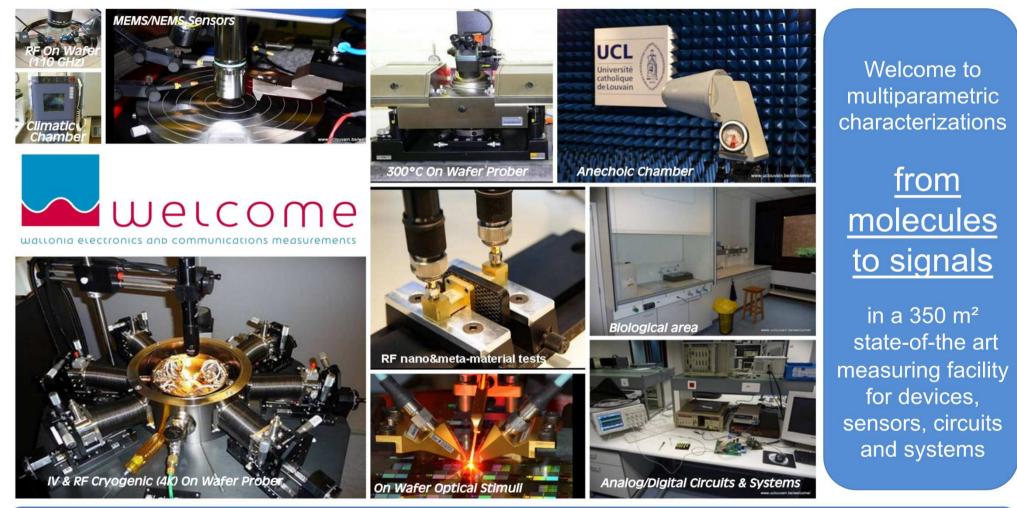
ICTEAM carries both basic and applied world-class research in various domains of Information and Communication Technologies, Electronics and Applied Mathematics.

- Applied Mathematics
- Biomedical Engineering
- Communication Systems and Networks
- Cryptography and Information Security
- Dynamical Systems, Control and Optimization
- Electronic Circuits and Systems
- Large Graphs and Networks
- Machine Learning and Artificial Intelligence
- Micro and Nano Process Technologies and Systems
- Microwave Engineering and Applied Electromagnetism
- Signal and Image Processing
- Software Engineering and Programming Systems



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Wallonia Electronics & Communications Measurements



2.13 MEuros equipment over 10 years – over 120 yearly users from 4 corners of the globe open to research, PhD/Master studies, industry http://www.uclouvain.be/welcome info-welcome@uclouvain.be

23-Apr-18



WINFAB : Micro- and nano-fabrication at UCL

• Cleanroom: ~1000 m² on two levels Critical work areas in ISO5 (stand-by)

« < 10 particules of 100 nm / feet³ of air »



Activities : more than 50 state-of-the-art equipments,
 ~80 active researchers, more than 20 R&D projects

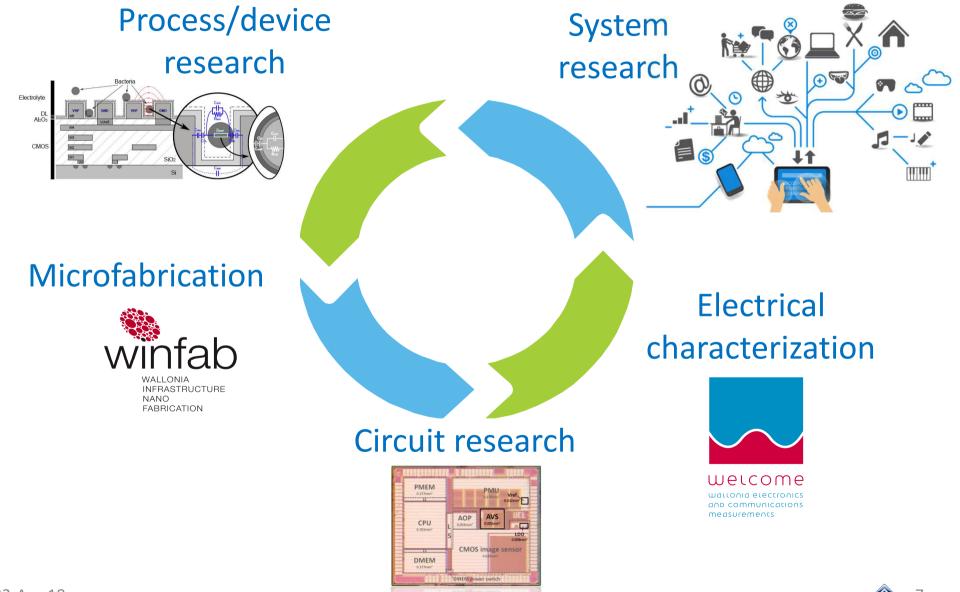
Level 1: « Ballroom »

Level 0 : « Support Area »





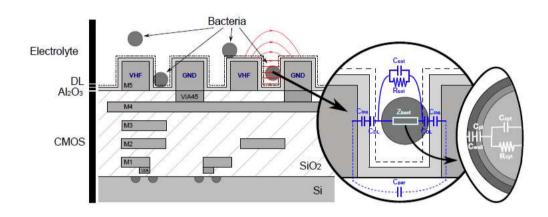




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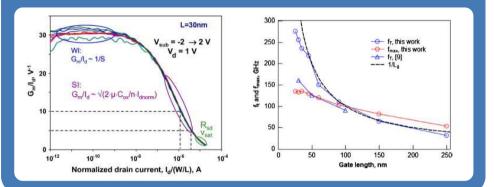


EMERGING CMOS Characterization, modeling, & design enablement

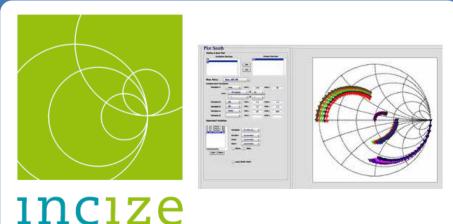


Characterization and modeling of CMOS technologies

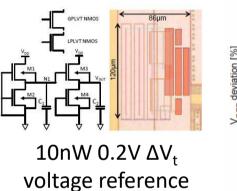
Analog/RF perfs of ultimate MOSFETs [Arshad, SSE, 2014][Makovejev, SSE, 2015]

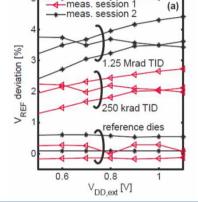


Characterization tools [incize, 2014]



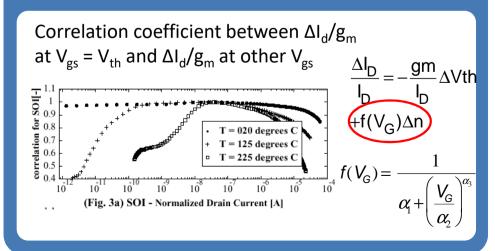
Radiation effects [de Vos, S3S, 2014]





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Effects of wide temperature range

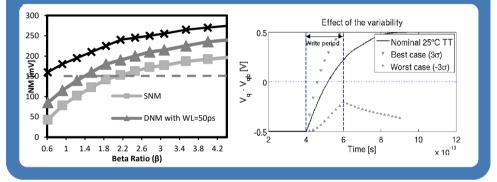




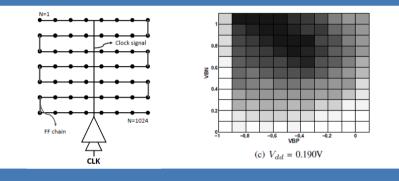


Design enablement

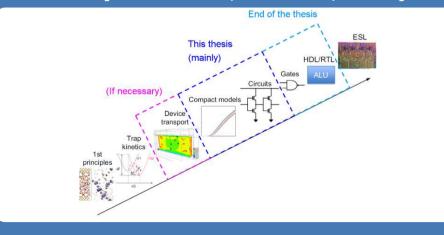
Assessment of embedded memories [Haine, FETCH, 2015][Elthakeb, ISCAS, 2015]



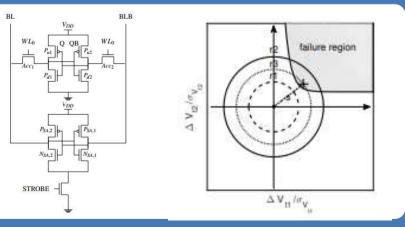
Minimum functional voltage characterization [Bernard, PATMOS, 2014]



Compact modeling of random telegraph noise [Van Brandt, MOS-AK, 2017]



Fast statistical assessment of high-σ circuit characteristics [Haine, DATE, 2018]

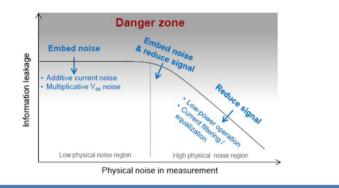




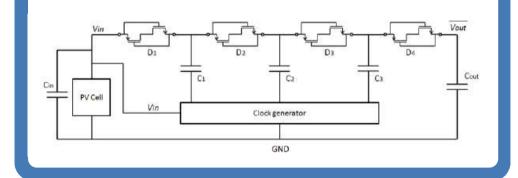


New device/circuit interaction concepts

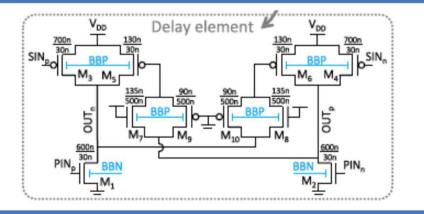
Noise exploitation for secure crypto circuits [Kamel, SPACE, 2016]



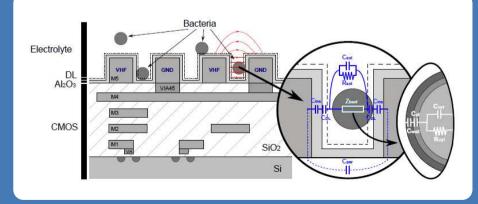
SOI co-integration of PV cell with interface circuit [Gosset, SOI conf., 2011]



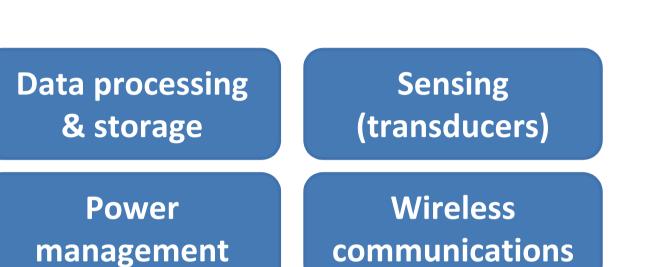
Back-gate controlled circuits in FD SOI [de Streel, JSSC, 2017]



Capacitive bacteria detection onto CMOS [Couniot, TCAS-II, 2015]







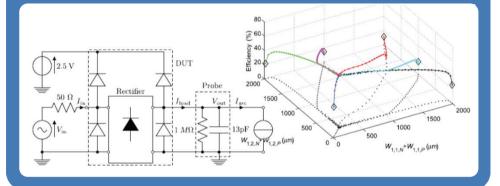
LOW-POWER CIRCUIT DESIGN Methodologies and IP blocks in the 4 IC functions



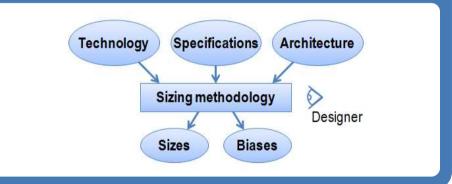


Low-power design methodologies

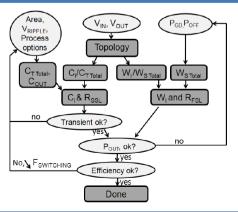
Sizing methodology for AC/DC rectifiers [Haddad, JSSC, 2016]



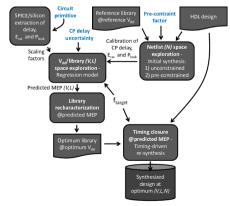
G_m/*I_d* sizing methodology for analog primitives [*Pollissard, AICSP, 2013*]



Sizing methodology for DC/DC converters [*De Vos, TCAS-I, 2014*]



Synthesis flow for ultra-low-voltage logic [Bol, TCAS-II, 2012]

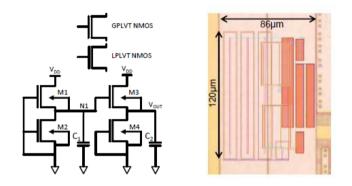




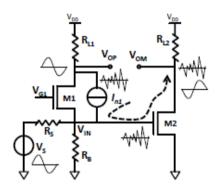
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Low-power analog/mixed-signal building blocks

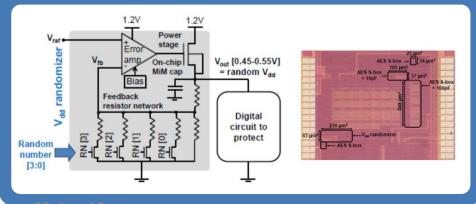
10nW 0.2V voltage reference [de Streel, S3S, 2015]



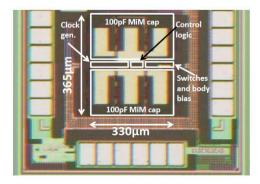
2mW 10GHz wideband low-noise amplifiers [*Gimeno, S3S, 2017*]



V_{dd} randomizer for secure crypto circuits [Kamel, SPACE, 2016]



Multi-mode SC DC/DC converters [De Vos, SubVt, 2012][Clerc, ISSCC, 2015]



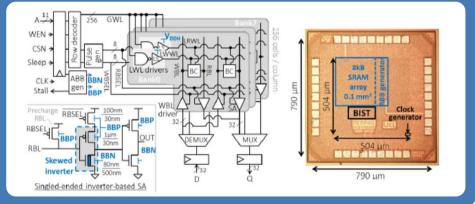
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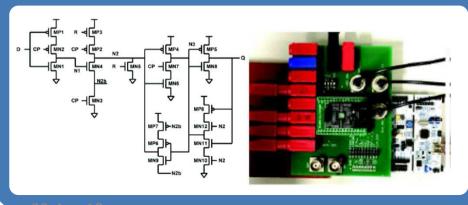


Low-power digital design: architecture and techniques

ULP 0.4V 80-MHz SRAM [Haine, ESSCIRC, 2017]

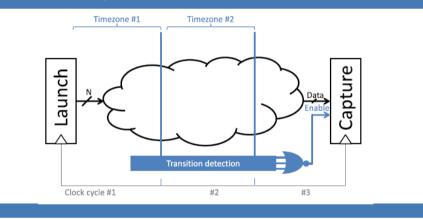


0.4V retentive TSPC flip-flops [Stas, ISCAS, 2017][Stas, TCAS-I, 2017]

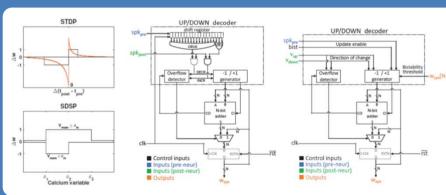


Data-dependent operation speedup technique [Botman, TVLSI, 2014]

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Spiking neural networks with on-line learning [Frenkel, ISCAS, 2017]



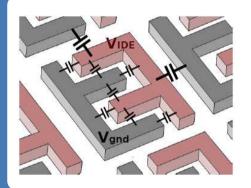
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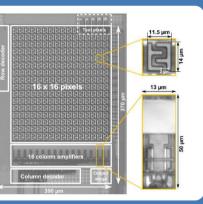




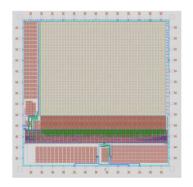
Low-power sensing circuits

Pixel-based biosensors for singlebacteria detection [Couniot, TBCAS, 2015]

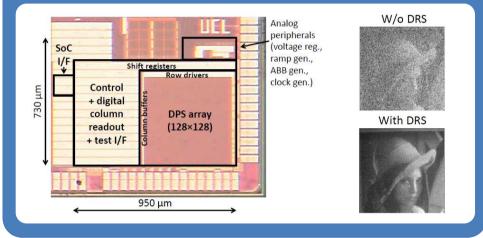




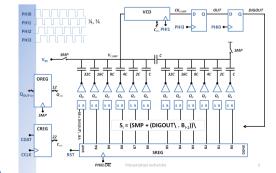
Computational CMOS imagers [Haine, to appear]

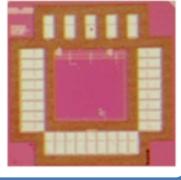


3µW 0.5V CMOS imager [*Bol, VLSI, 2014*]



0.5µW time-based ADC [Pollissard, Ph.D, 2013]





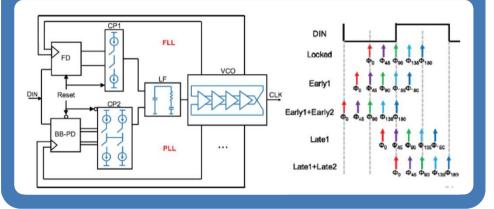
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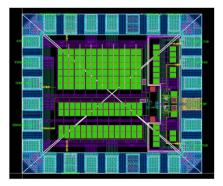
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Low-power wireless/wireline communications

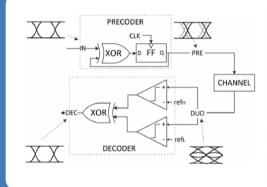
Low-power half-rate dual-loop clock recovery [*Gimeno, LASCAS, 2018*]

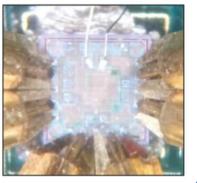


Impulse-radio UWB pulse-shaping emitter [Schramme, to appear, 2018]



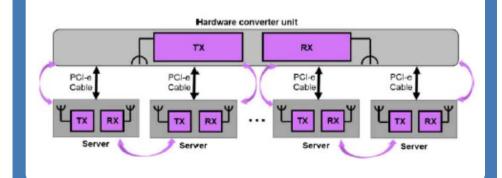
Wireline 10-Gbps duobinary transceiver [*Aguirre, TIE, 2018*]





17

Wireless multi-Gbps transceivers [Gimeno, TCAS-I, 2018]



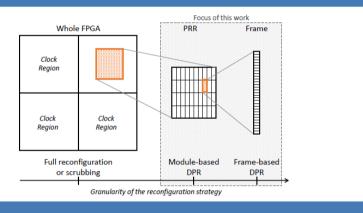
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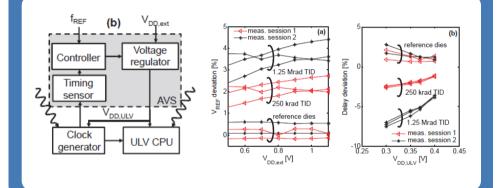


Radiation-hard low-power circuit design

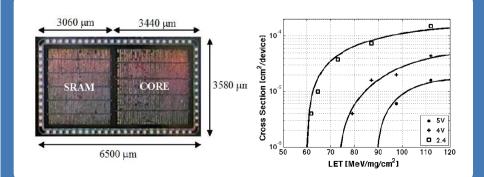
Rad-hard design on FPGA for low-power space applications [Frenkel, ReSoC, 2015]



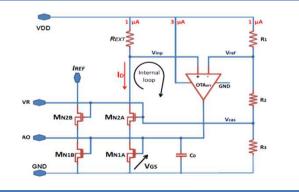
Adaptive circuits compensating total ionizing doze [*De Vos, S3S, 2014*]



PVT-Rad-hard digital circuits [Manet, RADECS, 2009]



PVT-Rad-hard analog circuits [Boufouss, PhD, 2014]



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INTERNET-OF-THINGS SYSTEMS Smart sensors for sustainable IoT

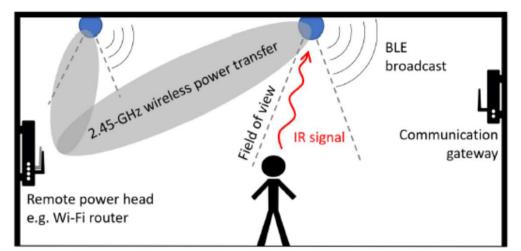


team Institute of Information and Communication Technologies, UCL **Electronics and Applied Mathematics Electronics Circuits and Systems Deployment:** Challenges for a sustainable IoT: carbon footprint & natural Energy harvesting resource pressure, ecotoxitiy **Operation:** spectrum congestion & low-power design 2 3 data deluge sssς security flaws Maintenance: 5 battery replacement [D. Bol et al., IEEE S3S, 2015] 10+ year Sensing 1 Power system Agile RF management communications RF Data processing 3 Computationally-Compression 0 0 and physicallyand classification 200111100011 secure operation



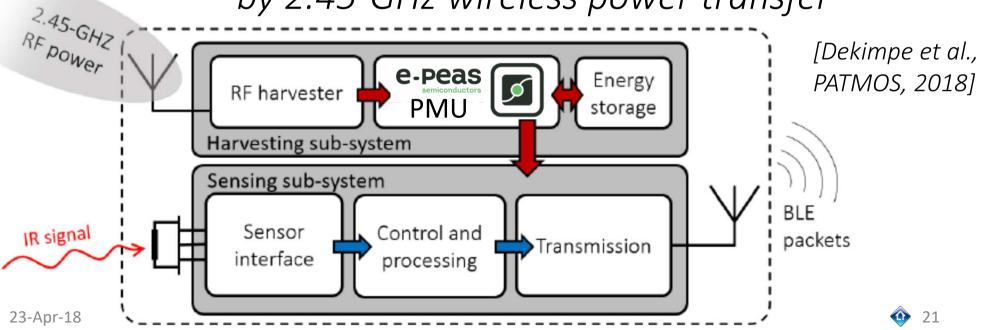


IoT smart sensor example: room occupancy detection



A battery-less BLE motion detector supplied

by 2.45-GHz wireless power transfer







Battery-less BLE motion detector supplied by 2.45-GHz WPT

Average power consumption [µW]

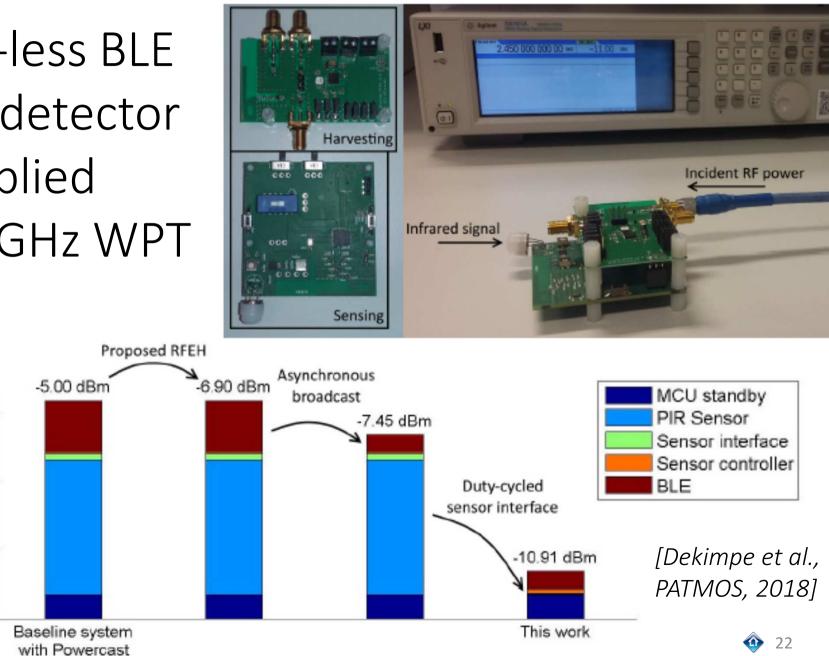
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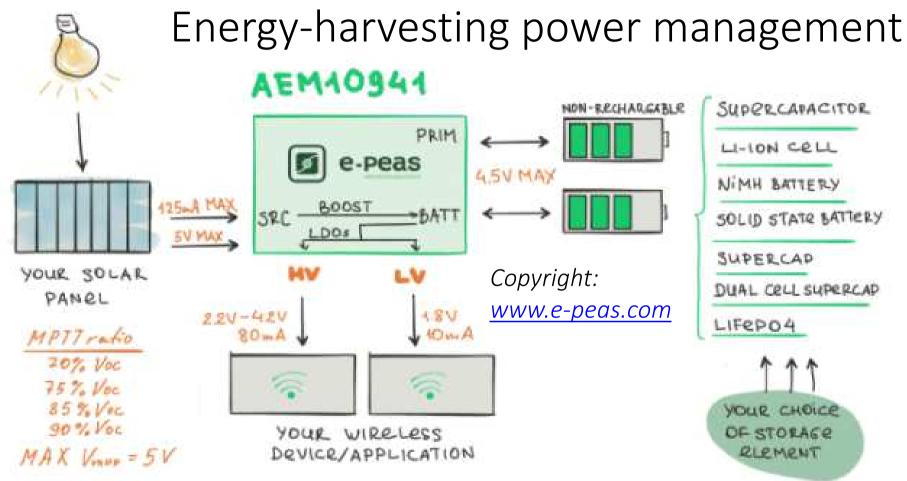
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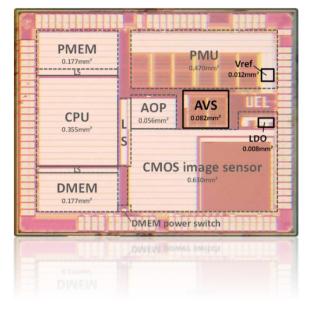




- 9 years active research lead to the creation of e-peas company in 2014
- e-peas' AEM product line offers power management units (PMICs) for solar, thermal, vibration and RF energy harvesting
- Best-in class efficiency and minimum input power







CHIP EXAMPLES From MCUs to mixed-signal SoCs



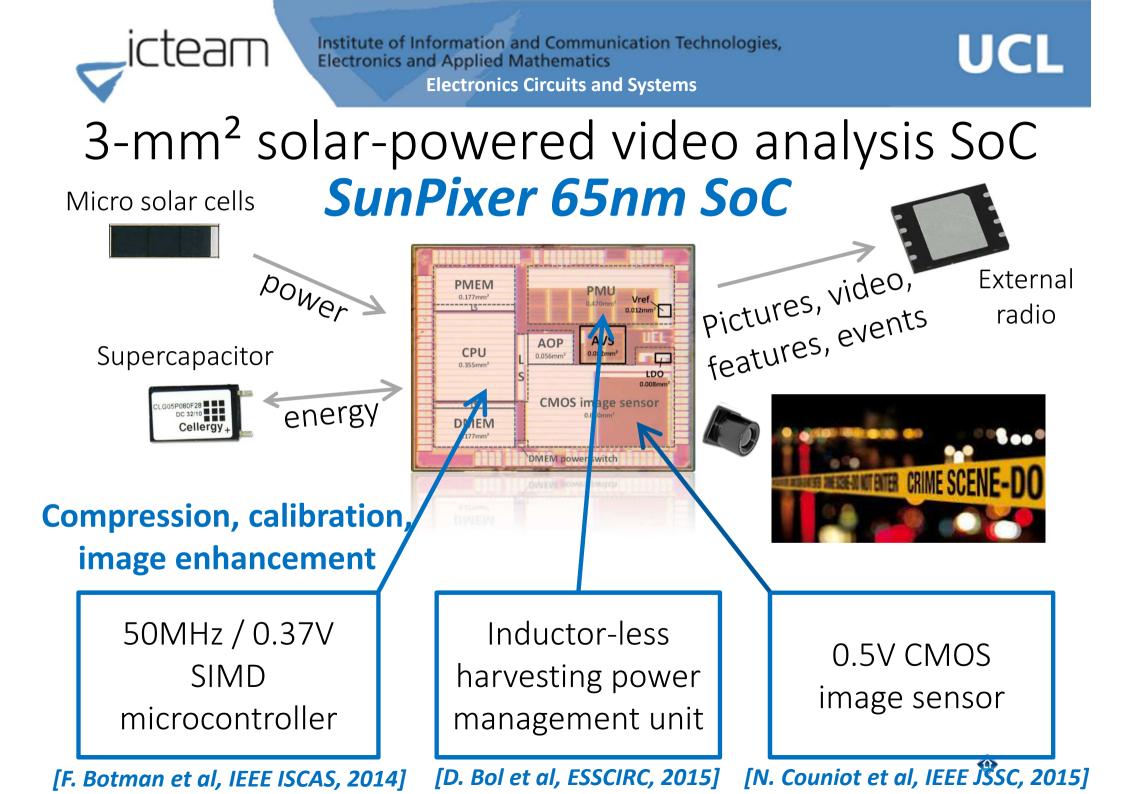


SleepWalker 65nm microcontroller SoC

- Low system CO₂ footprint
 - \checkmark low die area
 - \checkmark few off-chip components
- Energy-harvesting operation
 - ✓ low active energy
 - ✓ adaptive voltage scaling 0.32-0.48V
- Compatibility with commercial components
 - ✓ MSP430 instruction set, same memory capacity and peripherals
 - \checkmark 25MHz speed robust under industrial conditions

DC/DC converter 1.0-1.2V	PMEM 6T SRAM 1.0-1.2V	
AOP 1.0- 1.2V	CPU + I\$ 0.32-0.48V (AVS)	
	2122212 ′5μm	

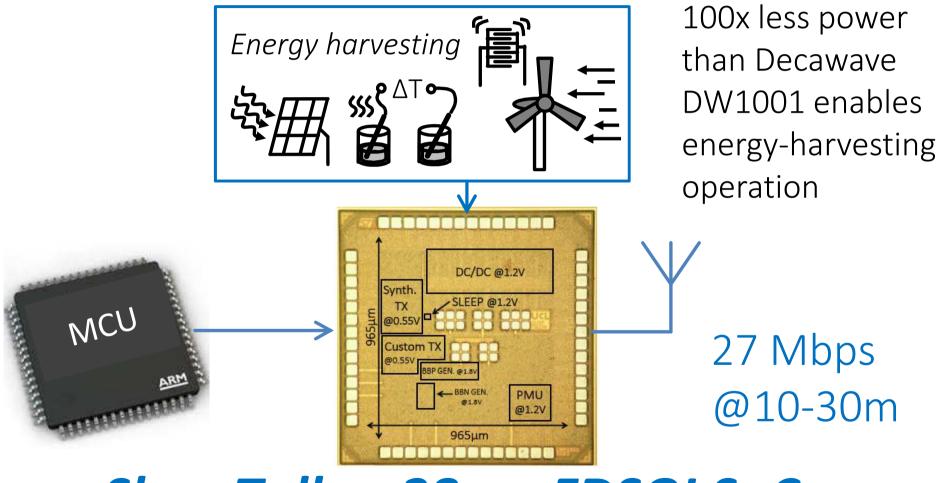
MSP430	This work [Bol, JSSC, 2013]	MIT (best research) [Kwong, JSSC, 2009]	TI (best commercial) [Zwerg, ISSCC, 2011]
Speed [MHz]	25 @0.4V	0.3 @0.5V	24 @1.5V
Energy [µW/MHz]	7	27.3	164
CO ₂ footprint [kg/1000 units]	14	47	83







700-µW IEEE 802.15.4a RF transmitter SoC



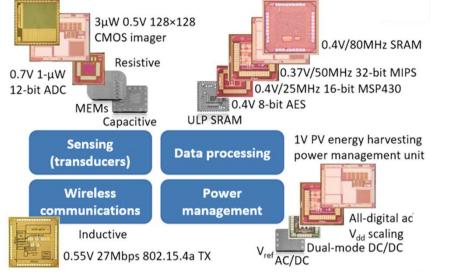
SleepTalker 28nm FDSOI SoC

[G. de Streel et al, IEEE Symp. VLSI, 2016] [G. de Streel et al, IEEE JSSC, 2017]

Institute of Information and Communication Technologies, Electronics and Applied Mathematics

Electronics Circuits and Systems





- Cutting-edge research @ UCL-ECS from process to circuits to systems
- Tens of working silicon chips from building IP blocks to full SoCs in 1µm, 0.18-0.13µm, 65nm, 28nm CMOS Strong added value @system/application levels when off-the-shelf components limit the specs/performances

