Electronic Circuits and Systems research group at UCL

David BOL, Denis FLANDRE, Jean-Didier LEGAT, François-Xavier STANDAERT
ICTEAM institute

• Three research divisions
  – Electrical Engineering (ELEN)
  – Computing Science Engineering (INGI)
  – Mathematical Engineering (INMA)

• About
  – 40 professors
  – More than 200 researchers
  – 20 computer scientists and technicians
  – More than 150 publications per year

• WELCOME technology platform
  → measurement facility

• Full access to the WINFAB platform
  → nanofabrication facility
Research directions at ICTEAM

ICTEAM carries both basic and applied world-class research in various domains of Information and Communication Technologies, Electronics and Applied Mathematics.

- Applied Mathematics
- Biomedical Engineering
- Communication Systems and Networks
- Cryptography and Information Security
- Dynamical Systems, Control and Optimization
- **Electronic Circuits and Systems**
  - Large Graphs and Networks
  - Machine Learning and Artificial Intelligence
  - Micro and Nano Process Technologies and Systems
  - Microwave Engineering and Applied Electromagnetism
  - Signal and Image Processing
  - Software Engineering and Programming Systems
Research scope of ECS group

Process
- MEMS
- Bio
- SOI
- Flex
- Heterogeneous integration
- CNTs
- Nano-CMOS

Circuits
- Crypto
- SRAM
- CMOS imager
- UWB
- Ultra-low
- Variability
- Resiliency
- Power management
- Multi-core
- SoC/NoC
- ADC
- Sensor I/F
- Harvesting

Systems
- IoT
- Localization
- Biomedical
- Vision
- RFID
- Space
- Communications

Level of abstraction

Professors:
- Pr. D. Flandre
- Pr. D. Bol
- Pr. J.-D. Legat
- Pr. F.-X. Standaert

Industrial collaborations:
- ST-Micro, IMEC, EADS, Thales, Cissoid, CEA-Leti, Deltatec, AMS, Samsung, iStar, ACIC, Honeywell, TowerJazz, Siemens, nSilition, Infineon, ...

Last 10 years:
- 5 patents
- 150+ papers / 3 awards
- 3 spin-off launched
- 1 ERC
- > 10 PhD graduation

EMERGING CMOS TECHNOLOGIES –

Characterization, modeling, design enablement and new concepts
Characterization and modeling

**Analog/RF perfs of ultimate MOSFETs**
[Arshad, SSE, 2014][Makovejev, SSE, 2015]

**Radiation effects**
[Alvarado, TNS, 2012]

**Characterization tools**
[incize, 2014]

**Wideband and non linear effects**
[Emam, AVL, 2012]
Design enablement

SRAM dynamic/statistical assessment
[Haine, FETCH, 2015][Elthakeb, ISCAS, 2015]

Pre-silicon compact MOSFET models
[Bol, SOI conf., 2011]

Minimum functional voltage characterization
[Bernard, PATMOS, 2014]

Digital power optimization techniques
[Bol, JLPEA, 2011][de Streel, S3S, 2013]
New concepts

Capacitive bacteria transduction onto CMOS [Couniot, TCAS-II, 2015]

Crosstalk mitigation for wireless SoCs [Roda Neve, Ph.D, 2012]

MEMS/CMOS co-integration for new sensors [André, J. Sensors, 2010]

SOI co-integration of PV cell with interface circuit [Gosset, SOI conf., 2011]
LOW-POWER CIRCUIT DESIGN FOR HIGH-PERFORMANCE APPLICATIONS – Methodologies and IP blocks
Low-power design methodologies

Sizing methodology for AC/DC rectifiers [Gosset, JETCAS, 2011]

$G_m/I_d$ sizing methodology for analog primitives [Pollissard, AICSP, 2013]

Sizing methodology for DC/DC converters [De Vos, TCAS-I, 2014]

Synthesis flow for ultra-low-voltage logic [Bol, TCAS-II, 2012]
Low-power analog/mixed-signal building blocks

10nW 0.2V voltage reference [de Streel, S3S, 2015]

Sub-mW 0.5V wideband low-noise amplifier [de Streel, S3S, 2015]

Single-pulse generator for UWB localization [Al Kadi Jazairli, ICUWB, 2010]

Multi-mode SC DC/DC converters [De Vos, SubVt, 2012][Clerc, ISSCC, 2015]
Low-power digital design: architecture and techniques

Variable-width SIMD processor [Botman, ISCAS, 2014]

Data-dependent operation speedup technique [Botman, TVLSI, 2014]

Pulsed flip-flop for digital standard-cell libraries [Bernard, S3S, 2013]

Hybric NoCs for real-time MPSoC applications [Kuti, RecoSoC, 2012]
Radiation-hard low-power circuit design

Rad-hard design on FPGA for low-power space applications [Frenkel, ReSoC, 2015]

Adaptive circuits compensating total ionizing dose [De Vos, S3S, 2014]

PVT-Rad-hard digital SOI circuits [Boufouss, PhD, 2014]

PVT-Rad-hard digital circuits [Manet, RADECS, 2009]
Low-power sensing circuits

Pixel-based biosensors for single-bacteria detection [Couniot, TBCAS, 2015]

Monolithic pixel sensor for particle instrumentation [Soung Lee, JI, 2012]

3µW 0.5V CMOS imager [Bol, VLSI, 2014]

0.5µW time-based ADC [Pollissard, Ph.D, 2013]
PHYSICALLY-SECURE CIRCUITS AND LIGHTWEIGHT CRYPTOGRAPHY
Secure and crypto circuits and systems

0.4V AES coprocessor for secure RFIDs [Hocquet, JCEN, 2011]

<table>
<thead>
<tr>
<th>AES coprocessor</th>
<th>128-bit encryption/decryption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm LP CMOS – 7 metal layers</td>
</tr>
<tr>
<td>Silicon area</td>
<td>135 μm × 135 μm (core)</td>
</tr>
<tr>
<td>Package</td>
<td>CQFP 44</td>
</tr>
<tr>
<td>Vdd range</td>
<td>0.32–1.2V (core) / 1.2V (I/O)</td>
</tr>
<tr>
<td>Max. frequency</td>
<td>890 kHz @0.4V</td>
</tr>
<tr>
<td>Power</td>
<td>0.85μW @0.4V</td>
</tr>
</tbody>
</table>

IP block protection [Kerckhof, HOST, 2013]

Energy-driven lightweight crypto implementations [Kerchof, CHES, 2012]

Physically-unclonable functions (PUFs) [Parusinski, WESS, 2013]

![Physical function system (PFS)](image_url)
Side-channel attacks and countermeasures

Impact of nanoscale variability and leakages [Renauld, Eurocrypt, 2011]

Fault attacks on low-power HW [Barenghi, TETC, 2014]

SCA security evaluation from SPICE simulations [Kamel, JCEN, 2014]

Dynamic-differential logic for secure computation [Kamel, JLPEA, 2012]
INTERNET-OF-THINGS SYSTEMS – 
Sustainability aspects, energy harvesting and green SoCs
Sustainability ICT aspects

**Application-aware LCA [Bol, ISSST, 2011]**

- Energy
- Materials
- Water
- Chip assembly
- Application assembly
- Use
- End of life

**Green SoCs for the IoT [Bol, FTFC, 2013]**

- Batteries
- Off-chip
- PCB
- PV cell
- 0.13-0.18μm CMOS
- 65/40 nm

**Bottom-up modeling of the Internet energy [Baudoin, TFE, 2013]**

<table>
<thead>
<tr>
<th>Section</th>
<th>Utilisation [J/MB]</th>
<th>TCAM</th>
<th>Production et Fin de vie</th>
<th>Améliorations Court terme</th>
<th>Améliorations Long terme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centres de données</td>
<td>126.1</td>
<td>-12%</td>
<td>11%</td>
<td>+++</td>
<td>+</td>
</tr>
<tr>
<td>Réseau central</td>
<td>4.6</td>
<td>-10%</td>
<td>5%</td>
<td>+</td>
<td>++</td>
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<tr>
<td>Accès fix</td>
<td>80.4</td>
<td>-10%</td>
<td>7%</td>
<td>+</td>
<td>+++</td>
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<tr>
<td>Accès Wi-Fi</td>
<td>140</td>
<td>-10%</td>
<td>7%</td>
<td>+</td>
<td>++</td>
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<tr>
<td>Accès mobile</td>
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<td>-13%</td>
<td>11%</td>
<td>++</td>
<td>+</td>
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<td>Smartphone</td>
<td>3</td>
<td>/</td>
<td>233%</td>
<td>/</td>
<td>/</td>
</tr>
<tr>
<td>Ordinateur portable</td>
<td>15</td>
<td>/</td>
<td>233%</td>
<td>/</td>
<td>/</td>
</tr>
<tr>
<td>Ordinateur fixe</td>
<td>70</td>
<td>/</td>
<td>100%</td>
<td>/</td>
<td>/</td>
</tr>
</tbody>
</table>

**Reconfigurable HW against technical obsolescence [de Streel, FTFC, 2012]**

- Delay
- Sense Buffer
- LUT
- Driver
- Multiplexer
- LILP ICs + energy harvesting
- Cubic-millimeter 3-D SIP
- Heterogeneous SOC in nano-CMOS technology
Energy-harvesting interface and power management

**Management unit for indoor/outdoor PV harvesting** [Bol, ESSCIRC, 2015]

**Rectifiers for RF energy harvesting** [Haddad, S3S, 2014]

**PV/TEG ambient energy manager** [e-peas, 2015]

**Voltage regulator LDO with 0.3nA quiescent current** [de Streel, FTFC, 2014]
Ultra-low-power SoC design

Robust ultra-low voltage logic design
[\textit{Bol, TVLSI, 2009}][\textit{Bol, JLPEA, 2011}]

Ultra-low leakage memory design
[Haine, FTFC, 2014]

Adaptive voltage scaling system
[\textit{De Vos, JOLPE, 2013}]

Ultra-low-voltage microcontroller sub-systems
[\textit{Bol, ISSCC, 2012}]
RECENT CHIP EXAMPLES –

*Green SoCs for a sustainable IoT*
SleepWalker microcontroller SoC for low-carbon WSNs

- Low system CO$_2$ footprint
  - low die area
  - few off-chip components
- Energy-harvesting operation
  - low active energy
  - adaptive voltage scaling 0.32-0.48V
- Compatibility with commercial components
  - MSP430 instruction set, same memory capacity and peripherals
  - 25MHz speed robust under industrial conditions

<table>
<thead>
<tr>
<th>MSP430</th>
<th>This work [Bol, ISSCC, 2012]</th>
<th>MIT (best research) [Kwong, ISSCC, 2008]</th>
<th>TI (best commercial) [Zwerg, ISSCC, 2011]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed [MHz]</td>
<td>25 @0.4V</td>
<td>0.3 @0.5V</td>
<td>24 @1.5V</td>
</tr>
<tr>
<td>Energy [µW/MHz]</td>
<td>7</td>
<td>27.3</td>
<td>164</td>
</tr>
<tr>
<td>CO$_2$ footprint [kg/1000 units]</td>
<td>14</td>
<td>47</td>
<td>83</td>
</tr>
</tbody>
</table>
3-mm² solar-powered video analysis SoC

**SunPixer 65nm SoC**

- Micro solar cells
- Supercapacitor
- 50MHz / 0.37V SIMD microcontroller

**Compression, calibration, image enhancement**

- Inductor-less harvesting power management unit
- 0.5V CMOS image sensor

**Power**

- External radio

**Energy**

- Pictures, video, features, events

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[F. Botman et al, IEEE ISCAS, 2014]
[D. Bol et al, ESSCIRC, 2015]
[D. Bol et al, Symp. VLSI, 2014]
Potential collaborations

EXAMPLES OF PROPOSED NEW R&D ACTIVITIES
• 20/14 nm process technology assessment:
  – Basic blocks to extract process parameters (noise, variability, ...) and to construct models
  – New design/verification methodologies for analog/mixed-signal

• Internet-of-Things:
  – New concepts of energy harvesting
  – Security aspects

• Communications:
  – New generation of low-power high-speed I/Os (wired / optical)
  – UWB wireless link and positioning
  – Wideband spectrum sensing
  – Wideband RF transceivers for software-defined/reconfigurable radios

• Integration (few mm³):
  – Heterogeneous integration, 3-D stacking, on-chip stress sensors
  – New materials: carbon nanotubes, graphene, biopolymers...
Others R&D activities beside ECS research

• Technical competences and skills base
• Take up of new technologies
• Behavioral modeling of mixed-signal systems
• EDA tools
• Test & validation tools
• Proof-of-concept structures
Conclusions

- Cutting-edge research @ UCL-ECS from process to circuits to systems
- Tens of working silicon chips from building IP blocks to full SoCs over the last years in 1µm, 0.13µm, 65nm CMOS (first 28nm tape-outs in 2015)
- Strong added value @ system/application levels when off-the-shelf components limit the specs
- Open to new projects and system drivers