Ultra-Low-Power Logic Style for Low-Frequency High-Temperature Applications

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1. Abstract
For ultra-low-power applications as sensor networks, digital integrated circuits may operate at low frequency to reduce dynamic power consumption [1]. At high temperature, the power consumption of such circuits can be dominated by static power dissipation due to leakage current. To avoid prohibitive static power dissipation, designers of high-temperature circuits use very-high-$V_T$ devices on micron-scale SOI technologies [2]. In this contribution, we propose a new logic style, namely Ultra-Low-Power (ULP) logic style, to benefit from the small area and low dynamic power of SOI deep-submicron technologies while keeping ultra-low leakage. In 0.13-µm PD-SOI technology, the static power consumption in active mode is reduced by nearly 3 orders of magnitude at the expense of increased delay.

2. ULP logic style
The structure of ULP logic gates is presented in Fig. 1 [3]. It is based on the equivalent standard CMOS gate with addition of 2 extra devices to gate subthreshold leakage, whose gates are connected to the output node. The header is an NMOS device and the footer is a PMOS device. The connection of the output node to the gate of the header and footer devices acts as a feedback loop by cutting off more the leakage current of the header or the footer device, depending on the output logic level. As shown in Fig. 1 for the ULP inverter, SOI implementation leads to compact layout as the footer (resp. header) can be abutted to the pull-down NMOS (resp. pull-up PMOS).

3. Leakage reduction mechanism
Let us consider $I_{OFF}$ current of the pull-down network (with PMOS footer device included) from the ULP inverter when input voltage is low, as presented in Fig. 2. The leakage reduction mechanism is based on the self-biased negative $V_{GS}$ of the NMOS and PMOS devices inside the pull-down network. $V_{GS}$ values depend on $V_A$ voltage of the internal node A. If devices are symmetrical, $V_A$ is close to $V_{DD}/2$. Devices thus operate with $V_{GS}$ close to $-V_{DD}/2$, leading to ultra-low leakage. Fig. 2 shows measured $I_{OFF,ULP}$ from ULP pull-down network in standard 0.13-µm PD-SOI technology at room and at high temperatures. When $V_{DD}$ increases, the subthreshold current first increases because $V_{DS}$ of the NMOS and PMOS devices increase too. Then, it strongly decreases as $V_{GS}$ of the devices becomes more and more negative. At room temperature, GIDL and gate leakage currents limit the achievable leakage when $V_{DD}$ is higher than 0.7V [4]. At room temperature, $I_{OFF,ULP}$ is reduced by more than 4 orders of magnitude as compared to $I_{OFF,NMOS}$ of standard NMOS device ($V_{DD}$=1V). At high temperature, this reduction of $I_{OFF}$ remains larger than 3 orders of magnitude.
4. DC behaviour

In order to assess the correct operation and the robustness of the ULP logic style, let us examine the DC characteristic of the ULP inverter depicted in Fig. 3. Simulation of the voltage transfer curve at 200°C is also presented in Fig. 3. The output levels are close to 0 and VDD. When VIN=0V, VO of P1 is highly negative and P1 represents a small equivalent impedance. N2 has thus VO=0 and the ION pull-up current is the subthreshold current of N2. This ION current is nearly 3 orders of magnitude higher than IOFF of pull-down network, as shown in Fig. 1. Similar reasoning can be applied to the case VIN=VDD. This leads to very good output logic levels. Moreover, as ION is only subthreshold current, the slope of the voltage transfer curve from the inverter is very steep, making the design very robust. The drawback is that the delay of the inverter will be high because ION is a subthreshold current. This is mitigated by the use of low-VT devices and the high temperature operation.

The curve from Fig. 3 shows hysteresis, the inverter switching voltage is different when the input is rising or falling. This is due to the feedback loop made of the connection of the output node to the header/footer gates [3]. This provides a very high static Noise Margin (NM) for the inverter: NM(S)=0.79V and NM(IS)=0.82V for VDD=1V, which are never achieved with standard CMOS logic style. This unique feature is highly valuable to build robust ultra-low-power SRAM cells.

![Fig.3: Simulated voltage transfer curve of ULP inverter (W/LN1=P1=0.15/0.13[µm] and W/LN2=0.30/0.13 [µm], VDD=1V, T=200°C)](image)

5. Performance comparison

In order to assess the efficiency of ULP logic style, performances are compared with standard CMOS logic style at gate level through simulation of an inverter with fan-out of 4. For ultra-low-power applications, delay of the gates is not of uttermost interest. The circuit only has to support low operating frequency in the kHz range. Therefore, we consider the following figures of merit: static current and total power consumption at low operating frequencies (i.e. 1 and 100 kHz), rather than power-delay or energy-delay products. The delay is given for information purpose.

The considered technology is a dual-VT technology. Low-VT devices (VT,N=0.34V, VT,P=-0.33V) are used for ULP logic style to increase drivability of pull-up/down networks and high-VT devices (VT,N=0.43, VT,P=-0.42V) are used for standard CMOS logic style to lower static current. Simulation results are summarized in Table 1.

At 1V, ULP inverter provides a static current reduction of nearly 3 orders of magnitude as compared to standard high-VT CMOS inverter. It leads to very low total power consumption in the pW-range at the expense of longer delay. Notice that the 34-ns delay for FO4 inverter is sufficient to operate circuits at low frequencies such as 100 kHz. The power consumption of high-VT CMOS inverter at 100 kHz is in the nW-range, being dominated by static current. As shown in Table 1, lowering the power supply voltage of high-VT CMOS logic leads to lower power but it remains in the nW-range.

### Table I. Performance comparison of inverters at 200°C

<table>
<thead>
<tr>
<th>Type</th>
<th>VDD</th>
<th>Istat</th>
<th>Delay @ 1 kHz</th>
<th>Power @ 1 kHz</th>
<th>Power @ 100 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULP</td>
<td>1</td>
<td>31 pA</td>
<td>34</td>
<td>32 nW</td>
<td>154 nW</td>
</tr>
<tr>
<td>High VT</td>
<td>1</td>
<td>27 nA</td>
<td>0.01</td>
<td>27 nW</td>
<td>30 nW</td>
</tr>
<tr>
<td>High VT</td>
<td>0.5</td>
<td>13 nA</td>
<td>0.37</td>
<td>6.8 nW</td>
<td>7.7 nW</td>
</tr>
</tbody>
</table>

6. Conclusions

We proposed an ULP logic style to benefit from small area and small dynamic power of deep-submicron technologies while keeping ultra-low-leakage at high temperature. ULP logic style is shown to be very robust and to reduce power consumption at low frequency by nearly 3 orders of magnitude. In order for the standard CMOS inverter to achieve the same static current as the ULP inverter, SPICE simulations show that VT of the devices from the CMOS inverter should be raised by 0.35V. This would lead to a threshold voltage of nearly 0.8V. Such a value is no longer proposed by chip manufacturers in very deep-submicron technologies. ULP logic style is thus a unique technique to design ultra-low-power digital circuits for high-temperature applications, i.e. with neither extra mask nor extra process cost.

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References