Channel Length Upsize for Robust and Compact Subthreshold SRAM

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***Abstract*—Subthreshold operation is an efficient way to achieve ultra-low-power consumption. However, subthreshold SRAM requires special design techniques to ensure sufficient robustness in the context of high process variability of nanoscale technologies. In this contribution, we propose to increase MOSFET channel length in the conventional 6T SRAM cell to operate safely at subthreshold V_{dd}. Two length upsizing schemes are proposed and we show that they lead to an efficient robustness increase with minimum area overhead (10%), thanks to DIBL and variability mitigation. We also show that the improved subthreshold swing yields a static power reduction by a factor 20 without significant speed deterioration.**

I. Introduction

Over the last decade, ultra-low-power design has become a vibrant research field for applications such as sensor networks, RFID tags and biomedical devices. Subthreshold operation is an efficient technique to achieve ultra-low power consumption for circuit with very loose timing constraint [1]. The principle is simple: lowering the power supply V_{dd} to extremely low voltages, below the threshold voltage V_t, leading to quadratic reduction of the dynamic power consumption.

Whereas subthreshold logic design is straightforward in principle thanks to the intrinsic robustness of CMOS logic style, serious stability issues are raised in subthreshold SRAM design by the inherent ratioed behavior of SRAM cells. Indeed, at low V_{dd}, read/hold stability and write ability are severely degraded because of reduced I_{on}/I_{off} ratio and magnified current variability due to the exponential dependence of subthreshold current on V_t [2]. The design target is thus to achieve safe operation at low V_{dd} values, compatible with subthreshold logic.

Because of this exponential current variability in subthreshold regime, read-stability and write-ability issues cannot be solved by tuning the device width, i.e. modifying the SRAM cell (β) and pull-up ratios, as it would lead to unacceptable device widths [2]. In previous articles on subthreshold SRAM, write-ability issues have been dealt by:

- unconventional biasing schemes: V_{dd} collapse or WL boost during a write operation [3], [4],
- device addition to the conventional 6T SRAM cell to break/weaken the feedback loop when writing the data [5], [6].

Read stability was ensured by decoupling the read BL from the cell memory nodes, through read buffer insertion [3]- [5], [7], [8]. Although very efficient, this technique requires the addition of 2 to 4 devices to the 6T SRAM cell with an important area overhead.

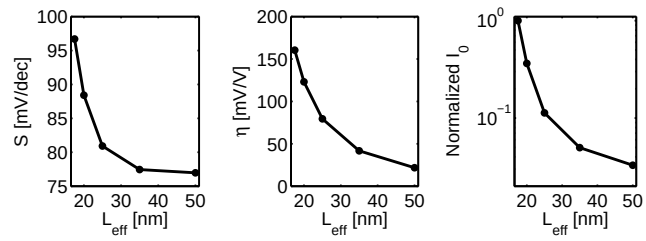

Fig. 1. Evolution of subthreshold parameters with increasing channel length for 45-nm technology (nominal L_{eff}=17.5nm)

In this contribution, for compactness issues, we focus on increasing robustness of the 6T SRAM cell without architectural modification nor device addition. Therefore, we propose to increase the channel length to solve read stability issues in two ways:

1) improvement of MOSFET subthreshold operation and variability mitigation [9] through uniform channel length upsize,
2) exponential cell (β) ratio increase by short-channel effects and variability mitigation.

This contribution is organized as follows. In Section II, we briefly examine the operation of MOSFET in subthreshold regime. In Section III, the issues in subthreshold SRAM design are presented with both channel length upsizing schemes. Finally, performances in 45nm technology are compared with resimulated versions of previously-proposed subthreshold SRAM cells in Section IV.

II. Subthreshold MOSFET operation

In subthreshold regime, drain current can be expressed as:

$$I_{sub} = I_0 \times 10^{\frac{V_{gs}+\eta\, V_{ds}}{S}} \times \left(1 - e^{\frac{-V_{ds}}{U_{th}}}\right) \qquad (1)$$

where I_0 is a reference current proportional to W/L_{eff}, which depends exponentially on V_t. S is the subthreshold swing, η the DIBL coefficient and U_{th} the thermal voltage close to 26 mV at ambient temperature. At a given temperature, I_{sub} depends only on three parameters: I_0, S and η. In this contribution, we consider a 45nm technology (nominal V_{dd}=1V, T_{ox}=1.1nm, L_{eff}=17.5nm and $V_{t,sat}$=0.37V) based on predictive technology model[1] from Arizona State University [10].

[1]Models available on-line at http://www.eas.asu.edu/ptm.

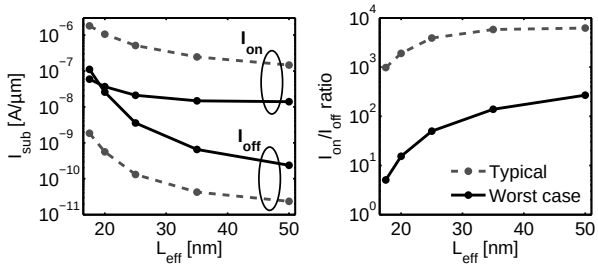

Fig. 2. Evolution of subthreshold current (left) and I_{on}/I_{off} ratio (right) with increasing channel length (W=68nm, V_{dd}=0.3V, worst case is 3σ). I_{on}/I_{off} ratio is computed between two adjacent devices (independent V_t but same L variables because of strong spatial correlation).

Spice simulation of this model gives the following values for the subthreshold parameters: I_0=0.59nA/μm, S=97mV/dec and η=160mV/V.

In the considered 45-nm technology, nominal effective channel length L_{eff} is 17.5nm. Increasing L_{eff} by several nanometers is easily achieved at layout level by increasing the drawn gate length by the equivalent quantity. The evolution of these parameters with increasing channel length is shown in Fig. 1 from Spice simulation. All parameters exhibit a negative exponential dependence on L_{eff}. Subthreshold swing tends toward long-channel value of $ln(10)\,U_{th}\,\left(1+\frac{C_{dep}}{C_{ox}}\right)$, where C_{dep} is the depletion capacitance in the channel. DIBL factor tends toward 0 and reference current I_0 decreases because of V_t roll-off short-channel effect.

In nanoscale technologies, process variability cannot be overlooked especially when focusing on subthreshold design, as variability of the circuit performances is magnified by the exponential dependence of I_{sub} on V_t [11]. Throughout all this contribution, variability is taken into account by carrying out Monte-Carlo simulations with two sources of variability. First, random doping fluctuation is considered by modeling V_t of each device as an independent normally-distributed variable with variance given by [12]:

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{W\,L_{eff}}} = 3.19\times10^{-8}\,\frac{T_{ox}N_{ch}^{0.4}}{\sqrt{W\,L_{eff}}}. \qquad (2)$$

This results in a σ_{Vt} of 44mV for minimum-sized devices. Second, variability of critical dimensions is considered through L_g variability. We model L_g variations as a normal distribution with $3\sigma/\mu$ equal to 20%. As L_g variations have a strong spatial correlation [13] and a single SRAM cell is very small, we consider a single normally-distributed L_g variable for all the devices of the cell. From 1k Monte-Carlo Spice simulations under 0.3V V_{dd}, the 3σ worst-case I_{on} is 30 times lower than typical I_{on} and the 3σ worst-case I_{off} is 60 times higher than typical I_{off}, with nominal channel length. Variability can be mitigated by length upsize, as random doping fluctuation depends on channel area according to Eq. (2) and as gate length variations are relatively smaller when the channel is long. Fig 2 shows that variability is efficiently reduced by length upsize. Combined with subthreshold swing reduction, it results in improved I_{on}/I_{off} ratio between adjacent devices.

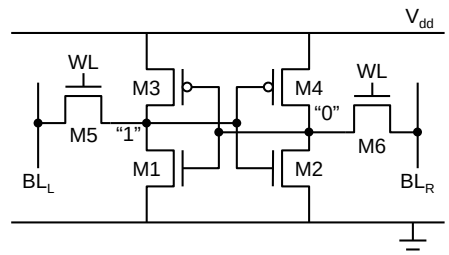

Fig. 3. Conventional 6T SRAM cell

In 45-nm technology, subthreshold swing, DIBL effect and current variability are very high due to short-channel effects. Channel length upsize improves subthreshold operation thanks to mitigation of these effects.

III. Robust and compact subthreshold SRAM design

In this section, we analyze the failure mechanisms of 6T SRAM cell operating in subthreshold regime. We then propose to upsize device length to efficiently increase read stability with minimum area overhead. The goal is to operate safely at a target 0.4V subthreshold V_{dd}.

A. Failure mechanisms

Robustness of the conventional 6T SRAM cell shown in Fig. 3 depends on 3 criterion:

1) Hold stability: measured by the hold SNM, computed when writing in an adjacent cell data different from the memorized ones, i.e. BL_L is assigned to "0" and BL_R to "1".

2) Read stability: measured by the read SNM, computed in precharge phase, i.e. with both BL clamped to V_{dd}.

3) Write ability: measured by the write margin (SNM during a write operation), computed by assigning BL_L to "0" and BL_R to "1".

Hold SNM and read SNM have to be positive while write margin has to be negative in order to ensure proper operation.

Evolution of the robustness criterion with V_{dd} is shown in Fig. 4 for the considered 45-nm technology. Notice that we choose the 4σ tail (99.997% confidence interval) instead of the traditional 6σ because ultra-low-power applications such as microsensor nodes, RFID tags or biomedical devices only require small SRAM arrays of several kilobytes and can rely on redudancy [4].

Some observations can be made from Fig. 4:

- robustness is severely degraded when lowering V_{dd};
- robustness is deteriorated by process variability;
- degraded subthreshold swing has little impact on robustness;
- DIBL considerably affects hold and read SNM while there is little effect on write margin.

The first two observations are straightforward. The impact of subthreshold swing is small as confirmed in [15]. Margins are computed when the cell actually flips and at that moment, the input voltage of the cross-coupled inverters are close to $V_{dd}/2$, making the V_{gs} of their devices equal. As a degradation

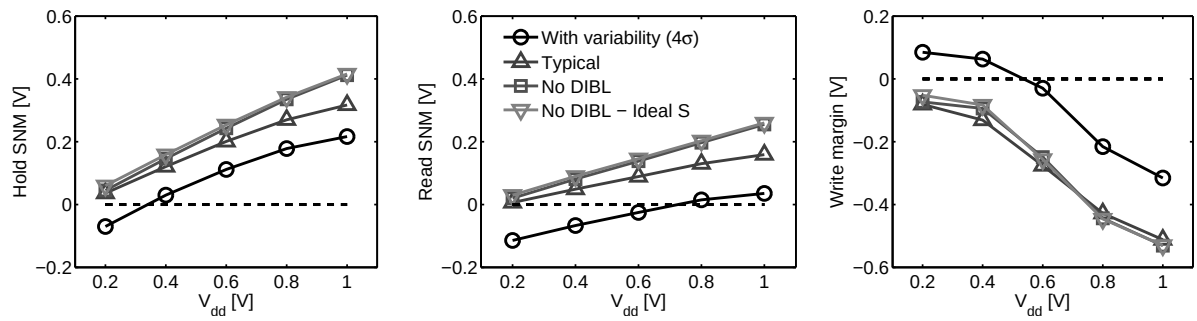

Fig. 4. Robustness criterion of conventional 6T SRAM cell vs. V_{dd}: hold SNM (left), read SNM (center) and write margin (right) (45-nm technology, cell ratio is 2, pull-up ratio is 1). DIBL effect and process variability affect robustness of the cell.

of the subthreshold swing reduces I_{on}/I_{off} ratio but does not influence the current between devices having same V_{gs}, the subthreshold swing value has small impact on voltage margins. A more complete robustness characterization would be achieved by investigating both voltage and current margins, as suggested in [16] with the N-curve computation. However, this is beyond the scope of this brief contribution.

To the authors' knowledge, the impact of DIBL on SRAM cell stability has never been considered up to now. Let us get an intuitive insight of this point. Hold/read stability depends on a ratioed behavior: ON cell devices ($M2$ and $M3$ in Fig. 3) have to keep the data at internal nodes while access devices ($M5$ and $M6$) drive some current from these nodes to the bitlines. This current from access devices is an ON current when in read operation, and an OFF current when in hold operation. In both cases, access devices $M5$ and $M6$ have a large V_{ds} close to V_{dd}, which lowers their V_t through DIBL effect as compared to ON cell devices $M2$ and $M3$ that keep internal nodes close to their ideal values and thus have a very small V_{ds}. DIBL effect thus implies a systematic V_t mismatch between ON cell devices and access devices, thereby lowering the SNM. In a write operation, things are different: a correct write operation depends on the ability of $M5$ access device that has to write a "0" to win the fight against $M3$ PMOS ON cell device keeping a "1". In this fight, access device has a V_{ds} close to V_{dd}, whereas PMOS ON cell device has a small V_{ds}. The DIBL-induced V_t mismatch is thus no longer detrimental and write ability is not clearly affected by DIBL effect.

From Fig. 4, read stability limits V_{dd} lowering for the considered technology, because read SNM is the first criterion to fail at 0.72V. As read SNM is strongly influenced by process variability and DIBL, limiting these effects is important in order to operate at subthreshold V_{dd}. That can be achieved through channel length upsize as explained in Section II. In next sections, we introduce two length upsizing schemes to improve read stability. We neglect hold stability as it remains better than read stability. Write margin issues are dealt by WL voltage boosting, as discussed in Section IV.

B. Uniform channel length upsize of all devices

Upsizing uniformly the channel length of all devices inside an SRAM cell was introduced in [15] for limiting variability. Moreover, we showed in Section II that it also reduces DIBL

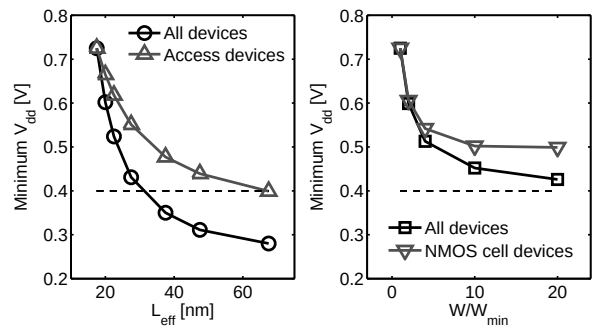

Fig. 5. Simulated minimum V_{dd} to ensure 4σ read stability of 6T SRAM cell when increasing the channel length (left) or the channel width (right).

effect, which would thereby further increase robustness of 6T SRAM cell at subthreshold V_{dd} as shown in Section III-A. Fig. 5 (left) shows the improvement brought by uniform length upsize in terms of minimum V_{dd} to ensure read stability (positive SNM). In order to meet the target 0.4V subthreshold V_{dd}, all channel lengths have to be upsized by only 13nm. As a comparison, minimum V_{dd} when upsizing the width of all the devices is shown in Fig. 5 (right). In this case, variability mitigation leads to a reduction of minimum V_{dd} but the width has to be upsized to unacceptable values in order to operate at 0.4V.

C. Cell-ratio channel length upsize of access devices

The other possibility to improve read stability is to increase the cell (β) ratio, i.e. the ratio between W/L of NMOS cell devices ($M1$-$M2$) and access devices ($M5$-$M6$). This is traditionally achieved by increasing the width of the cell NMOS devices. However, as shown in Fig. 5 (right), this is not feasible in subthreshold regime as it would lead to unacceptable width in order to compensate exponential current variability. We rather propose to tune cell ratio by increasing the length of the access devices[2]. Fig. 5 (left) shows that it yields an efficient reduction of minimum V_{dd}, thanks to DIBL mitigation and V_t roll off, which leads to a highly decreased

[2]Notice that in [8], a length upsize of the access devices has been proposed in the opposite way to improve write margin thanks to reverse short-channel effect: an I_0 increase when upsizing the length. Indeed, depending on the considered devices (peak doping/halo implants), a channel length upsize could have a different impact on I_0 whether forward or reverse short-channel effect dominates. However, the impact on S and DIBL effect remains the same.

TABLE I
COMPARISON OF SRAM CELL PERFORMANCES IN 45NM TECHNOLOGY

Cell type	Channel length upsizing scheme	V_{dd} [V]	Area overhead	Min. WL boost voltage [mV]	4σ worst-case I_{read} [nA]	P_{stat} [pW]	Max. # cells per BL
6T	/	1.0	/	0	$3.5\ 10^4$	$2.3\ 10^4$	570
6T	uniform (+13nm)	0.4	9.5%*	66	23.8	26	190
6T	cell-ratio (+50nm)	0.4	7%*	132	13.0	370	210
8T [7]	/	0.4	29% [7]	59	24.8	850	$5^\dagger$
10T [8]	/	0.4	60% (estimated)	$59^\ddagger$	18.0	800	∞

* Evaluated with 45nm high-density SRAM design rules from [17].
† Can be solved by peripheral assist (rising buffer foot voltage to V_{dd}) [4].
‡ Solved in [8] by reverse short-channel effect (see footnote 2).

subthreshold current of access devices, as we reported in Fig. 2. A channel length upsize of 50nm is required to ensure read stability at target 0.4V V_{dd}.

IV. PERFORMANCE COMPARISON

Let us now examine main performances of SRAM cell obtained with both channel length upsizing schemes (uniform upsize of all devices and cell-ratio upsize of only access devices). Performances are compared in Table I with resimulated version in the same 45nm technology of previously-reported 8T and 10T subthreshold SRAM cells relying on read buffer insertion to improve read stability. For comparison purpose, performances of minimum-sized conventional 6T cell are presented under 1V V_{dd} as this cell fails to operate at 0.4V.

First, the area overhead of the proposed upsizing schemes is very low (less than 10%), leading to compact SRAM design. Then the minimum WL boost voltage to achieve 4σ write ability at 0.4V when uspizing uniformly the channel length of all devices is comparable with 8T and 10T cells. The main drawback is that read and write WL are not decoupled in the 6T versions and they have to be driven at different voltages depending on the operation (read or write). Minimum WL boost voltage in cell-ratio upsizing scheme is somewhat higher due to weakened access devices.

Worst-case read current determines the speed of read operation. It is better for the uniform than for cell-ratio upzising schemes and comparable with 8T cell. Mean static power dissipation with uniform length upsize is drastically reduced without significative speed penalty, thanks to improved subthreshold swing. Finally, the maximum number of cells per BL that enables to differentiate a low data read from leakage of unaccessed cells is presented too. This is computed by specifying that worst-case read current has to remain $10\times$ higher than the BL leakage of all unaccessed cells [14]. The maximum number of cells per BL for the proposed upsizing schemes remains good even in subthreshold regime, whereas the 8T cell requires either peripheral assist or addition of 2 extra devices (10T cell from Table I) [14].

V. CONCLUSION

Channel length upsize improves subthreshold MOSFET operation and mitigates variability. We show that upsizing the MOSFET channel length in the conventional 6T SRAM cell increases read stability in subthreshold regime with small area overhead. Moreover, uniform length increase of all the devices greatly reduces static power dissipation thanks to improved subthreshold swing.

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