Pushing Ultra-Low-Power Digital Circuits into the Era

David Bol

Ph.D public defense

December 16, 2008
Pushing Ultra-Low-Power Digital Circuits into the Era

David Bol

Ph.D public defense

December 16, 2008
Why ultra-low power?

High-performance circuits
Performances: 10 GOp/s
Power < 100 W

Low-power circuits
Performances: 1 GOp/s
Power < 1 W
Hearing aids
ULP digital circuits

RFID tags

Hearing aids and biomedical

Ultra-low-power circuits
Performances: 10 k - 10 MOp/s
Power < 1µW

Wearable electronics

Sensor networks

Smart Dust [Berkeley]
Pushing Ultra-Low-Power Digital Circuits into the \textit{Nanometer} Era

\textit{David Bol}

Ph.D public defense

December 16, 2008
Moore’s law (1965)

Every 18 months: \( x \times 2 \)

[Graphics showing transistor counts over time, with labels like '1965 Actual Data', '1975 Projection', 'Memory', 'Microprocessor', and Intel processor generations like '4004', '8080', '80286', 'i386', 'Pentium', 'Pentium II', 'Pentium III', 'Pentium IV', 'Itanium', and '4G'.]
Moore’s law today

Gordon Moore estimated in 2003 that the number of transistors shipped in a year had reached about 10,000,000,000,000,000,000,000 (10^17). That’s about 100 times the number of ants estimated to be in the world.

Copyright © 2006 Intel Corporation. All rights reserved.

The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

Copyright © 2006 Intel Corporation. All rights reserved.
Moore’s law

Moore’s law without technology scaling

Moore’s law with technology scaling
Technology scaling

Clock frequency

Transistor count

1 MHz

10 MHz

100 MHz
Technology scaling

Clock frequency
- 1 MHz
- 10 MHz
- 100 MHz
- 1 GHz

Transistor count
- 10
- 4
- 5
- 6
- 7
- 8
- 9

ULP circuits

2008
45nm

D. Bol
Trend in ULP digital circuits

Last chips [IEEE ISSCC’08]:

- Ultra-low-power 0.3V µC for biomedical applications [Kwong]
- Ultra-low-power 0.32V motion estimator [Kaul]
Outline

- Motivation
- **Basics: energy consumption of ULP digital circuits**
- Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
Sources of power dissipation
Sources of power dissipation

\[ V_{dd} \]

\[ 1/f_{clk} \]

IN

\[ \text{‘1’} \]

OUT

\[ \text{‘0’} \]

\[ I_{on} \]

\[ C_L \]
Sources of power dissipation

\[ P_{\text{dyn}} \sim f_{\text{clk}} \times C_L \times V_{dd}^2 \]
Sources of power dissipation

$P_{\text{dyn}} \sim f_{\text{clk}} \times C_L \times V_{\text{dd}}^2$
8-bit RCA multiplier in 130nm technology

ULP applications = subthreshold logic

Minimum $V_{dd}$ [V]

Power consumption

$P_{dyn} \sim f_{clk} \times C_L \times V_{dd}^2$

Functional limit

Pervasive

Subthreshold logic

ULP applications

Throughput [Op/s]
Sources of power dissipation

$I_{off} = I_{leak}$

$P_{stat} \sim V_{dd} \times I_{leak}$
Power consumption

8-bit RCA multiplier in 130nm technology

ULP applications
= subthreshold logic

Functional limit

Speed limit

ULP applications
= subthreshold logic

\[ P_{\text{dyn}} \sim f_{\text{clk}} \times C_L \times V_{\text{dd}}^2 \]

\[ P_{\text{stat}} = V_{\text{dd}} \times I_{\text{leak}} \]

Throughput [Op/s]

Minimum \( V_{\text{dd}} \) [V]

Power [W]

D. Bol
Energy consumption

8-bit RCA multiplier in 130nm technology

ULP applications = subthreshold logic

Minimum $V_{dd}$ [V]

Throughput [Op/s]

Energy per operation [J]

$E_{dyn} \sim C_L V_{dd}^2$

$E_{min}$

$E_{stat}$

$E_{	ext{ulp}}$ applications

Frequency/voltage scaling

D. Bol
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
  - Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
Impact of technology scaling

\[ T_{\text{ox}}, L, W \sim \frac{1}{S} \]
Impact of technology scaling

- $I_{on}$
- $C_L$
- $I_{leak}$

$E_{stat} \sim I_{leak} V_{dd}^2$

- Speed
- Reduce $V_{dd}$

$E_{dyn} \sim C_L V_{dd}^2$

Variability!
Variability

130nm technology

Gate

Source

Drain

Continuous doping

Gate

Source

Drain

45nm technology

Gate

Source

Drain

Straight line edges

Rough line edges

Discrete dopants

Gate

Source

Drain

Gate

Source

Drain

D. Bol
Impact of technology scaling

8-bit RCA multiplier

Throughput [Op/s]

Energy per operation [J]

Minimum $V_{dd}$ [V]

Functional limit

Speed limit

Variability

$E_{dyn}$

130nm

45nm

D. Bol
Impact of technology scaling

8-bit RCA multiplier

Minimum $V_{dd}$ [V]

Throughput [Op/s]

Energy per operation [J]

-14
-13
-12
-11
-10

10
-10
10
-9
10
-8
10
-7
10
-6
10
-5
10
-4
10
0.5
1
1.5

130nm
45nm

Speed limit

Functional limit

ULP applications

$E_{dyn}$

$E_{stat}$

$130nm$

$45nm$
Impact of technology scaling

Energy per operation vs Throughput

ULP applications

Energy per operation x10 !

130nm

45nm

1

2
What if you have to scale?

Scale, scale, scale...

Famous Intel co-founder
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
Technology versatility

- **High-Performance/General-Purpose**
  - Short $L_g$
  - Thin $T_{ox}$
  - Low $V_t$
  - Mid $V_{dd}$
  - **High $I_{on}$**
  - **High $I_{leak}$**

- **Low-Power**
  - Mid $L_g$
  - Mid $T_{ox}$
  - High $V_t$
  - High $V_{dd}$
  - **Low $I_{on}$**
  - **Low $I_{leak}$**
Technology selection

8-bit RCA multiplier in 45 nm technology

Minimum $V_{dd}$ [V]

Throughput [Op/s]

Energy per operation [J]

High-$V_t$ LP

High-$V_t$ GP

Low-Power

General-Purpose

ULP applications

D. Bol
Dual-$V_t$ assignment

Register

Std-$V_t$

Non-critical path

Non-critical path

clk

clk
**Dual-\(V_t\) assignment**

![Diagram showing Dual-\(V_t\) assignment with two paths: Std-\(V_t\) and High-\(V_t\). Each path contains non-critical paths with inverters and registers. The clock signal (clk) triggers the registers.]
Dual-\(V_t\) assignment

Critical path

Std-\(V_t\)

OUT

High-\(V_t\)

IN

OUT

Maximum \(N\)

Typical

With variability

2 3

19

11

7 8

32

27

Inefficient

\(V_{dd} [V]\)

\(N\)
Circuit adaptation

- Global process variations
- Temperature variations
- Modeling errors
- Device aging

Energy per operation vs target throughput
Circuit adaptation

Energy per operation vs. throughput with a target throughput. The graph shows the comparison between the actual and model energy per operation curves, indicating an adaptation point for optimal performance.
Circuit adaptation

8-bit benchmark multiplier in 45 nm LP technology

Norm. throughput

Norm. energy per op.

V_{dd} [V]

V_{BB} [V]

ASV (V_{BB} = 0V)

ABB (V_{dd} = 0.35V)
Circuit adaptation

8-bit benchmark multiplier in 45 nm LP technology

Minimum $V_{dd}$ [V]

- ASV ($V_{BB}=0V$)
- ABB ($V_{dd}=0.35V$)

Norm. throughput

AXI better

Norm. energy per op.

- ABB better
- ASV better

D. Bol
Circuit adaptation

Reverse body bias is fine in 45 nm LP technology

Problem in 45 nm GP! What at 32 nm?
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
$E_{\text{min}}$ modeling

[Hanson, IEEE TED, pp. 175-185, 2008]
Evolution of $E_{\text{min}}$

New effects in nanometer technologies

In all flavors

$E_{\text{min}}$ [fJ]

130nm  90nm  65nm  45nm

$C_L S^2$
New effects in nanometer technologies

New effects:

- Bad short-channel $S$
- Drain-induced barrier lowering
- Gate leakage
- Variability

\[
E_{\text{min}} \text{ [fJ]}
\]

\[
C_L S^2
\]
New effects in nanometer technologies

New effects:

- Bad short-channel S
- Drain-induced barrier lowering
- Gate leakage
- Variability

\[ E_{\text{min}} \text{ [fJ]} \]

\[ C_L S^2 \]

\[ \text{Var.} \]

\[ I_{\text{gate}} \]

\[ \text{DIBL} \]

\[ S_{\text{short}} \]

\[ S_{\text{long}} \]

Low \( V_t \) + long \( L_g \)
FULLY-DEPLETED SOI TECHNOLOGY

- Low $C_j$, Low variability
- Low $S$, mid DIBL
- Buried oxide

**Undoped Channel**

**Bar Graph**

- $E_{\text{min}}$ vs. technology node
- $C_LS^2$ contribution

**Diagram**

- Source to Drain
- Gate
- Low $C_j$, Low variability
- Buried oxide
- Low $S$, mid DIBL
Evolution of $E_{\text{min}}$
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
High-temperature operation

130nm PD SOI technology

Leakage x 100

$I_{\text{leak}}$ [A/µm]

$V_{dd}$ [V]

- $25^\circ C$
- $200^\circ C$

$D$

$G$

$S$

$I_{\text{leak}}$

High-temperature operation

130nm PD SOI technology

Leakage x 100

$I_{\text{leak}}$ [A/µm]

$V_{dd}$ [V]

- $25^\circ C$
- $200^\circ C$
Low-leakage SOI technology

1 or 0.5 µm, 5 or 3.3V

- \( E_{\text{stat}} \sim I_{\text{leak}} \) 😊
- \( E_{\text{dyn}} \sim C_L V_{dd}^2 \) 😞
- Die area

33
Standard SOI technology

0.13 μm, 1 V
High-temperature operation

ULP transistor

130nm PD SOI technology

\( V_{gs} < 0 \)
ULP logic style

ULP logic style

Layout in SOI

Hysteresis
ULP logic style at 200°C:

- 1000x $P_{\text{stat}}$ reduction
- Long delay $\rightarrow$ max $\sim$ 1 MOp/s
Outline

- Motivation
- Basics: energy consumption of ULP digital circuits
- Impact of technology scaling
- Reaching $E_{\text{min}}$
- Reducing $E_{\text{min}}$
- ULP logic style for high-temperature applications
- Roadmap for nanometer ULP circuits
ITRS recommendations

Logic CMOS Device Categories

HP CMOS (High Performance)
- Highest Ion, Lowest CV/I
- High leakage
- Medium Vdd

LOP CMOS (Low Operation Power)
- Lowest Vdd
- Medium Ion, medium CV/I
- Medium leakage

LSTP CMOS (Low Standby Power)
- Lowest leakage
- Low Ion, high CV/I
- High Vdd

ULP

ITRS07
Reducing $E_{\text{min}}$

Technology level

Single device type for all logic gates

Low $C_L$, $S$, DIBL, variability ($I_0$)

$I_{\text{gate}}, I_{\text{junc}} < I_{\text{sub}}$ @ 0.3-0.4V

Relaxed constraints:

- $C_{g,sub}$
- $I_{\text{gate}}, I_{\text{junc}}$
- $R_{s,d,g}$
- Mobility

- Multi-$I_0$ devices with coarse granularity
- On-chip $I_0$ tuning with fine granularity

Reaching $E_{\text{min}}$

Circuit level

Active

$I_0$ tuning

- Design-time device selection
- Run-time adaptive technique

Sleep-mode technique

- High leakage reduction
- Low impact on active-mode operation
## Technology/circuit roadmap

<table>
<thead>
<tr>
<th>Applications</th>
<th>Node</th>
<th>130 / 90 nm</th>
<th>65 / 45 nm</th>
<th>32 / 22 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-temperature ULP</td>
<td>ULP logic</td>
<td>PD SOI</td>
<td>Reliability issues</td>
<td>Reliability issues</td>
</tr>
<tr>
<td>ULP industrial applications</td>
<td>style</td>
<td>• (FD SOI)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ GP flavor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard ULP applications</td>
<td>Subthreshold logic</td>
<td>Bulk (+ <em>adapt. RBB</em>)</td>
<td>Subthreshold logic</td>
<td>Subthreshold logic</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Bulk + <em>adapt. RBB</em></td>
<td>@ GP flavor</td>
<td>• FD SOI @ LP flavor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• (FD SOI)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ GP flavor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ULP mode in LP applications</td>
<td><strong>Performance issues</strong></td>
<td>Subthreshold logic</td>
<td>Subthreshold logic</td>
<td>Subthreshold logic</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Bulk opt. + <em>adapt. RBB</em></td>
<td>FD SOI</td>
<td>• FD SOI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• (FD SOI)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ GP flavor</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Architectural techniques (//, pipe) for meeting throughput constraint
Thank you!

Any questions?

Acknowledgements:
D. Bol’s work was funded by FNRS and Walloon region of Belgium.
Energy consumption

8-bit RCA multiplier in 0.13 µm technology

Energy per operation [J]

Energy consumption

Sub $V_t$ ← I

$E_{min}$

$E_{dyn} \sim C_L V_{dd}^2$

$E_{stat} = V_{dd} \times I_{leak} \times T_{del}$

$T_{del}$ increase