Digital SOI design in the nanometer era – From high-performance to ultra-low-power circuits

EuroSOI 2009 tutorial

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SOI for high-performance applications

Partially-depleted SOI technologies

IBM Cell Broadband Engine in 45nm SOI
[Takahashi, ISSCC’08]

IBM Cell Broadband Engine in 65nm SOI
[Pille, ISSCC’07]

Benefits of scaling:

- -34% area
- -100mV $V_{dd}$
- -40% power @ iso-speed
SOI for high-performance applications

- Typical claims of PD SOI for high-performance applications:
  - +15/30% speed @ iso-power
  - -20/40% power @ iso-speed
  - area reduction (floating-body devices)

- Drawbacks:
  - Self heating (because BOX = thermal insulator)
  - History effects (variable delay < floating body)

- PD SOI foundries and chips: IBM, AMD, Freescale, Sony/Toshiba
Why ultra-low power?

High-performance circuits
Performances: 10 GOp/s
Power < 100 W

Low-power circuits
Performances: 100M-1GOp/s
Power < 1 W
ULP digital circuits

Hearing aids and biomedical

RFID tags

Ultra-low-power circuits

Performances: 10 k - 10 MOp/s

Power < 1μW

Wearable electronics

Sensor networks

Ultra-low-power circuits

Smart Dust [Berkeley]
Technology versatility

45nm technology

General-Purpose
- Short $L_g$
- Thin $T_{ox}$
- Low $V_t$
- Mid $V_{dd}$

- High $I_{on}$
- High $I_{leak}$

Low-Power
- Mid $L_g$
- Mid $T_{ox}$
- High $V_t$
- High $V_{dd}$

- Low $I_{on}$
- Low $I_{leak}$

For ULP applications, play with $V_{dd}$
Ultra-low power/energy

Ultra-low-power

= subthreshold logic

8-bit RCA multiplier in 0.13 µm technology

Sub $V_t$ →

$E_{\text{min}}$

Energy per operation [J]

10^{-12} 10^{-13} 10^{-14} 10^{-15}

$E_{\text{dyn}} \sim C_L V_{dd}^2$

$E_{\text{stat}} = V_{dd} \times I_{\text{leak}} \times T_{\text{del}}$

$V_{dd}$ [V]

$T_{\text{del}}$ increase
Ultra-low power/energy

8-bit RCA multiplier in 0.13 µm technology

Energy per operation [J]

Sub $V_t$ ← $E_{\text{min}}$

$E_{\text{dyn}} \sim C_L V_{dd}^2$

$E_{\text{stat}}$

Standard ULP applications

Consumer low-power/wireless applications

- DFVS
- Massive parallelization

Ultra-low power/energy...
Subthreshold logic trend

- What is the impact of technology scaling? (45 nm?)
- Does partially/fully-depleted SOI bring advantages?

Last chips [IEEE ISSCC’08]:

Ultra-low-power 0.32V motion estimator [Kaul]

Research papers on subthreshold logic [Kwong]
Outline

- SOI for high-performance computing
- Ultra-low-power computing
- MOSFET subthreshold operation
- Subthreshold circuit robustness
- Minimum-energy point
- Practical energy
- Roadmap for nanometer subthreshold circuits

Impact of technology scaling
+ SOI advantages
Subthreshold current

\[ I_{sub} = I_0 \times 10^{V_{gs} + \eta V_{ds} + \sigma V_t} \times \left( 1 - e^{-\frac{-V_{ds}}{V_{th}}} \right) \]
Subthreshold current

\[ I_{sub} = I_0 \times 10 \frac{V_{gs} + \eta V_{ds}}{S} \pm \sigma V_t \]

**Slow \( T_{ox} \) scaling!**

[Boi, TVLSI’09]
Subthreshold swing and DIBL

\[ I_{\text{sub}} = I_0 \times 10^{V_{gs} + \eta V_{ds} \pm \sigma V_t / S} \]

45nm technology

T_{BOX} = 10, 20, 65, 145 nm

S \,[\text{mV/dec}]

T_{Si} \, \text{or} \, X_j \,[\text{nm}]

FD SOI

Expressions from [Skotnicki, TED’08]

BD SOI

T_{BOX} = 10, 20, 65, 145 nm

\eta \,[\text{mV/V}]

T_{Si} \, \text{or} \, X_j \,[\text{nm}]

[Bol, SOIC’08]
BOX fringing field

Source  Gate  Drain

Buried oxide

DIBL_{BOX}

Substrate
Reference current

\[ I_{\text{sub}} = I_0 \times 10^{V_{gs} + \eta V_{ds} \pm \sigma V_t / S} \]

Two possibilities:
- Iso \( I_0 \)
- Iso \( V_t \)

Implementations:
- Doping \( N_{ch} \)
- Gate work function (undoped channel + mid-gap metal gate)
Poly gate

\[ T_{\text{ox,el}} = T_{\text{ox,phys}} + T_{\text{g,dep}} \]

Substrate

Buried oxide

Source     Drain

Gate

Poly depletion
Metal gate

\[ T_{ox,el} = T_{ox,phys} \rightarrow S, \eta \]
Subthreshold current variability

\[
I_{\text{sub}} = I_0 \times 10^{\frac{V_{gs} + \eta V_{ds}}{S} \pm \sigma V_t}
\]

\[
\sigma_{V_t,\text{RDF}} = \frac{AV_{t,\text{RDF}}}{\sqrt{WL_{eff}}} = 3.19 \times 10^{-8} \frac{T_{ox}N_{ch}^{0.4}}{\sqrt{WL_{eff}}}
\]

[Asenov, TED03]

@ \( V_{dd,\text{nom}} \)

[BoL, TVLSI’09]
Variability in FD SOI

\[ I_{sub} = I_0 \times 10^{\frac{V_{gs} + \eta V_{ds}}{S} \pm \sigma V_t} \]

Bulk/SOI comparison: analytical expression

\[
\sigma_{V_t, RDF} = \frac{\partial V_t}{\partial n_c} \sigma_{n_c} = \frac{1}{C_{ox}} \frac{\partial Q_c}{\partial n_c} \sigma_{n_c} = \frac{q T_{ox}}{\epsilon_{ox} W L} \sigma_{n_c}
\]

[Skotnicki, TED’08]

\[
\sigma_{V_t, RDF}|_{bulk} = 4^{\frac{3}{2}} q^3 \epsilon_{Si} \Phi_F N_{ch} \times \frac{T_{ox}}{\epsilon_{ox} \sqrt{W L}}
\]

\[
\sigma_{V_t, RDF}|_{SOI} = q \sqrt{N_{ch} T_{Si}} \times \frac{T_{ox}}{\epsilon_{ox} \sqrt{W L}}.
\]

[Bol, SOIC’08]
Variability in FD SOI

\[ I_{sub} = I_0 \times 10^{\frac{V_{gs} + \eta V_{ds} \pm \sigma V_t}{S}} \]

Bulk/SOI comparison: analytical expression

<table>
<thead>
<tr>
<th>( \sigma_{V_t} [\text{mV}] )</th>
<th>RDF</th>
<th>( T_{Si} )</th>
<th>Other</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>44</td>
<td>0</td>
<td>15</td>
<td>46</td>
</tr>
<tr>
<td>Doped FD SOI</td>
<td>32</td>
<td>15</td>
<td>15</td>
<td>39</td>
</tr>
<tr>
<td>Undoped FD SOI</td>
<td>1.4</td>
<td>~0</td>
<td>15</td>
<td>15.1</td>
</tr>
</tbody>
</table>

[Bol, SOIC’08]
Capacitances in subthreshold regime

Addition of $C_{dep}$ in series with $C_{ox} \rightarrow C_g \downarrow$

Inversion

Substrate

Electrode

Gate

$2/3 C_{ox}$

1V

Source

Drain

Depletion

Substrate

Electrode

Gate

$C_{ox}$

$C_{dep}$

0.2V

$C_{g,sub}$

$C_{g,sub}$

Nominal $V_{dd}$

CFS era

Slow $T_{ox}$ scaling

Subthreshold $V_{dd}$

$C_{g,sub}$

Technology node [nm]

[0, 50, 100, 150, 200, 250]

[0.2, 0.4, 0.6, 0.8, 1.0]

$C [fF/\mu m]$

[Bol, ISVLSI’08]
Parasitic capacitances

Diagrams showing capacitances in a transistor, including:
- Electrode
- Gate
- Source
- Drain
- Substrate

Symbols:
- \( C_{of, top} \)
- \( C_{of, side} \)
- \( C_{of, dif} \)
- \( C_{ov} \)
- \( C_{ox} \)
- \( C_{ov} \)
- \( C_{if} \)
- \( C_{dep} \)
- \( C_j \)
Junction capacitances

More important than $C_g$ in subthreshold regime

[Ref: Bol, ISVLSI’08]
Capacitances in FD SOI

\[ C_{j} \]
\[ C_{i} \]
\[ C_{BOX} \]
\[ C_{Si} \]
\[ C_{OX} \]
Capacitances in FD SOI

Bulk FD SOI

- Capacitances [fF/µm]
  - C_{of}
  - C_{if}
  - C_{ov}
  - C_{j}
  - C_{g,sub}

-25% change in 45 nm technologies

Bulk, FD SOI comparison graph with capacitance breakdown.
## Summary

### 45nm technologies

<table>
<thead>
<tr>
<th></th>
<th>$S$ [mV/dec]</th>
<th>$\eta$ [mV/V]</th>
<th>$I_0$ [pA/µm]</th>
<th>$I_{on}$ var. [-]</th>
<th>$C_L$ [fF/µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>92.5</td>
<td>183</td>
<td>340</td>
<td>30.8</td>
<td>21.5</td>
</tr>
<tr>
<td>Doped FD SOI</td>
<td>72.4</td>
<td>199</td>
<td>340</td>
<td>26.8</td>
<td>17.1</td>
</tr>
<tr>
<td>Undoped FD SOI</td>
<td>70.2</td>
<td>167</td>
<td>340</td>
<td>3.3</td>
<td>18.7</td>
</tr>
</tbody>
</table>

[Bol, SOIC’08]
Outline

• SOI for high-performance computing
• Ultra-low-power computing
• MOSFET subthreshold operation
• Subthreshold circuit robustness
• Minimum-energy point
• Practical energy
• Roadmap for nanometer subthreshold circuits

Impact of technology scaling

+ FD SOI advantages
Functionality

![Graph showing V_out vs V_in for Typical and RDF cases, with SNM indicated.]
Method from [Kwong, ISLPED’06]:

- Monte-Carlo simulation with variability
- Equivalent to infinite NAND-NOR chain
- SNM is the lowest $V_N$, which switches the outputs
- SNM must be positive
Static noise margins

[Graph showing static noise margins (SNM) for different technology nodes (nm) and various conditions such as Without DIBL, Nominal, μ-3σ, and μ-4σ. The graph illustrates the degradation (S) and variability effects as technology nodes change.]

[Bol, TVLSI’09]
Static noise margins in FD SOI

@ 0.3V

SNM [mV]

[0, 20, 40, 60, 80, 100, 120]

Bulk

Doped FD SOI

Undoped FD SOI

DIBL

3σ

4σ

6x

@ 0.3V

[Bol, SOIC’08]
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+ FD SOI advantages
Minimum-energy point

\[ E_{\text{tot}} = E_{\text{dyn}} + E_{\text{stat}} \]
\[ = \frac{1}{2} N_{\text{sw}} C_L V_{dd}^2 + V_{dd} \times I_{\text{leak}} \times T_{\text{del}} \]
\[ E_{\text{stat}} = V_{dd} \times I_0 \times 10^{nV_{dd}/S} \times C_L V_{dd} / I_0 \times 10^{(1+n)V_{dd}/S} \]
\[ = C_L V_{dd}^2 \times I_0 \times 10^{-V_{dd}/S} \]

\[ E_{\text{min}} \sim C_L S^2 \] \[\text{[Hanson, TED’08]}\]
Impact of technology scaling

8-bit RCA multiplier in bulk technologies

Energy per operation [fJ]

$V_{dd}$ [V]

$E_{op}$

$E_{stat}$

$E_{min}$

[130nm, 90nm, 65nm, 45nm]

[Bol, Ph.D’08, to be published]
$E_{\text{min}}$ in nanometer technologies

8-bit RCA multiplier in bulk technologies

$E_{\text{min}}$ [fJ]

130nm 90nm 65nm 45nm

$C_L S^2$

New effects in nanometer technologies

[Bol, Ph.D’08, to be published]
Nanometer limitations on $E_{\text{min}}$

DIBL: increases $I_{\text{leak}}$ by $10^{(\eta V_{dd}/S)}$ decreases $T_{\text{del}}$ by $10^{(k \eta V_{dd}/S)}$

$k \approx 0.25 \text{ to } 0.35$

$I_{\text{gate}}$: increases $I_{\text{leak}}$

Variability: increases $I_{\text{leak}}$ (mean) increases $T_{\text{del}}$ (worst-case)

$$E_{\text{stat}} = V_{dd} \times I_{\text{leak}} \times T_{\text{del}}$$

[Bol, Ph.D’08, to be published]
Technology flavors in bulk

ITRS recommended technology flavors:
- High-Performance
- Low Operating Power
- Low Stand-by Power

8-bit RCA in 45nm bulk technology

Inefficient!
$E_{\text{min}}$ in FD SOI

Doped FD SOI:
Reduction of $C_L$, $S$ and variability

Undoped FD SOI:
Reduction of DIBL and variability

[Bol, Ph.D’08]
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Impact of technology scaling
+ FD SOI advantages
Applications constraints:

- functional yield
- speed yield

Minimum $V_{dd}$

8-bit RCA in 45nm technologies

10x speed increase at 0.4V

[Functional limit]

[Speed limit]

[Bol, SOIC’08]
Practical energy

8-bit RCA in 45nm technologies

Minimum $V_{dd}$ [V]

Throughput [Op/s]

-70% $E_{\text{stat}}$

-60% $E_{\text{min}}$

[Ref: Bol, SOIC’08]
How to reach $E_{\text{min}}$ in practice?

8-bit RCA in 45nm bulk technology

![Graph showing Minimum $V_{dd}$ vs. Throughput]

- **High $V_t$**
- **Low $V_t$**

Versatility needed at design time

$E_{\text{min}}$ range

$= \text{multi-}I_0 \text{ devices}$

[Bol, ICCD’08]
Wider granularity

8-bit RCA in 45nm bulk technology

Minimum $V_{dd}$ [V]

Throughput [Op/s]

Energy per operation [J]

Versatility needed at design time

= multi-$I_0$ devices

with large granularity
Dual-\(V_t\) assignement

Inefficient because:

- Delay difference increase in subthreshold regime
- Short paths feature higher variability

45nm bulk

[45nm bulk graph showing maximum N vs. \(V_{dd}\) with typical and with variability, illustrating inefficiency]

[Inefficiency!]

[Bol, Ph.D’08, to be published]
Circuit adaptation

- Global process variations
- Temperature variations
- Modeling errors
- Device aging

\[ E_{\text{op}} \]

Throughput

Model

Actual

Adapt.

\( \text{target } f_{\text{op}} \)

\( \text{actual } f_{\text{clk,opt}} \)
Circuit adaptation in bulk

Adaptive reverse body-bias is better than adaptive \( V_{dd} \)

[Bo, Ph.D’08, to be published]
Circuit adaptation in bulk

\[ V_t = V_{t,\text{ref}} - \gamma V_{BB} \]

\[ I_0 = I_{0,\text{ref}} \times \kappa V_{BB} \]

<table>
<thead>
<tr>
<th>Bulk technologies</th>
<th>( \gamma ) [mV/V]</th>
<th>( \kappa ) [x/V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>130nm GP</td>
<td>150</td>
<td>125</td>
</tr>
<tr>
<td>45nm GP</td>
<td>85</td>
<td>14</td>
</tr>
<tr>
<td>45nm LP</td>
<td>120</td>
<td>50</td>
</tr>
</tbody>
</table>

Need large \( V_{BB} \) to shift \( E_{\text{min}} \) sufficiently

Problem in 45 nm GP! What at 32 nm?

Body bias is fine in 45 nm LP technology

[Bol, Ph.D’08, to be published]
FD SOI with

- 145nm $T_{\text{BOX}}$
- 1.1nm $T_{\text{ox}}$
- 10nm $T_{\text{Si}}$

$\gamma < 10 \text{ mV/V}$

How to reach sufficient $\gamma$?

- Ultra-thin BOX [Tsuchyia, IEDM’07]
- Dual-gate devices with independent-gate config. [Masahara, TED’05]
• SOI for high-performance computing
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Outline

Impact of technology scaling
+ FD SOI advantages
Technology/circuit specs

1. Reducing \( E_{\text{min}} \)

Technology level

- Single device type for all logic gates
- Low \( C_L, S, \text{DIBL, variability (} I_0 \text{)} \)
- \( I_{\text{gate, junc}} < I_{\text{sub}} @ 0.3-0.4V \)

Relaxed constraints:
- \( C_{\text{g,sub}} \)
- \( I_{\text{gate, junc}} \)
- \( R_{s,d,g} \)
- Mobility
- Multi-\( I_0 \) devices with coarse granularity
- On-chip \( I_0 \) tuning with fine granularity

2. Reaching \( E_{\text{min}} \)

Circuit level

- Design-time device selection
- Run-time adaptive technique
- \( I_0 \) tuning
- Sleep-mode technique
- High leakage reduction
- Low impact on active-mode operation

[Boi, Ph.D’08, to be published]
## Technology/circuit roadmap

<table>
<thead>
<tr>
<th>Applications</th>
<th>Node 130 / 90 nm</th>
<th>Node 65 / 45 nm</th>
<th>Node 32 / 22 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard ULP applications</td>
<td>Subthreshold logic • Bulk (+ adapt. RBB)</td>
<td>Subthreshold logic • Bulk + adapt. RBB</td>
<td>Economical issues</td>
</tr>
<tr>
<td></td>
<td>• (FD SOI) @ GP flavor</td>
<td>• FD SOI @ LP flavor</td>
<td></td>
</tr>
<tr>
<td>ULP mode in LP applications</td>
<td>Performance issues</td>
<td>Subthreshold logic • Bulk opt. + adapt. RBB</td>
<td>Subthreshold logic • FD SOI + UTBOX/DG + adapt. dual-BG bias</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• FD SOI @ HP/GP flavor</td>
<td>• @ dedicated flavor</td>
</tr>
</tbody>
</table>

Architectural techniques (\/, pipe) for meeting throughput constraint

**Bonus track:** in **ULP circuits**, there is no self heating

[SOI appropriate]  
[Bol, Ph.D’08, to be published]
Conclusions and challenges

• Advantages of **PD SOI** for **high-performance** applications are well known

• Advantages of **FD SOI** are magnified at low voltages for (ultra-) **low-power** applications

• Advantages of FD SOI
  – **Doped + Poly-gate**: $C_L$ reduction (from $C_j$), S and variability reduction
  – **Undoped + metal-gate**: further S, DIBL and variability reduction
  – Solve robustness and $E_{\text{min}}$ issues

• Challenges of FD SOI
  – Technology versatility (different $I_0$)
  – Low-cost adaptive technique

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Common to all logic gates
Thin BOX
DG SOI
SOI is even more valuable for (ultra-) low-power applications than for high-performance ones

Thank you!

Any questions?

Acknowledgement:

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References


[Bol, SOIC'08] D. Bol, R. Ambroise, D. Flandre and J.-D. Legat, “Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications”, in Proc. IEEE International SOI Conference, pp. 57-58, 2008. This poster presentation was awarded as Best Poster of the conference.


