Ultra-Low-Voltage Nanometer CMOS Circuits for Smart Energy-Autonomous Systems

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UCL’s breath recording system

- Humidity sensor with capacitive I/F and wireless transmission over IEEE802.15.4
- Diagnosis of sleep apnea-hypopnea syndrome
- Custom sensor with COTS µC and radio
- 2x AAA batteries
- Autonomy limited to 40hrs 😞

[André, IEEE J. Sensors, 2010]
IMEC’s EEG monitoring

- 1cm³ 8-channel ambulatory EEG system
- Custom readout with COTS μC and radio
- 120 mAh Li-ion battery 60hrs autonomy 😞
- Power dominated by radio and μC [Yazicioglu, IEEE JSSC’08]
  [Yazicioglu, Micro. J’08]

MIT’s EEG monitoring

- 1-channel EEG seizure detection system
- 0.18μm CMOS 1V SoC with custom readout + feature extraction processor

Dedicated on-chip processing saves radio bandwidth

40x power savings 😊

Limited programmability 😞

[Verma, VLSI’09] [Verma, JSSC’10]
TI’s EEG SoC

- 3mm² EEG seizure detection system [Sridhara, SVLSI’10]
- Custom Cortex-M3 μC + dedicated HW 😊 programmability
- 0.13μm CMOS, power @ 0.5V< 1μW
- Max. freq.: 7kHz @0.5V – 5MHz @1V 😞

Energy-Autonomous Systems

- **Radio bandwidth** is limited by available energy
- On-chip processing costs less energy than wireless communications
- Need **smart EAS** to transmit only useful data
- Constraint: currently low-volume market → require low NRE and generic platforms
Outline

- Motivation
- **Why ULV in nanometer CMOS circuits?**
- ULV logic design challenges
- FD SOI technology
- ULV targets and roadmap
- Test case
**Ultra-low-voltage nano-CMOS**

**Motivations 😊**

- **$V_{dd} \leq 0.5V$:** MOSFETs in near/subthreshold regime
  - Logic: low active energy $E_{op}$
  - Memories: low static power $P_{\text{leak}}$

**Limitations 😞**

- Speed penalty
- Sensitivity against variations

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**$V_{dd}$ scaling**

8-bit RCA multiplier in 130nm technology

- **$E_{op}$**
  \[ E_{op} = \int^{T_{op}} P_{\text{tot}} \, dt \]

- **$E_{op}$**
  \[ E_{op} = \frac{1}{2} N_{\text{sw}} C_{L} V_{dd}^2 R_{3} \]
  \[ + V_{dd} \times I_{\text{leak}} \times T_{op} \]

- Scaling $V_{dd}$ below $V_{min}(R3/R2)$ is not useful
- $E_{min}$ at one particular target frequency!

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["D. Bol, Analysis and minimization of practical energy in 45nm subthreshold logic circuits, 2008, Best Paper Award"]
Outline

- Motivation
- Why ULV in nanometer CMOS circuits?
  - **ULV logic design challenges**
    - Energy efficiency
    - Robustness
    - Timing closure
- ULV targets and roadmap
- Test case
Energy efficiency

![Graph showing energy efficiency](image)

**Theoretical E\textsubscript{min} scaling trend**

- T=25°C
- TCAD models
- LSTP bulk
- Min. L
- Constant W/L
- No variability

\[ V_{\text{min}} \sim S \]
\[ E_{\text{min}} \sim C_L S^2 \]

[Hanson, IEEE TED, 2008]
Practical $E_{\text{min}}$ scaling trend

Increase in:
- Subthreshold swing
- Gate leakage
- DIBL
- Variability (RDF)

leads to $E_{\text{min}}$ penalty in nano-CMOS technologies

[D. Bol, Nanometer MOSFET effects on the minimum-energy point of 45nm subthreshold circuits, ACM/IEEE ISLPED, 2009] [D. Bol, ACM TODAES, 2010]

Optimum MOSFET selection

Table 1: Subthreshold MOSFET characteristics

<table>
<thead>
<tr>
<th>Device</th>
<th>$S$ (mV/dec)</th>
<th>$\eta$ (mA/V)</th>
<th>$L_{\text{var}}$</th>
<th>$L_{\text{opt}}/L_{\text{bas}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>92.5</td>
<td>183</td>
<td>20.7</td>
<td>0.99</td>
</tr>
<tr>
<td>Optimum</td>
<td>81.9</td>
<td>83</td>
<td>13.1</td>
<td>0.09</td>
</tr>
</tbody>
</table>

[D. Bol, Nanometer MOSFET effects on the minimum-energy point of 45nm subthreshold circuits, ACM/IEEE ISLPED, 2009] [D. Bol, ACM TODAES, 2010]
Energy efficiency

- $E_{\text{leak}}$ is increased
- $E_{\text{op}}$ as $f_{\text{target}}$ increases

Technology flavors

- Commercial 65/45nm technology:
  - **GP flavor**
    - 1V
    - 1-3GHz
    - 10-100W
  - **LP flavor**
    - 1.2V
    - 100-600MHz
    - 0.5-5W

For smart EAS, what to choose?

[D. Bol et al., Technology flavor selection and adaptive techniques for timing-constrained 45nm subthreshold circuits, ACM/IEEE ISLPED, 2009]
Technology flavors for ULV CMOS

Commercial 65/45nm technology:

- **GP flavor**
  - 0.3-0.5V
  - 1-50MHz
  - 10-500μW

- **LP flavor**
  - 0.3-0.5V
  - 10kHz-1MHz
  - 0.1-10μW

**Smart EAS**

[D. Bol et al., Technology flavor selection and adaptive techniques for timing-constrained 45nm subthreshold circuits, ACM/IEEE ISLPED, 2009]

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Minimum-energy @ target frequency

High $I_{\text{leak}}$ in GP requires leakage reduction technique:

- **Active mode**:
  - Dual-V, not feasible
  - too large delay difference at ULV

- **Sleep-mode**:
  - RBB not effective
  - low body effect
  - Power-gating harms robustness

[D. Bol et al., Technology flavor selection and adaptive techniques for timing-constrained 45nm subthreshold circuits, ACM/IEEE ISLPED, 2009]
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- Why ULV in nanometer CMOS circuits?
  - ULV logic design challenges
    - Energy efficiency
    - Robustness
    - Timing closure
- FD SOI technology
- ULV targets and roadmap
- Test case
**Logic noise margins**

- S degradation
- DIBL
- Variability
- Functional failure

![Benchmark circuit to estimate probability of functional faults in logic](Kwong, ISLPED'06)

[D. Bol et al., Interests and limitations of technology scaling for subthreshold logic, IEEE Trans. VLSI, 2009]

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**ULV circuit robustness**

- 3σ functional yield
- Robust 0.3V operation is no longer reachable in 45/32nm technologies

![Functional failure](Pu, JSSC’09) ![Functional failure](Kwong, JSSC’09)

Existing solutions: • Library redesign
• Adaptive β ratio

Our solutions: • Logic gates with limited stacks
• Channel length upsize

[D. Bol, IEEE Trans. VLSI, 2009]
Robustness-aware sleep transistor engineering for power-gated nanometer subthreshold circuits

### Power gating and robustness

45nm LP simulations

- **$V_{dd} = 0.35V$**
- Sleep-transistor series resistance harms robustness

![DIBL!](image)

[D. Bol et al., Robustness-aware sleep transistor engineering for power-gated nanometer subthreshold circuits, IEEE ISCAS, 2010]

### Sleep transistor engineering

#### 45nm LP simulations

<table>
<thead>
<tr>
<th>Sleep-mode technique</th>
<th>Min. Vdd for iso-robustness</th>
<th>$E_{min}$ penalty</th>
<th>$E_{sleep}$ reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>RBB @ $E_{min}$</td>
<td>0.35</td>
<td>0 %</td>
<td>9.6x</td>
</tr>
<tr>
<td>Conv. sleep transistor</td>
<td>0.42</td>
<td>19 %</td>
<td>105x</td>
</tr>
<tr>
<td>Opt. sleep transistor</td>
<td>0.37</td>
<td>8 %</td>
<td>108x</td>
</tr>
<tr>
<td>Opt. sleep transistor</td>
<td>0.41</td>
<td>18 %</td>
<td>168x</td>
</tr>
</tbody>
</table>

[D. Bol et al., Robustness-aware sleep transistor engineering for power-gated nanometer subthreshold circuits, IEEE ISCAS, 2010]
Motivation

Why ULV in nanometer CMOS circuits?

**ULV logic design challenges**
- Energy efficiency
- Robustness
- Timing closure

FD SOI technology

ULV targets and roadmap

Test case

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Timing closure

At **ULV**: 1) temperature impact on delay stronger than global PV
2) low temperature = worst case

[D. Bol et al., The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic, ESSCIRC, 2010]
PVT-induced $T_{cycle}$ margins

Lower bound of industrial temperature range (-40°C) degrades speed by a factor 5.3x

<table>
<thead>
<tr>
<th></th>
<th>Room</th>
<th>Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{cycle}$ margin</td>
<td>25°C</td>
<td>-40°C</td>
</tr>
<tr>
<td>20mV $V_{dd}$ drop</td>
<td>60%</td>
<td>95%</td>
</tr>
<tr>
<td>3σ die-to-die process variations</td>
<td>43%</td>
<td>75%</td>
</tr>
<tr>
<td>SS process corner</td>
<td>55%</td>
<td>96%</td>
</tr>
<tr>
<td>Combined PVT</td>
<td>2.3x</td>
<td>18.1x</td>
</tr>
</tbody>
</table>

Low temperature further increases the sensitivity against process and voltage variations (deeper sub-$V_t$)

[D. Bol et al., The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic, ESSCIRC, 2010]

Impact of RDF on timing

ULV circuits in nano-CMOS are prone to hold time violations

[Kwong, IEEE J. Solid-State Circuits, 2009]
Temperature and timing uncertainties

- Temperature magnifies path delay variations
- Low-temperature is a worst case for hold time

[D. Bol et al., The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic, ESSCIRC, 2010]

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FD SOI technology

Partially-depleted (PD) SOI
- Poly-Si gate
- Buried oxide (BOX)
- $T_{\text{dep}} \sim 1/VN_{\text{ch}}$
  - Doping similar to bulk to control the SCE
- 32nm FD SOI MOSFET with high-$\kappa$/metal gate

Fully-depleted (FD) SOI
- Mid-gap metal gate
- Buried oxide (BOX)
- Undoped channel
- [Weber, IEDM’08]
  - No RDF $\rightarrow$ low variability
  - No history effect

FD SOI for ULV circuits

<table>
<thead>
<tr>
<th>45nm technologies</th>
<th>$S$ [mV/dec]</th>
<th>$\eta$ [mV/V]</th>
<th>$I_0$ [pA/µm]</th>
<th>$\sigma_V$ [mV]</th>
<th>$C_L$ [fF/µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>92.5</td>
<td>183</td>
<td>340</td>
<td>46</td>
<td>21.5</td>
</tr>
<tr>
<td>Undoped FD SOI</td>
<td>70.2</td>
<td>167</td>
<td>340</td>
<td>15.1</td>
<td>18.7</td>
</tr>
</tbody>
</table>

- Energy: -60% $E_{\text{min}}$
- Speed: 10x boost @0.4V
- Robustness: minimum $V_{\text{dd}}$ -90 mV

[D. Bol et al., ACM TODAES, 2010]
[D. Bol et al., Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications, IEEE SOI Conference, 2008], Best Poster award
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ULV technology/circuit specifications

1. Reducing $E_{\text{min}}$
   Technology level
   - Single device type for all logic gates
   - Low $C_{\text{gs}}$, $S$, DIBL, variability ($I_0$)
   - $I_{\text{gate}} < I_{\text{junc}} < I_{\text{sub}} @ 0.3-0.4\text{V}$
   - Relaxed constraints:
     - Gate capacitance
     - Mobility
     - Gate/junction leaks
     - Access resistances
     - Multi-$I_0$ devices with coarse granularity
     - On-chip $I_0$ tuning with fine granularity

2. Reaching $E_{\text{min}}$
   Circuit level
   - Active
     - $I_0$ tuning
   - Stand-by
   - Design-time device selection
   - Run-time adaptive technique
   - Sleep-mode technique
     - High leakage reduction
     - Low impact on active-mode operation

[D. Bol, "Roadmap for nanometer ultra-low-power digital circuits based on sub/near-threshold CMOS logic", www.soconsortium.org, 2009]
### ULV technology/circuit roadmap

<table>
<thead>
<tr>
<th>Node</th>
<th>130 / 90 nm</th>
<th>65 / 45 nm</th>
<th>32 / 22 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applications</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EAS for basic ULP applications</td>
<td>Subthreshold logic</td>
<td>Subthreshold logic</td>
<td>Economical issues</td>
</tr>
<tr>
<td>&lt; 5µW</td>
<td>Bulk std devices</td>
<td>Bulk opt. devices</td>
<td>@ GP flavor</td>
</tr>
<tr>
<td>@0.01-1MIPS</td>
<td>@ GP flavor</td>
<td>@ LP flavor</td>
<td>+ ULV design flow</td>
</tr>
<tr>
<td>Smart EAS for new applications</td>
<td>Performance issues @ULV</td>
<td>Near-threshold logic</td>
<td>Near-threshold logic</td>
</tr>
<tr>
<td>5-100µW</td>
<td></td>
<td>Bulk opt. devices</td>
<td>UTB FD SOI</td>
</tr>
<tr>
<td>@1-50MIPS</td>
<td></td>
<td>@ GP flavor</td>
<td>@ dedicated flavor</td>
</tr>
<tr>
<td>Architectural techniques (//, pipe)</td>
<td>for meeting target frequency</td>
<td>+ ULV design flow</td>
<td>+ ULV design flow</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ power gating</td>
<td>+ ???</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ arch. technique</td>
<td></td>
</tr>
</tbody>
</table>

[D. Bol, "Roadmap for nanometer ultra-low-power digital circuits based on sub/near-threshold CMOS logic", www.soiconsortium.org, 2009]

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AES coprocessor for secure RFID tags

- ULV design flow - 65nm LP
- 8-bit architecture
- 3.5 kGE - 0.012 mm²
- Internal CLK generator

Power Budget for:
- HF (13.56 MHz): 22.5 µW
- UHF (900 MHz): 4 µW

AES preliminary results

- ULV flow saves 5-10% energy
- Upsized L_g saves 10-15% energy
- Fits within passive RFID power budget

[C. Hocquet et al., to be published, 2010]
Conclusions

- Autonomy/functionality of EAS is limited by radio power
- Need smart EAS with processing capability to limit radio usage
- ULV circuit operation + nanometer CMOS technologies enables boosted processing capability within μW power budget
- Proposed design techniques @65/45nm enable easy and fast design (low NRE) for versatile smart EAS

\[E_{\text{op}} \text{ extrapolated at minimum reported } V_{\text{dd}} \text{ from 1.5V with } V_{\text{dd}}^2 \text{ scaling law}\]

Fast and low-cost ULV design flow in 65nm LP → strong energy reduction without efforts devoted to architecture/circuit optimizations

\[C. Hocquet et al., to be published, 2010\]
Thank you!

Any questions?

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- D. Bol’s work is funded by FNRS and Walloon region of Belgium
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References