Publications of David Bol

PAPERS IN SCIENTIFIC JOURNALS


BOOK CHAPTER


PATENTS


INVITED TUTORIALS AND KEYNOTES


• D. Bol and D. Flandre, “Fully-depleted SOI for nanometer subthreshold circuits”, in tutorial on “FD SOI” of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EuroSOI), 2008.
• D. Bol, “Digital design on SOI in the nanometer era - from high-performance to ultra-low-power circuits”, in tutorial on “SOI design” of the 5th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EuroSOI), 2009.
• D. Bol, “Digital design on SOI in the nanometer era - from high-performance to ultra-low-power circuits”, in tutorial on “SOI design” of the 5th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EuroSOI), 2009.

CONTRIBUTIONS IN INTERNATIONAL CONFERENCES

• G. de Streele, J. De Vos and D. Bol, “A ΔVr: 0.2V to 1V 0.01mm² 9.7nW Voltage Reference in 65nm LP/GP CMOS”, in Proc. IEEE SOI-3D-Subthreshold Microelectronics Tech. Unified Conf., 2 p., 2015.


- G. de Streel, J. De Vos, D. Flandre and D. Bol, “A 65nm 1V to 0.5V linear regulator with ultra-low quiescent current for mixed-signal ULV SoCs”, in Proc. IEEE FTTC Conference, 4 p., 2014. This paper was awarded the Best student IC Design Award of the conference.


• D. Bol, R. Ambroise, D. Flandre and J.-D. Legat, “Sub-45nm fully-depleted SOI CMOS subthreshold logic for ultra-low-power applications”, in Proc. IEEE International SOI Conference, 2 p., 2008. This poster presentation was awarded as Best Poster of the conference.


