

Glitch-Induced Within-Die Variations of Dynamic Energy in Voltage-Scaled Nano-CMOS Circuits

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Abstract—Variability strongly impacts performances of nanometer CMOS digital circuits. In this paper, we experimentally study the effects of variability on dynamic energy consumption of 65nm logic circuits, considering deep voltage scaling for low-power applications. While we confirm that variations in dynamic energy at 1V are small and dominated by die-to-die correlated capacitance fluctuations, we report for the first time that within-die uncorrelated delay variability magnifies dynamic energy variations at lower voltages by a factor $5\times$. Indeed, random glitches are generated by variability-induced unbalanced logic paths, which affect the activity factor of combinatorial circuits. The associated normalized dynamic power variations at 0.4V are comparable to die-to-die leakage power variations.

I. INTRODUCTION

The high demand for portable electronic applications motivates the use of advanced power-management techniques aiming at minimizing energy per operation. Amongst them, voltage scaling is the most straightforward. It leads to a quadratic reduction in the energy consumed to switch internal capacitances at the expense of delay penalty [1]. Voltage scaling can either be static with a fixed V_{DD} reduction at design time or dynamic with on-demand V_{DD} lowering in low-power modes [2]. When speed performances are not critical, V_{DD} can ultimately be set at a value below the threshold voltage V_t , leading to the so-called subthreshold logic [3], [4].

On top of this, CMOS technology scaling brings increased speed performances and functionalities with reduced energy per operation. However, when reaching nanometer-scale geometries for MOSFET devices, variability becomes a serious concern [5]. The variability impact on circuit performances should thus be properly characterized and modeled for allowing its prediction and minimization at design time. On the first order, MOSFET variability sources can be classified into two main categories:

- spatially-correlated variations that equally affect all transistors from the same type on die-to-die (D2D), wafer-to-wafer (W2W) or lot-to-lot (L2L) basis,
- uncorrelated variations that affect each transistor independently on a within-die (WID) basis.

At circuit level, these sources induce delay variations. Cycle time margins are thus required to accommodate worst-case delay. This has traditionally been dealt with at design time by carrying out global process corner simulations. However, the recent increase of uncorrelated variability sources in nanometer CMOS technologies such as random dopant fluctuations

(RDF) and line edge roughness (LER) has motivated the development of statistical static timing analysis tools [6]. They help to avoid overestimating margins, by taking averaging effect and parametric yield into consideration. Deep voltage scaling worsens the picture by magnifying the sensitivity against MOSFET variations [7]. Noticeably, V_t contribution to delay variations increases as V_{DD} is scaled down. This comes from I_{on} dependence on V_t , which increases with the reduction of the gate overdrive voltage ($V_{DD} - V_t$) and which ultimately becomes exponential in subthreshold regime. Uncorrelated variations might lead to hold time violations due to high timing uncertainties [8] as well as severe functionality issues due to vanishing noise margins [9]. These effects get worse when entering the nanometer era [10].

Variability sources also strongly affect leakage power of logic circuits through variations of subthreshold leakage. Its exponential dependence on V_t and L_g through short-channel and DIBL effects makes it also highly sensitive to both correlated and uncorrelated variability sources [5]. Statistical simulation/prediction of leakage power has been an important research field for the past few years [11], [12].

On the contrary, dynamic energy has been considered up to now as weakly sensitive to variability [5], [11] and is thus not usually modeled in circuit simulations [7], [12], [13] nor explicitly measured in circuit characterizations [14]–[16]. In this paper, we experimentally study dynamic energy variations in voltage-scaled logic circuits through measurement of a 65nm test chip in a low-power (LP) CMOS process. While we confirm that dynamic energy variations remain low at 1V, we demonstrate for the first time that uncorrelated delay variability significantly magnifies it at low voltages because of the generated random glitches caused by spatial randomness between manufactured circuits. Indeed, noise-induced temporal randomness does not come from MOSFET variability and is thus beyond the scope of this paper. From this study, we show that dynamic energy variability cannot be neglected in combinatorial circuits at low voltages and that statistical simulations are required for properly capturing worst-case energy consumption.

This paper is organized as follows. Section II presents the 65nm test chip implemented for experimentally monitoring variations of dynamic energy. Measurement results are presented and analyzed in sections III and IV, respectively.

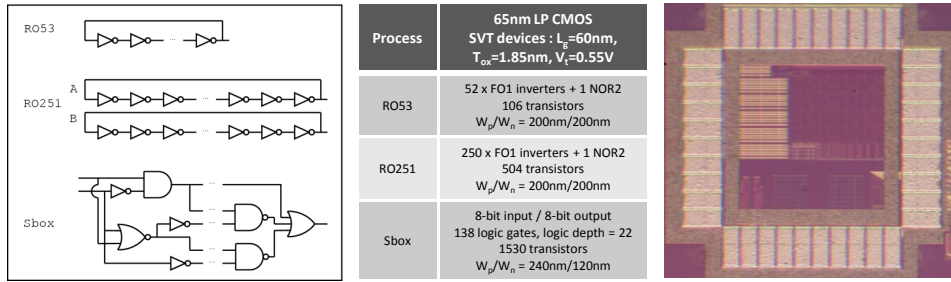


Fig. 1. Test chip schematic, characteristics and microphotograph.

II. TEST CHIP AND MEASUREMENT SETUP

For monitoring dynamic energy variations of digital circuits, a test chip has been fabricated in a 65nm low-power (LP) CMOS technology whose characteristics are given in Fig. 1. It features logic circuits with different topologies to highlight various variability effects. First, an FO1 inverter ring oscillator enables the characterization of simple effects. It comes in two versions with 53 (RO53) and 251 (RO251) stages to investigate the impact of averaging on variability. Second, a non-regular combinatorial circuit is designed to investigate complex effects. This circuit is an Sbox from the *Advanced Encryption Standard* (AES), with the architecture from [17] as implemented in [18]. It has an 8-bit architecture, which features 1,530 transistors in static CMOS logic style and a maximum logic depth of 22. Standard- V_t (SVT) devices are used with minimum gate length and small device widths for low power concern but not minimal to avoid magnifying variability. In order to enable measurements for a wide range of supply voltages, the test chip contains buffers and level shifters. Fig. 1 shows the microphotograph of the test chip.

Two copies (A and B) of RO251 test circuit are placed on each die to monitor within-die variability. A single copy of RO53 and Sbox test circuits is on each die. Measurement results are based on data from 20 dies. All circuits on the 20 measured dies are operational with scaled V_{DD} down to 0.2V. However, we limit our analysis to 0.4V, as the huge delay penalty below 0.4V strongly limits the possible applications. Dynamic energy (E_{dyn}) is extracted from total power (P_{tot}), leakage power (P_{leak}) and frequency ($freq$) data following:

$$E_{dyn} = \frac{P_{tot} - P_{leak}}{freq}. \quad (1)$$

For ring oscillators, P_{tot} is measured at their natural oscillating frequency, while P_{leak} is measured when gating the oscillation through a NOR gate. For the Sbox, P_{tot} is measured with a pseudo-random 2560-transition input pattern, at 100 kHz to avoid timing problems at low voltage. P_{leak} is measured as the average consumption over the 2^8 input vectors, under static conditions.

III. MEASUREMENT RESULTS

In this section, we present the raw measurement results before analyzing them in section IV.

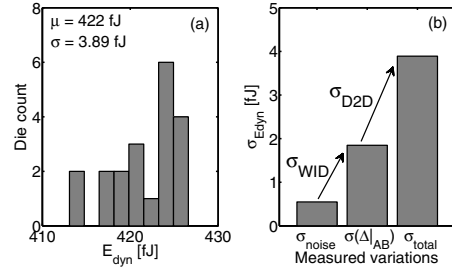


Fig. 2. (a) Measured E_{dyn} of a 251-stage FO1 ring oscillator (RO251) for 20 dies at 1V and (b) standard deviations of the performed measurements.

TABLE I
MEASURED RELATIVE CONTRIBUTIONS TO TOTAL E_{dyn} VARIATIONS

σ/μ [%]	noise	WID	D2D
@1V	0.13	0.42	0.80
@0.4V	0.23	0.53	0.76

A. Contributions to E_{dyn} variations for RO251 circuit

Fig. 2 (a) shows the E_{dyn} histograms for copy A of RO251 test chip at 1V. Total measured E_{dyn} variations come from three contributing variables: measurement noise, within-die (WID) and die-to-die (D2D) variability. We consider these variables as independent so that the measured total E_{dyn} standard deviation σ_{total} can be expressed as:

$$\sigma_{total} = \sqrt{\sigma_{noise}^2 + \sigma_{WID}^2 + \sigma_{D2D}^2}. \quad (2)$$

In order to evaluate the importance of each contribution, we first perform noise measurement on a single die by simply repeating the measurement step 20 times. The resulting σ_{noise} is shown in Fig. 2 (b). It is an order of magnitude below σ_{total} . Second, we perform differential measurement of A and B copies of RO251 circuit on each die. For estimating the importance of within-die contribution, we then compute the standard deviation of the E_{dyn} difference between A and B copies, denoted as $\sigma(\Delta|_{AB})$. Computed values are shown in Fig. 2 (b). From these measurements, we can isolate noise, WID and D2D contributions to total E_{dyn} variations with Eq. (2). The relative standard deviation normalized to mean E_{dyn} for copy A of RO251 over the 20 dies are given in Table I. Die-to-die contribution dominates, while noise contribution is small. Similar contributions are observed at 0.4V.

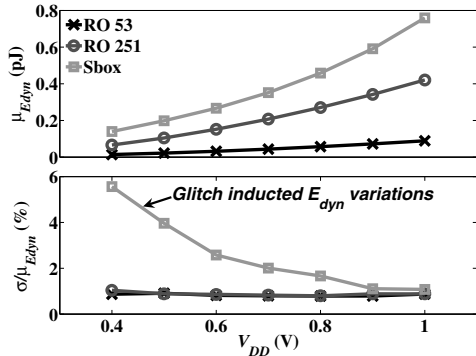


Fig. 3. Measured mean and relative standard deviations of dynamic energy for ring oscillators (RO53 and RO251) and Sbox circuits.

B. E_{dyn} variations vs. circuit type

Fig. 3 shows the mean (μ) measured E_{dyn} of the 20 dies for RO53, RO251 and Sbox circuits with their normalized standard deviation σ/μ , as a function of the supply voltage V_{DD} . Mean E_{dyn} in ring oscillators increases with the number of stages while their E_{dyn} variability is pretty stable over the whole V_{DD} range with $\sigma/\mu \sim 1\%$. In contrast, E_{dyn} variability of the Sbox, although comparable at 1V, increases dramatically at lower voltages with $\sigma/\mu = 5.6\%$ at 0.4V. This reveals a new phenomenon in low-voltage combinatorial circuits.

IV. RESULTS ANALYSIS

The dynamic energy is composed of two parts, the switching component (E_{SW}) due to charging of capacitive loads and the short circuit component (E_{SC}) due to the direct current path from the supply voltage to the ground. Short-circuit energy is usually 10 % of the total E_{dyn} at nominal V_{DD} and is even neglected at subthreshold operation [1]. We thus simplify the nominal E_{dyn} expression of an n -gate circuit to the summation of switching energies E_{SW} of all gates:

$$E_{dyn} = \sum_{gate} E_{SW} = V_{DD}^2/2 \times \sum_{j=1}^n (\alpha_{F,j} \cdot C_{L,j}) \quad (3)$$

where $\alpha_{F,j}$ represents the activity factor and $C_{L,j}$ the load capacitance of the j^{th} gate.

When it comes to variability, we model E_{dyn} as a normal distribution. As a consequence, E_{dyn} can be considered as a summation of normally distributed random variables ($\alpha_F \cdot C_L$), since V_{DD} is considered as fixed.

A. Load capacitance variability

Fig. 3 shows that relative E_{dyn} variations of both RO53 and RO251 circuits are small and roughly constant over the whole V_{DD} range. This can be explained by analyzing the impact of variability on Eq. (3). As the activity factor is fixed in ring oscillators, the only possible variability source is capacitance fluctuation.

As shown in [19], WID C_L variability is quite small and mainly due to random dopant fluctuations. For a device with 30nm channel length and 30nm width σ/μ is below 1% at

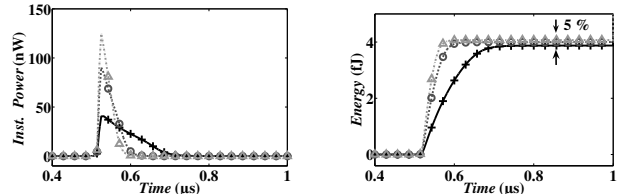


Fig. 4. SPICE simulations of 3 particular Monte Carlo runs of dyn. power and dyn. energy of a single inverter due to short circuit current at 0.4V.

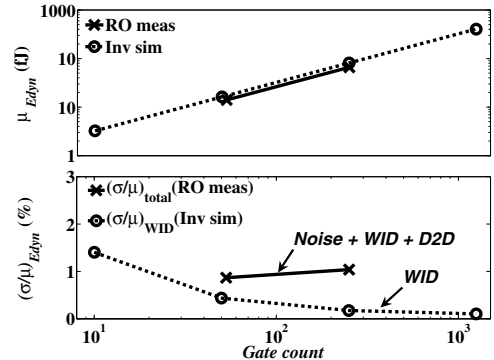


Fig. 5. Measured and simulated average dynamic energy and variability of ring oscillators as a function of gate count at 1V.

1V [19]. To illustrate this idea, Fig. 4 shows the instantaneous power in three extreme Monte-Carlo runs of a single inverter under high-to-low input transition, when enabling WID variations. It is clear that even though the instantaneous power strongly varies, E_{dyn} variations remain within 5% while including all variability sources i.e. capacitances and currents. Moreover, as WID variations are uncorrelated, they are averaged out over the number of stages n in the ring oscillator as:

$$\sigma_{WID} |_{RO} = \sqrt{n} \times \sigma_{WID} |_{inverter}. \quad (4)$$

This is confirmed in Fig. 5 from Monte-Carlo SPICE simulations of an inverter chain with a varying number of stages. In these simulations only WID contribution is considered, which clearly demonstrates the averaging effect on E_{dyn} variations.

Finally, we perform corner simulations, which show a global C_L variability around 3.5 % at 1V between FF (Fast NMOS, Fast PMOS) and SS (Slow NMOS, Slow PMOS) corners. This is an upper bound as it includes D2D, W2W and even L2L variability. This further validates the limited E_{dyn} variability for ring oscillator structures dominated by correlated D2D capacitance fluctuations, for the whole V_{DD} range.

B. Activity factor variability

In Fig. 3, it can be seen that E_{dyn} variations of the Sbox closely match variations of the ring oscillators at 1V, which indicates that it is also dominated by D2D C_L fluctuations. However, when V_{DD} is scaled down, E_{dyn} variations dramatically rise with a normalized standard deviation (σ/μ) up to 5.6% at 0.4V. From Eq. (3), it can only come from the activity factor α_F . As explained in [1], α_F is a function of topology, signal statistics and spurious transitions or glitches associated to delay skew and logic depth. Up to now α_F has

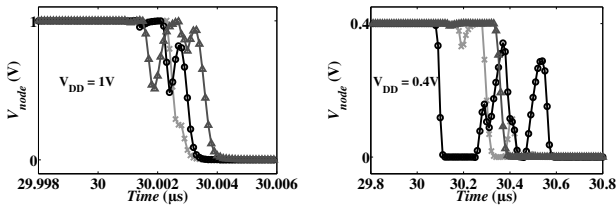


Fig. 6. SPICE simulations (3 Monte Carlo runs) of an internal Sbox node voltage at $V_{DD} = 1V$ and $V_{DD} = 0.4V$.

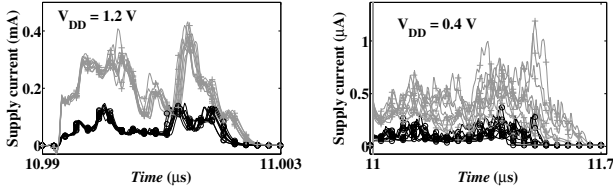


Fig. 7. Sbox supply current traces of 10 Monte Carlo runs for two random input vectors at $V_{DD} = 1.2V$ and $V_{DD} = 0.4V$.

TABLE II

MEASURED RELATIVE VARIATIONS OF DYNAMIC AND LEAKAGE POWER

σ/μ [%]	P_{dyn}	P_{leak}
@1V	1.07	8.23
@0.4V	5.56	8.90

been regarded as deterministic for a given circuit topology and input transition. However, measurement results of the Sbox show that α_F becomes randomly distributed between manufactured circuits at low voltage.

As a demonstration, we perform Monte-Carlo simulations of an internal node voltage of the Sbox, while considering WID variations. Fig. 6 shows the simulated waveforms for three distinct Monte-Carlo runs at 1V and 0.4V, with a single input transition. Although the topology, signal statistics, input transition and logic depth are the same, the node activity considerably varies and increases at 0.4V. This comes from WID delay variability that is magnified at low voltage. It introduces large delay skews, which generates random glitches and thus α_F variations. This affects the dynamic power consumption as seen from the supply current traces in Fig. 7, where the WID variability effect on α_F is clearly shown at 0.4V. This explains the increase in E_{dyn} variations of the Sbox at low voltages as observed in measurement results from Fig. 3. The associated impact on dynamic power ($E_{dyn} \times freq$) variations becomes comparable to the measured D2D P_{leak} variations as shown in Table II.

It is worth mentioning that E_{dyn} variations reported in this paper for the Sbox are a result of power measurement averaged over a 2560-transition input pattern. Worst-case input transitions also exist that feature higher E_{dyn} variations. For example, we measured relative E_{dyn} standard deviation (σ/μ) up to 8% for input patterns with 256 transitions.

V. CONCLUSIONS

While D2D variability is the dominant contributor to P_{leak} variations and WID variability presents a threat for delay sensitive applications, E_{dyn} is traditionally considered as weakly affected by variability. In this work, we prove for the first time

that E_{dyn} of combinatorial circuits is susceptible to WID variability due to glitch-induced variations of α_F at low voltage. Measured E_{dyn} variations are increased by a factor $5\times$ at 0.4V. The associated normalized standard deviation (σ/μ) of dynamic power is 5.6% and can no longer be neglected with respect to D2D variability of leakage power (8.9% measured). This work also shows that E_{dyn} variability in complex circuits cannot be modeled by ring oscillator structures whose α_F is equal to 1. Their E_{dyn} variations thus only exhibit the typical D2D capacitance fluctuations. With the increase of WID variability in nanometer CMOS technologies, we conclude that E_{dyn} variability should strongly be considered for statistical circuit simulations, as it might change design paradigms and affect circuit robustness at next technology nodes.

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