AN INTEGRATED CIRCUIT-BASED RADIOFREQUENCY-POWERED IMPLANTABLE TELEMETRY MICROSYSTEM FOR EMG RECORDING

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ABSTRACT—This paper presents an implantable telemetric microsystem for EMG recording purposes focusing on the development of an implant based on a hybrid circuit which includes a mixed-mode ASIC, designed specially for this application. In conjunction with another paper from this congress (Scholz, 1997), the development of a new radiofrequency-powered and bi-directional transcutaneous data link is presented.

INTRODUCTION

Implantable microsystems are currently of great interest in the biomedical research field. New microtechnologies permit development of sophisticated electronic systems with very good performance in terms of volume and power consumption. In conjunction with suitable isolation materials, reliable long-term implantable microsystems can be achieved. In this context the inclusion of wireless communication circuitry interfacing with the external world offers a wide range of advantages. The primary approach uses a wire connection, which brings with it many problems related to infections and mechanical breakages, especially for long-term applications. A telemetry system permits interaction on-line with the internal unit without any skin damage, increasing the health-level of the patient, who does not suffer any discomfort. In such systems, power becomes critical when long-term applications are required. There are two main approaches for solving this: (1) to use a battery (McCreesh, 1996) or (2) to radiofrequency power the microsystem inductively (Puers, 1995; Nardin, 1995). Battery problems related to life-time (change means surgical operation) and volume make the second option very attractive. The main applications of implantable microsystems are in recording biosignals (EMG, neural, etc.) or for stimulating muscles or nerves, using several types of electrode. The work presented here has been done in the framework of the ITUBR[1] project, which aims to develop an implantable device for telemetry of muscle signals in order to control an artificial prosthesis via electromyographic signals. Miniaturization of the system requires microelectronic technology. An integrated circuit (IC) containing telemetric and EMG recording circuits has been designed to join several passive elements in order to conform a totally implantable hybrid microsystem. In this paper an overview of the progress is presented dealing mainly with the telemetric circuit, which allows digital data to be transmitted bi-directionally at the same time as powering the implant by radiofrequency.

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[1] ITUBR: **I**mplantable **T**elemetry **U**nit for **B**iomedical **R**esearch is a #950917 INCO European project, led by the CNM (Barcelona) with CINVESTAV (Mexico), the UCL (Belgium), the CCC (Uruguay) and the ULA (Colombia) acting as partners.

METHODS

The ITUBR system is based on the following parts: (1) an internal unit consisting of a telemetric part (IC and coils, basically) and a recording part (sensor and IC) and (2) an external unit consisting of a telemetric part (receiver and transmitter) and a data acquisition unit controlled by a PC. In order to save area (not only silicon but especially PCB bonding area due to the reduction of the number of pads) a unique chip has been designed with the telemetric (TC) and conditioning (CC) circuitry. The following picture shows a diagram of the ITUBR system.

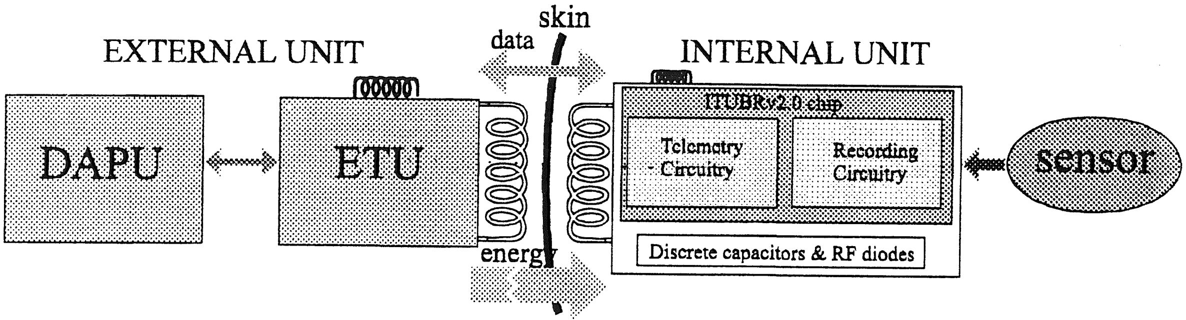

Fig. 1: ITUBR system block diagram

External Unit: the DAta Processing Unit (DAPU) is based on several programmable chips and a PC, interfacing between the user and the External Telemetric Unit (ETU). Currently in this version the connexion between DAPU and ETU is not by telemetry, but to give a reasonable level of portability this is something to be done in future. Thus power will become more critical (battery powered). The DAPU does all the data treatment (coding, decoding, data storage, etc.) and the ETU (which is close to the skin) only contains the minimum circuitry in order to reduce power consumption and size. This unit contains an RF power supply and data transmitter and a receiver. The transmitter is based on a Class E driver. This choice is due to its high efficiency (100% theoretically), its independence of power transistor drain-source capacitance and its ease of modulation if an ASK modulation is needed. The carrier frequency has been fixed at 10 MHz, higher than usual for powering, in order to reach a high data rate; lower frequencies would be preferred to avoid RF tissue absorption, to obtain more easily the optimum Class E operating point, as well as to decrease the frequency crosstalk with the on-chip transmitter carrier. The ETU also contains a 30 MHz Binary Phase Shift Keying receiver to pick up the data coming from the implant.

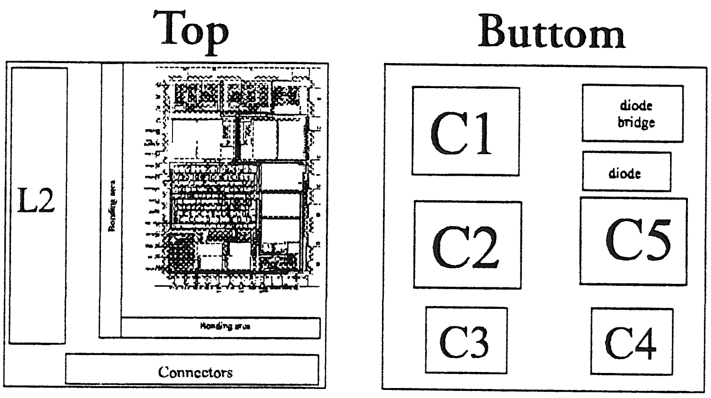

Fig. 2: Hybrid system PCB design

Internal Unit: First an overview of the microsystem will be given. A more detailed explanation on the ASIC development will follow.

Microsystem design: The implant is based on a hybrid system in which most of the circuits are integrated into an ASIC designed for the project. Additional passive SMD elements (large capacitors for fine regulation and RF diodes for rectifying) as well as the coils are required. Figure 2 shows a layout of the double-sided PCB circuit. Final area is expected to be close to 1cm^2. ASIC pads for testing purposes only (so not bonded to the PCB) are aligned on two sides to reduce the bonding area on the card. In 'Top' there is the chip, the transmitting magnetic-cored coil and the connec-tors to the electrodes. In 'Bottom' there is the rest of the SMD elements. The power coil can be fixed just over the board (within the Silastic package) or if cross-talk problems are important can be separated from the rest of the implant.

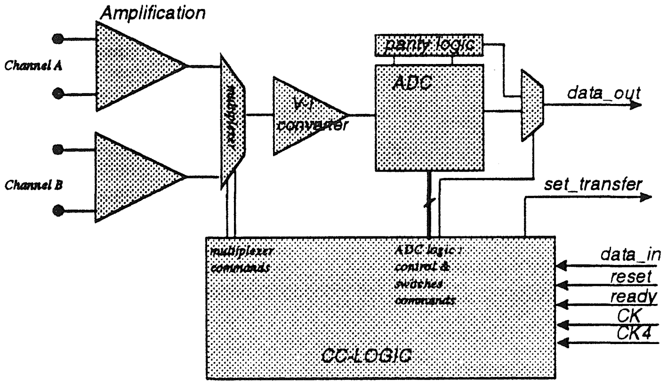

Fig. 3: Block diagram of the EMG circuitry.

ASIC design: Within the chip there are the telemetric and the application-specific parts. This paper focuses on the chip telemetry circuits. Nevertheless a brief explanation of the EMG recording circuitry follows.

The global scheme of the conditioning circuitry is given in Figure 3. The *amplification part* consists of two channels. Each channel amplifies and filters the differential signal from a pair of electrodes implanted in muscles. These two channels are selected by sending control data from outside the body to the control unit of the conditioning circuitry. It is possible to choose either one, two or no channels. As two channels can be selected, time-multiplexing must be performed. The A/D conversion is performed in current mode, so a previous voltage-to-current converter is required. A final logic stage sends the required lines to the telemetric circuit. The telemetric part is built of four main[2] blocks: (1) energy, (2) receiver, (3) transmitter, and (4) control unit.

-Energy block: RF Power is transmitted through an inductive link formed by two coupled coils (one external and the other implanted). The amount of power transmitted and its efficiency depend mainly on the coupling factor (k) between the coils, which depends on the geometry and orientation of the inductors. The IC receives a full-wave-rectified secondary voltage and through a line regulator provides the whole chip with the supply voltage and several current references. A zener-based pre-regulator with an output voltage centred near 11.7 V provides not only a fairly stable input voltage to the final regulation step but also acts as an useful high-voltage protector, permitting secondary voltages up to 50 V. Next there is the final bandgap-based regulator. Using several standard library elements of HBIMOS[3] technology, a very low load-sensitive 5 V regulator has been implemented. A high PSRR OpAmp supplies the 5 V to the whole circuitry. Two supply lines are required in order to obtain a voltage stable enough for the analog recording circuitry. An 8-bit A/D converter working at 5 V needs 20 mV maximum ripple on the supply, so a 5 V power line supplies this critical part and the rest of the chip is fed through another 5 V line. Additionally two current references at 100 μA and 12 μA are required for the CC circuitry. Using PNP and NPN mirrors, the telemetry supplies to the EMG circuit the following current sources: (1) one 5 V to the low 100 μA line, (2) one ground to the high 100 μA line, (3) two 5 V to the low 12 μA lines and (4) one ground to the high 12 μA line.

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[2] Also a power-on reset with a 5ms time constant has been designed. Details are not included in this paper.

[3] HBIMOS is an ALCATEL-MIETEC 2m BiCMOS technology supported by Europractice.

-Receiver: Amplitude Shift Keying (ASK) has been the choice for modulating the RF carrier, which at the same time powers the system. Thus an envelope detector is required to demodulate the signal. By filtering and Schmitt-triggering the single diode input, one can obtain the envelope of the AC-induced voltage. The design of this block has been done with careful attention to the wide variation of receiver induced voltages that can be achieved, and is thus able to demodulate for a reasonable range of modulation depths.

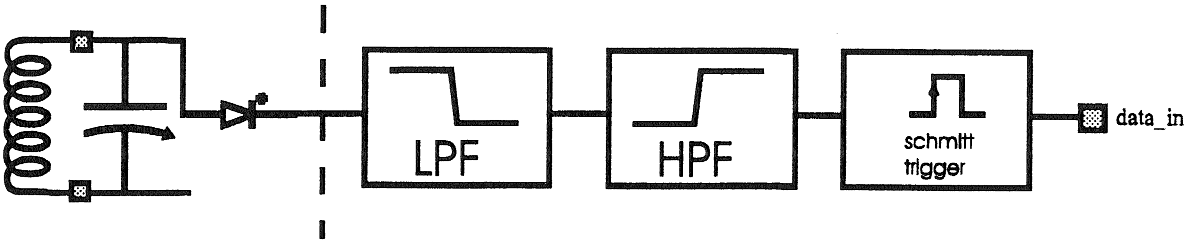

Fig. 4: ASK demodulator

-Transmitter block: The internal-to-external transmission is achieved by BPSK modulation (offering low sensibility to noise, easy modulation and not very difficult demodulation). Two dephased paths are commuted according to the modulator signal. Special efforts to reduce the relative path delay have been made in order to obtain a clear π change of phase. The on-chip RF generator is obtained through a Class-B driver in a resonant parallel LC tuned circuit shown in Figure 5.

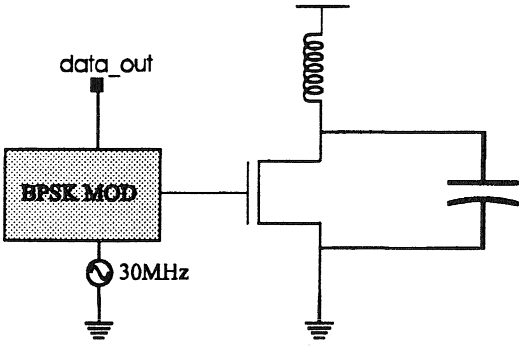

Fig. 5: On-chip driver

The inductor is external but the capacitor is integrated, with a value of 12 pF. The RF electromagnetic-wave magnitude depends directly on the peak current through the coil. This value is a function of (1) the quality factor Q of the coil, (2) the voltage dropped through the LC and (3) the geometry of the current source transistor. By fixing the LC voltage at 5 V and considering a serial coil resistance near 50 Ω at 30 MHz, one can obtain the relationship between transistor geometry and the peak current through the coil. Two bits program the coil current. The four chosen values are depicted in the following table.

(bit7, bit8)	**NMOS size**	**Coil current (pp)**	**Efficiency (I_{coil}/I_{vdd})**
0,0	10 u/6 u	4.3 mA	14
0,1	20 u/6 u	8,5 mA	17
1,0	40 u/6 u	13,9 mA	18
1,1	80 u/6 u	17,9 mA	17

The on-chip 30 MHz generator is produced by a seven-stage resettable CMOS ring oscillator. Although this configuration cannot assure a very stable frequency the system is not very sensitive to small variations in the base-clock. As the communication is asynchronous and the quality factor of the transmitter is not extremely high, the use of a quartz crystal seemed unnecessary.

-Control Unit block: Data flow is mainly from internal to external. The communication protocol behaves as shown in Figure 6. The internal unit stands-by until it receives an asynchronous reset signal; it then decodes the next incoming eight bits, sends them as an

echo frame and afterwards starts to send indefinitely the recorded data, including a synchro-nizing byte every 8 bytes. According to the established protocol, this unit will provide to CC (1) the input data properly decoded, (2) the reset signal, (3) the base-clock, (4) a four times faster clock, and finally (5) a ready signal for starting the AD conversion. In its turn the CC will send (1) the digitized recorded data for sending to the outside and (2) the synchro-frame time-interval. Owing to its complexity the semi-custom design has been carried out without using any synthesis tool. Logic simulation has been implemented through Verilog. The main modules of the control unit will now be described.

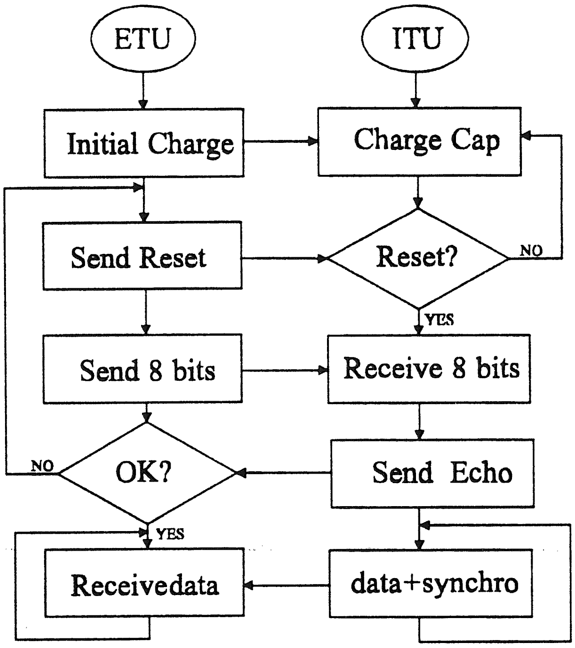

Fig 6: Protocol

i) Decoder: this circuit decodes the incoming envelope-detected data according to the following coding criteria: Return-to-zero pulse width modulation has been chosen. Using several 3.75 MHz clocked counters one can detect if a '0' a '1' or a reset-init signal is received. Data is updated on every negative edge of the demodulated line.

ii) Synchro adapter: this circuit converts the incoming ETU clocked data to digital data synchronized with the internal on-chip oscillator using a serial-parallel load.

iii) Clock generator: the entire internal unit is synchronized by a signal generated internally. The basic synchro signal is the same 30 MHz carrier frequency. For providing the required clock signals to the whole circuit, a six-stage clock divider has been designed, generating the 2-submultiples of 30 MHz down to 234 kHz.

iv) Coder: this circuit takes the digitized recorded data, encodes it and sends it to the BPSK modulator, including the synchro frame. The bit rate can be programmed at 468 kHz or 234 kHz.

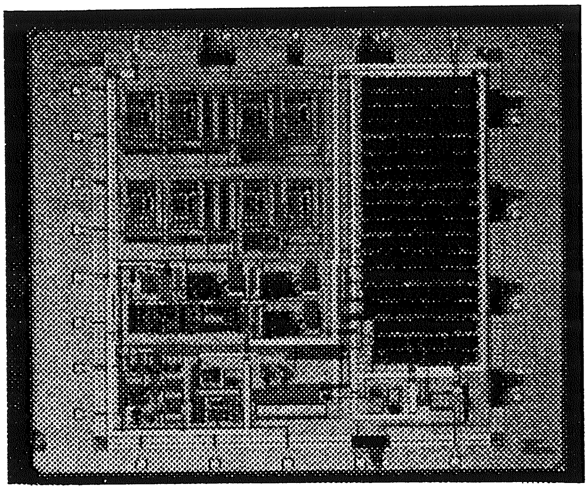

Fig. 7: ASIC microphotograph

Top Design. The final chip design (including the EMG circuit) was completed with 22 bondpads. The final chip area is about 30 mm^2.

RESULTS

Figure 7 shows the ASIC already fabricated and tested. The overall con-sumption of the chip is about 4.5 mA, but de-pends on the induced secondary voltage: the higher the input voltage the higher the current consumption in the regulator. With an internal power coil of 10 mm diameter and using an external coil of 20 mm we are able to power the chip up to 15 mm with no misalignment. This is enough to meet our application requirements (distances down to

10 mm). Through the bandgap regulator this chip gives an analog voltage supply of 4.97 V and a digital supply of 4.99 V. DC input voltage sensitivity is very low (less than 1 mV per Volt).

In relation to the data trans-mission, the InLink (data coming to the inside) has been successfully achieved. Figure 8 shows the oscilloscope wave-form when sending a '11000100' frame to the implant at the same time as the system was powered by RF and with up to 15 mm of ETU-ITU distance. *Line_1* is the reset and the data for the EMG part: *line_2* is the data line once demodulated and decoded; *data_out* is the line which modulates the 30 MHz to be sent to the outside. Once the data comes in there is an echo transmission to the ETU. The implant then starts to send recorded data including a synchro byte every eight bytes.

The OutLink transmission has a problem related to the BPSK modulation, which does not allow a 30 MHz carrier frequency to be used. As a consequence, *data_out* is the output of the modulator, which is the gate voltage of the NMOS driver. Every transition of this voltage defines a self-oscillation of the LC circuit that can be detected in the external receiver. Communication up to 10 mm has been achieved in this way and is shown in Figure 9. On the left there is the internal coil current and on the right appears the received voltage in the external unit. Every transition in the data_out means a peak in the external received voltage. Due to the same 30 MHz problem all the internal clocks have been divided by a factor of two so that the InLink bit rate is 120 kbps and the OutLink bit rate can be programmed at 117 kbs or 234 kbps.

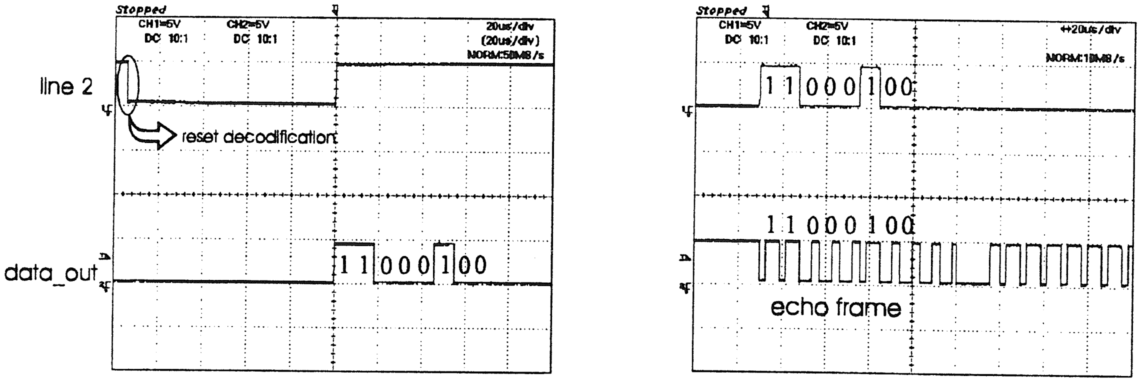

Fig 8: Oscilloscope waveforms for InLink communication

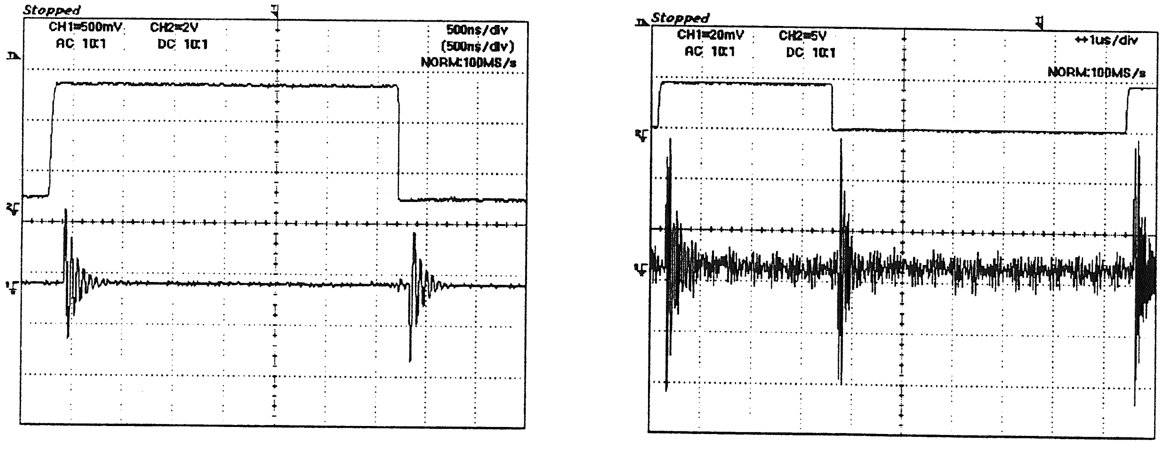

Fig.9: Oscilloscope waveforms for OutLink communication

DISCUSSION

Based on the results presented here, a new chip has already been designed and now is currently in the fabrication stage. This chip includes a new improved modulator which is programmable to several carrier frequencies (going from 20 MHz to 40 MHz) and an additional oscillator to provide the internal clock. Also it is possible to use the technique of transmitting a burst of signals using the self-oscillation transitory current on the LC. Despite a very poor S/N ratio this option has the advantage of a very low power consumption in the transmitter. A substancial effort will be made in future to increase the bit-rate (up to 1 Mbps) and to improve the efficiency of power transference through the use of close-loop control of the induced secondary voltage.

CONCLUSION

This paper has presented the work done within the ITUBR project to develop the implantable telemetric device. A first prototype containing an ASIC with telemetry and recording circuitry has been set up. Data and power transference from the external unit has been successfully achieved in the application range. Despite a problem detected in the on-chip modulator, data transmission from the implant has also been accomplished, but the bit rate was reduced by a factor of two. A new chip correcting the detected problems has been already designed and is currently in fabrication.

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