understand this important fact because the makers of battery powered products generally do not inform the purchaser of the amount of power the product consumes and the manufacturers of disposable batteries (primary cells) do not tell the purchaser how much energy their batteries contain.

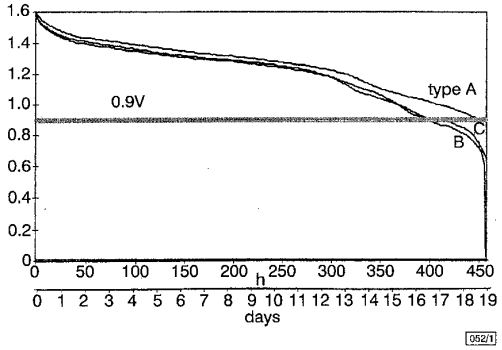

Fig. 1 *Discharge test with constant current of 20 mA for three makes of battery (A, B, C)*

The energy content of three internationally known brands of C-size alkaline cells have been measured to establish the cost of battery power. A radio might typically use four cells in series to give a supply of 6V with a power demand of 120mW, corresponding to a 20mA discharge rate. Fig. 1 shows the results of the three makes of cell being discharged at at this rate. If it is assumed that the radio will continue to function until the cell voltage has fallen to 0.9V, it can be seen that 400h of continuous operation can be obtained from a set of batteries, whatever the make. Analysis of the results shows that each cell contributes approximately 36,000J. The purchase price of a single 1.5V C-type alkaline cell is approximately £1.75 in the UK. The cost of operating the four-battery radio is therefore £0.0175p/h.

The importance of reducing the power demand of battery powered products is illustrated by the following calculation. The typical purchase price for a medium quality radio is ~ £20 in the UK. If the radio is operated for 10h a day, every day, the yearly battery cost is £63.88. If the radio is owned for five years the total battery cost would be approximately £319, so that the initial purchase price would be only ~ 6% of the total ownership cost. It is therefore important that the power consumption of radios should be drastically reduced. The present typical power demand of 120mW can easily be reduced to 5mW [1] and any small increase in purchase cost required to achieve this is likely to be a negligible proportion of the total ownership cost. Labelling battery powered equipment to show its rate of battery usage and labelling of primary batteries to show their energy content would enable consumers to calculate the total ownership cost of these products.

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Two-quadrant CMOS analogue divider

C. Dualibe, M. Verleysen and P. Jespers

A novel circuit performing the division operation is proposed. The numerator and denominator input data are currents whereas the output quotient is a voltage. The circuit was designed to be used in the defuzzifier of a fuzzy controller.

Introduction: Recently, the use of analogue current-mode circuits for signal processing has grown considerably [1, 3, 4]. One asset of these circuits is their ability to cope with low supply voltages. The need for current-to-voltage or voltage-to-current converters, however, offsets this advantage to some extent and makes circuits generally more complex while affecting accuracy. Therefore, circuits which combine the two modes naturally offer interesting alternatives.

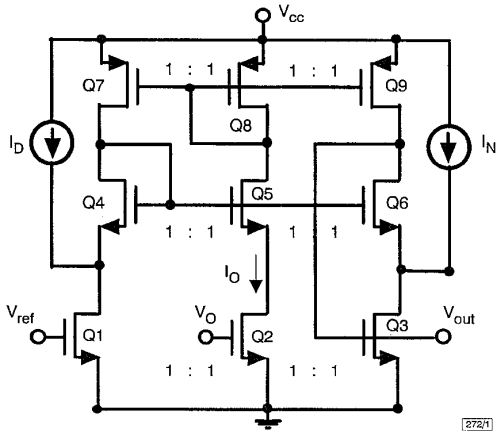

Fig. 1 *Current-input/voltage-output two quadrant divider*

Circuit description: In the simplified schematic drawing of the divider shown in Fig. 1, the numerator and denominator are two currents, called, respectively, I_N and I_D. The output is the gate voltage of transistor Q3. The circuit comprises three layers of transistors. The lowest one performs the actual division operation. All common source transistors (Q1–3) have the same size and are supposed to operate in the triode region. The middle layer consists of two source followers Q5 and Q6, controlled by the diode-connected transistor Q4, which replicates the drain voltage V_{ds} of Q1 at the drains of Q2 and Q3. Finally, the upper layer is a current mirror mirroring the drain current of the centre transistor Q2 into the drains of Q1 and Q3.

The principle of the divider is described in the following, considering transistors Q1 and Q2 first. With the drain current of Q1 being equal to the sum of I_D and the mirrored drain current of Q2, we have

$$I_D + I_o = \beta\left((V_{ref} - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (1)$$

where

$$I_o = \beta\left((V_o - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (2)$$

Hence

$$I_D = \beta(V_{ref} - V_o)V_{ds} \quad (3)$$

Now consider transistor Q3. Since its drain current is equal to the sum of I_N and I_o, its gate voltage V_{out} must adjust itself to satisfy the expression

$$I_N + I_o = \beta\left((V_{out} - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (4)$$

Hence, similarly to eqn. 3,

$$I_N = \beta(V_{out} - V_o)V_{ds} \quad (5)$$

and thus

$$V_{out} - V_o = (V_{ref} - V_o)\frac{I_N}{I_D} \quad (6)$$

Thus if V_{out} is referred to V_o, a two-quadrant divider is obtained. Note that the gate voltage of Q3 being connected to a high impedance node, the loop gain controlling the output voltage can be very large, while the output impedance is very large.

Accuracy considerations: Since the currents in Q4–9 are all identical, the drain voltages of the lower transistor layer are affected by transistor mismatches only. Therefore they can be kept within reasonable tolerances. Furthermore, as in any translinear network,

the mobility variations among Q1–3 introduce current imbalances. Moreover, the simple quadratic expressions of the drain currents do not introduce the moderate inversion mode of operation as well as the threshold voltage variations which go along with changes of the gate voltage.

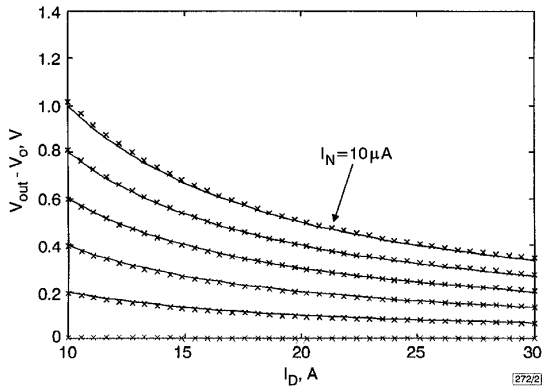

Fig. 2 *V_{out}-V_o against I_D for I_N from 0 to 10μA in 2μA steps*

——— calculated
× measured

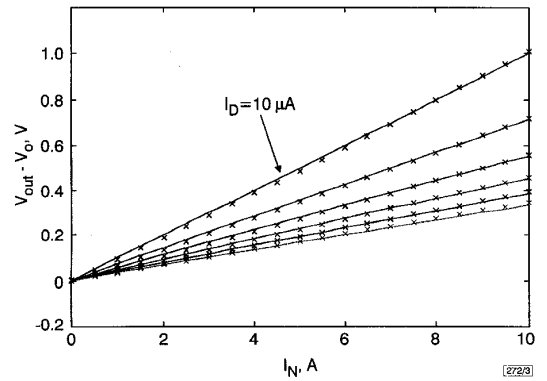

Fig. 3 *V_{out}-V_o against I_N for I_D from 10 to 30μA in 4μA steps*

——— calculated
× measured

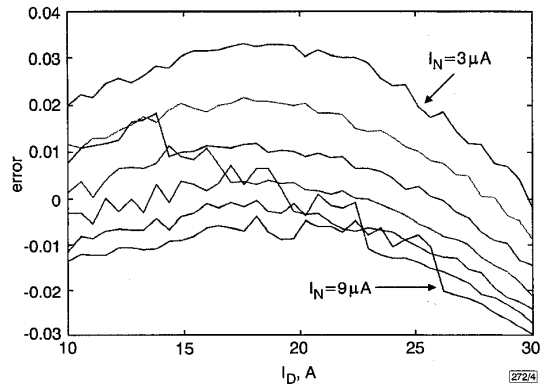

Fig. 4 *Relative error on (V_{out}-V_o) against I_D for I_N from 3 to 9μA in 1μA steps*

Experimental results: The proposed circuit was simulated with HSPICE and fabricated in a 2.4μm N-well CMOS technology with V_{cc} = 5V, I_N and $I_D \leq 30\mu A$, $I_N/I_D \leq 1$ and the output range $0 < (V_{out}-V_o) < 1V$. V_{ref} and V_o were set to 2.7 and 1.7V, respectively. The transistor sizes are (*W/L*) 1, 2, 3 = 8/8μm; (*W/L*) 4, 5, 6 = 15/6.4μm and (*W/L*) 7, 8, 9 = 22/3μm. In the actual implementation, the last three transistors were replaced by an enhanced Wilson current mirror whose higher output impedance improves accuracy for the gain increase at the output node.

The curves in Fig. 2 show (V_{out}-V_o) against I_D while I_N is held constant. In Fig. 3 the parameter is I_D while the curves reflect (V_{out}-V_o) against I_N. In both cases, measured and calculated data are displayed together. The measured relative error shown in Fig. 4 rises to ±3%. This is mainly due to mismatch produced by mobility reduction (in our case $\theta = 0.04\ V^{-1}$). The output offset (when $I_N = 0$) was also measured for different values of I_D and it is < 1.6mV in all cases.

Conclusion: The proposed divider fulfils the requirements for current-mode fuzzy controllers. The circuit shows the robustness, simplicity and acceptable precision useful for such applications.

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Circularly polarised printed antenna with conical beam

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A new circularly polarised printed antenna concept with conical beam is presented. The proposed concept describes a simple printed structure with an omnidirectional pattern and maximum gain of ~ 6dBi at elevation angles between 30° and 60°, with features suitable for various commercial applications. The voltage standing wave ratio is < 1.3 and the axial ratio is < 2dB in the 3% operational bandwidth around 4.6GHz. The experimental results show good agreement with those obtained by simulation.

Introduction: Circularly polarised antennas are particularly interesting for communication scenarios where line of sight (LOS) propagation is planned. Typical applications vary from satellite-Earth communication, via indoor LOS wireless LANs, to outdoor LOS private links. Apart from there being no need for antenna orientation, the special advantage of circularly polarised antennas is the additional physical attenuation of reflected waves (due to changing polarisation direction) which improves the propagation channel and makes the overall system more resistant in the case of multipath propagation. This advantage appears mainly if an LOS path exists. There are two major application areas where circularly polarised antennas with conical antenna characteristics are required: