DESIGN OF A RF POWERED MIXED-MODE IMPLANTABLE IC FOR A WIRELESS EMG RECORDING PURPOSE

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ABSTRACT. This paper presents the design of an implantable mixed-mode chip for EMG recording purposes which contains telemetric circuits for a wireless bi-directional communication with an external-outdermal unit. Moreover the chip contains additional circuitry permitting to power by RF the internal microsystem through an inductive transcutaneous link.

INTRODUCTION. Implantable microsystems are nowadays of great interest in the biomedical research field. New microtechnologies permit to develop sophisticated electronic systems with very good performances in volume and power consumption [Ziai93] [Fern92]. In conjunction with useful isolation materials, reliable long-term implantable microsystems can be achieved. On that point the inclusion of a wireless communication circuitry interfacing with the external world offers a wide range of advantages. The primary approach uses a wire connection which carries many problems related to infections and mechanical breakages specially for long-term applications. A telemetry system permits to interact on-line with the internal unit without any skin damage, increasing the health-level of the patient which don't suffer of any discomfort. In such systems, power becomes critical when long-term applications are required. There are two main approaches for solving this: (1) to use a battery [Fang93] [McC96] [Beta96] or (2) to RF power the microsystem [Tang95] [Puer95] [Nard95]. Battery problems related to its life-time (change means surgical operation) and its volume make the second, less known option, very attractive. Main applications of implantable microsystems are centered in recording biosignals (EMG, neural, ...) or for stimulating not only muscles but also nerves, using several types of electrodes. The work here presented has been done in the framework of the ITUBR[1] project, which aims to develop an implantable device for telemeter muscle signals in order to control an artificial prosthesis via electromyographic signals. Miniaturization of the system requires microelectronics technologies. An integrated circuit containing telemetric and EMG recording circuits has been designed to join several passive elements in order to conform a hybrid microsystem totally implantable. Thus in this paper an overview of the chip design is presented.

SYSTEM OVERVIEW. The ITUBR system is based on the following parts: (1) an internal unit formed by a telemetric part (IC and coils basically) and a recording part (sensor and IC) and (2) and external unit formed by a telemetric part (receiver and transmitter) and a data acquisition unit controlled by a PC. In order to save area (not silicon but specially PCB

[1] ITUBR: **I**mplantable **T**elemetry **U**nit for **B**iomedical **R**esearch is a #950917 INCO european project, leadered by the CNM (Barcelona) and acting as partners the CINVESTAV (Mexico), the UCL (Belgique), the CCC (Uruguay) and the ULA (Colombia).

bonding area) a unique chip (named ITUBRv2.0) has been designed with the telemetric (TC) and conditioning (CC) circuitry.

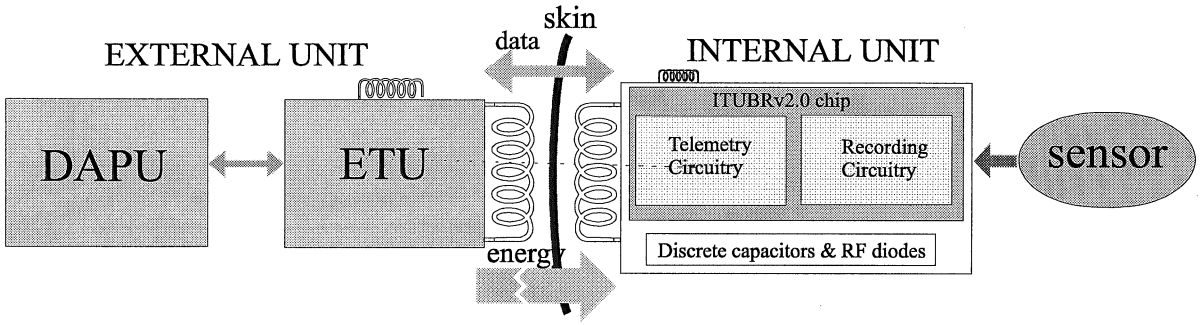

Figure 1. ITUBR system block diagram

TELEMETRY CIRCUITS. The telemetric part is build on four main[2] blocks: (1) energy, (2) receiver, (3) transmitter and (4) control unit.

Energy block

RF Power is transmitted through an inductive link formed by two coupled coils (one external and the other implanted). The amount of power transmitted and its efficiency depend mainly on the coupling factor (k) between both coils, which depend on the geometry's and orientation of the inductors. The IC receives a full-rectified secondary voltage and through a line regulator provides to the whole chip the supply voltage and several current references. Figure 2 shows an schematic representation of this unit.

-Voltage sources: A zener-based pre-regulator with an output voltage centered near 11.7V provides not only a pretty-stable input voltage to the final regulation step but also acts as an useful high-voltage protector, permitting secondary voltages up to 50V. Next there's the final bandgap-based regulator. Using several standard library elements of the HBIMOS[3] technology a very low load-sensitive 5V regulator has been implemented. A high PSRR OpAmp supplies to the whole circuitry the 5V. Two supply lines are required in order to obtain a stable enough voltage for the analog recording circuitry. A 8 bits A/D converter working at 5V needs a 20mV maximum ripple of the supply. So a 5V power line supplies this critical part and the rest of the chip is feeded through another 5V line. There is also another line which gives a voltage reference of 2.5V for biasing the recording site.

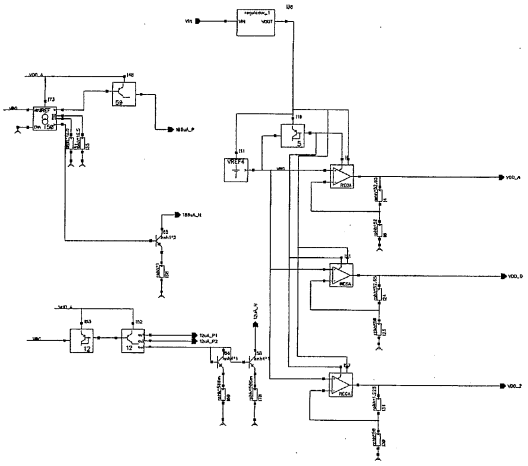

Figure 2. Energy block schematic

The 5V voltage regulator (including the two steps) has already been experimentally tested [Int96] with the ITUBRv1.0 test chip showing good results. Minimum dropping voltage was about 2.1V.

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[2] Also a power-on reset with a 5µs time constant has been designed. No details on this paper.

[3] HBIMOS is an ALCATEL-MIETEC 2µ BiCMOS technology supported by Europractice

-Current sources: Two current references at 100μA and 12μA are required for the CC circuitry. This has been achieved using two elements of the standard analog circuitry. Using PNP and NPN mirrors the TC supplies to CC the following current sources: (1) one 5V to down 100μA line, (2) one ground to up 100μA line, (3) two 5V to down 12μA lines and (4) one ground to up 12μA line.

Receiver block

Amplitude Shift Keying (ASK) has been the choice for modulating the RF carrier which at the same time powers the system. Thus an envelop detector is required to demodulate the signal. Filtering and schmid-triggering the single diode input, one can obtain the envelop of the ac induced voltage. Figure 3 depicts in a transistor level the design of this circuit.

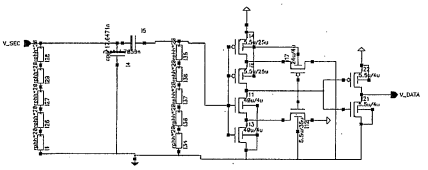

Fig.3 ASK demodulator

Again this detector has been fabricated and tested with good results in the ITUBRv1.0 previous test chip [Int96]. Up to now, this circuit in conjunction with the 10MHz ETU is able to achieve good performances up to 250 kbps in a wide range of modulation depths.

Transmitter block

The internal-to-external transmission is achieved by BPSK modulation (due to low sensibility to noise, easy modulation and not very difficult demodulation). Two dephased paths are commuted according to the modulator signal. Special effort on reducing the relative path delay has been done in order to obtain a clear π change of phase. The on-chip RF generator is obtained through a Class-C driver in a resonant parallel LC tunned circuit showed in figure 4.

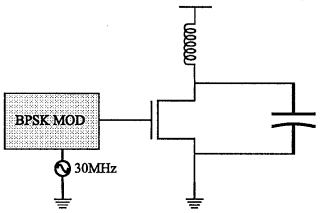

Figure 4. On-chip driver

The inductor is external but the capacitor is integrated with a value of 12pF.

The RF electromagnetic-wave magnitude depends directly on the peak current through the coil. This value is a function of (1) the quality factor Q of the coil, (2) the dropping voltage through the LC and (3) the geometry of the current source transistor. Fixed the LC dropping voltage at 5V and considering a serial coil resistance near 50Ω's at 30MHz, one can obtain the relation between transistor geometry and the peak current through the coil. Two bits program the coil current. The four chosen values are depicted in next table.

(bit7, bit8)	NMOS size	Coil current (pp)	Eficiency (I_{coil}/I_{vdd})
0,0	10u/6u	4.3mA	14
0,1	20u/6u	8,5mA	17
1,0	40u/6u	13,9mA	18
1,1	80u/6u	17,9mA	17

Control Unit block

Data flow is mainly from the internal to the external. The communication protocol behaves as follows in next diagram: the internal unit stands by up to receiving an asynchronous reset signal; then decodifies the next incoming eight bits, send them as an echo frame and afterwards starts to send indefinitely the recorded data including every 8 bytes a synchro byte. According to the established protocol [Itub96] this unit will provide to CC (1) the input data properly decodified, (2) the reset signal, (3) the base-clock , (4) a four times faster clock and finally (5) a ready signal for starting the AD conversion. In it's turn the CC will send (1) the digitized recorded data for being sended to the outside and (2) the synchro-frame time-interval. Due to its reasonable complexity the semi-custom design has been carried out without using any synthesis tool. Logic simulation have been implemented through Verilog. Next follows the main modules of the control unit:

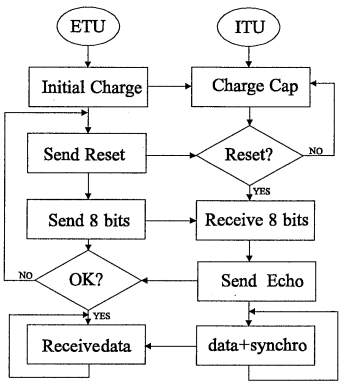

Fig 5. Protocol

i) Decoder: this circuit decodifies the incoming envelop detected data according to the following codification criteria:

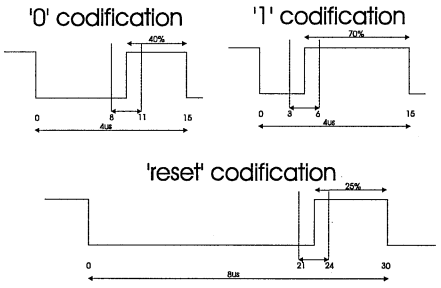

Fig. 6. Receiver codifications

A return-to-zero pulse with modulation has been chosen. Using several 3.75MHz clocked counters on can derive if comes a '0' a '1' or a reset-init signal. Data is updated every negative edge of the demodulated line.

ii) Synchro adapter: this circuit converts the incoming ETU clocked data to a digital data synchronized with the internal on-chip oscillator using a serial-parallel load.

iii) Clock generator: all the internal unit is synchronized by a signal generated internally. The basic synchro signal is a 30 MHz wave, produced by a seven-stages resetable CMOS ring oscillator. This frequency will be the ITU to ETU transmission carrier. A slightly lower frequency oscillator has been already designed, fabricated and tested with good results. For providing the required clock signals to the whole circuit, a six-stages clock divider has been designed, hence obtaining the 2-submultiples of 30MHz down to 234kHz.

iv) This circuit takes the digitized recorded data, codifies it according to the following codification scheme (figure 7) and send it to the BPSK modulator, including the synchro frame. The bit rate can be programmed at 468kHz or 234kHz.

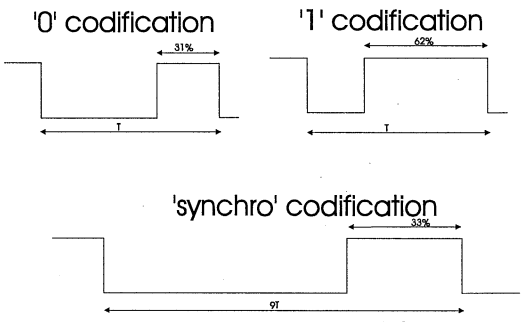

Figure 7. Transmitter codifications

EMG RECORDING CIRCUITS. The global scheme of the conditioning circuitry is given below at figure 8. The *amplification part* consists of two channels. Each channel amplifies and filters the differential signal from a pair of electrodes implanted in muscles. These two channels are selected by sending control data from outside the body to the control unit of the conditioning circuitry. Choosing either one, two or no channels is possible. As the two channels can be selected, a time-multiplexing must be performed. The A/D conversion is performed in current mode, thus a previous VI converter is required. A final logic stage sends the required lines to the telemetric circuit.

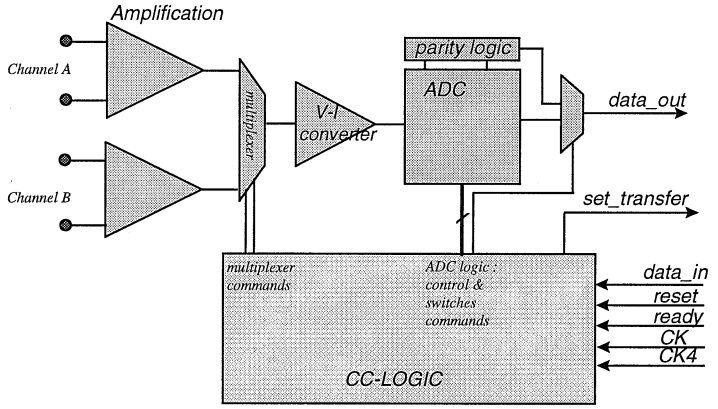

Figure 8.Global scheme of the conditional circuitry.

Amplifier stage

The system architecture must fit the following requirements:

Differential input signal	-1.5mV to 1.5mV
Signal bandwidth	0.3Hz to 10KHz
Differential dc component	-50mV to 50mV
Maximum input noise	11.7uV

Figure 9 shows the amplification scheme chosen.

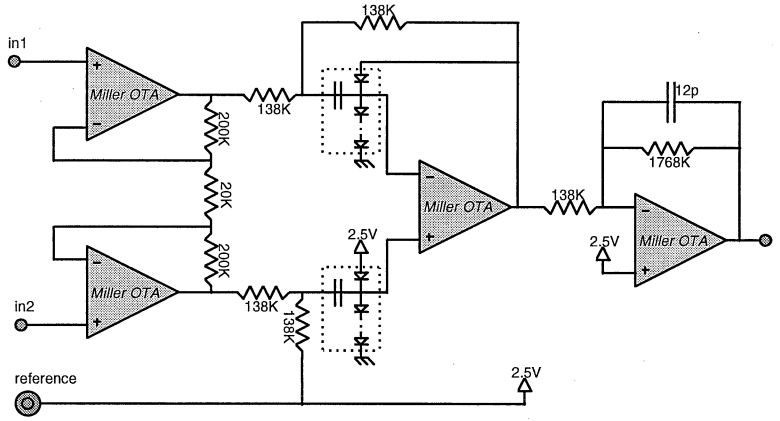

Figure 9. Amplification circuitry.

This circuit consists of three main parts. The first one is a classical instrumentation pre-amplifier, offering an extremely high input impedance. The second part has three goals: to

high-pass filtering the signal, eliminating all frequencies below 1Hz and also the dc component of the signal; to convert the differential signal to single-ended mode; and to eliminate the common-mode signal. The last part is a common inverting-mode amplifier which amplifies the signal to the needed level and also filters all frequencies above 7.5kHz. The high-pass filter uses a special design based on diodes, which is needed to reach the required very low cut-off frequency (around 1 Hertz).
The same operational amplifier is used for each part of the circuit, it is a Miller OTA, an operational transconductance amplifier. It was chosen due some advantages versus the normal OPA: (1) Class A output stage : high linearity, (2) low-consumption and (3) easy design. OTA configurations as simple, folded and cascoded are not to be chosen for two reasons. On one hand, output impedance is so high that, loaded with the retroaction resistors, the cascode effect is destroyed (load and output impedance are in parallel). On the other hand, cascode mode reduces output dynamic. And, finally, simple OTA configuration is not sufficient to have convenient gain. The Miller configuration was chosen between other ones because it meets the requirement of convenient high gain, and a low output impedance. Dimensioning this amplifier was made by taking into account: distortion, noise reduction, low consumption, gain, stability and occupied surface on the integrated circuit. All values and parameters and a wide range of possible lengths were examined. The complete dimensioning was made in MATLAB™.As explained before, the differential signal at the electrodes presents a dc component ranging from +50mV to -50mV. It's thus necessary to filter this undesirable part. The solution of filtering the signal directly at the input before amplification was not taken : in that case, the noise of the filtering circuit is injected in the beginning of the amplification chain, and this considerably degrades the signal-to-noise ratio. That's why a pre-amplification is made before filtering the signal. So, as we the S/N ratio is mainly due to the first stage of amplification, the noise keeps an acceptable value.
Final amplification stage characteristics follows:

Overall fixed gain	49 dB
Total circuit input noise	9.3μV
Amplification band	0.8Hz - 7.5kHz
Overall consumption	740μW

Multiplexer stage
This multiplexer is used to select one of the two channels for recording. Special attention was paid to the design to ensure high isolation between channels. Switches are implemented using CMOS switches. To improve isolation between the two channels, the signal from the channel not selected is connected to the ground using a CMOS switch, and shortening of the site which is connected to the other output channel is prevented using a third switch.

V/I stage
The circuit consists of a Miller OTA, already used for the amplification part, one resistor and a current mirror made of pnp transistors. As the gain of the Miller OTA is great (80dB), good linearity is obtained. The input voltage is directly reported to the resistor node, producing a current proportional to the voltage, $I=Vin/R$; this current, minus the reference current, is

doubled by means of a current mirror. So the relation $I_{out} = 2\left(\frac{V_{in}}{R} - I_{ref}\right)$ is performed. As the input voltage ranges from 2.1V to 2.9V, the output current ranges from 10μA to 90μA.

A/D converter stage

The chosen technique for this application is the current-mode algorithmic analog-to-digital conversion. This technique takes advantage of relatively simple hardware to produce ADC of good resolution. An algorithmic conversion is performed as shown in the figure 10 below. The input signal, Iin, is first doubled to create 2Iin. The new signal, 2Iin is then compared with the reference (100μA). If 2Iin is less than the reference, the digital output is set to zero and 2Iin becomes the new Iin. If 2Iin exceeds the reference, the digital output is set to one. For this case, the reference is then subtracted from 2Iin to create the new Iin. This process is repeated as many times as necessary to obtain the desired resolution.

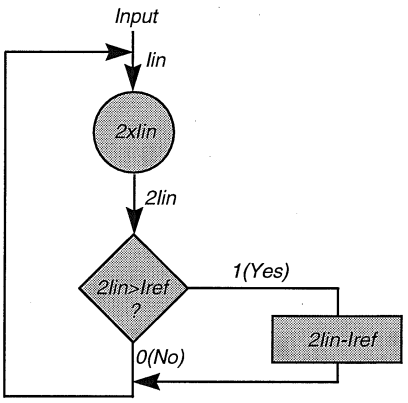

Figure 10. ADC algorithm

Figure 11 shows the implementation chosen. To perform an algorithmic conversion, the converter's switches are controlled by a logic circuitry. The clock sequence is essentially the same for each bit conversion except during the acquisition of the input signal for the conversion of the most significant bit. The conversion of the most significant bit is initiated by closing switches S1, S2 and S3, causing the current in the copier cell N1 to be set to Iin. The copier cell memorises the current by means of a capacitor. Once the current is memorised, S2 and S3 are opened while S4 and S5 are closed to set the current in N2 to Iin. Then by opening S1 and S5 and by closing S2, S4, S6 and S7, the current stored in N1 and N2 is summed, generating a current equal to 2Iin, -and that's the great advantage of the circuit- without the need of well matched devices. The resulting current is loaded in P1. Once P1 is set, S2, S4, and S7 are opened while S6 and S8 are closed, thus allowing the comparator to sense the current imbalance and hence determine if the signal, 2Iin, is greater than the reference, Iref. If the signal exceeds the reference, the output for the MSB will be '1' otherwise it will be '0'. This completes the conversion of the MSB. The remaining 7 bits are then converted in the following manner. The signal, which is now stored in P1, is loaded into N1 by closing S6, S2, and S3. If the output of the preceding bit was a '1', S8 is also closed to subtract the reference from the signal. If the output is '0', S8 is opened so that the signal remains unchanged. Once N1 is set, N2 is then set by closing appropriate switches. The signal is then doubled and compared with the reference. This sequence is repeated until the 8-bits resolution is achieved.

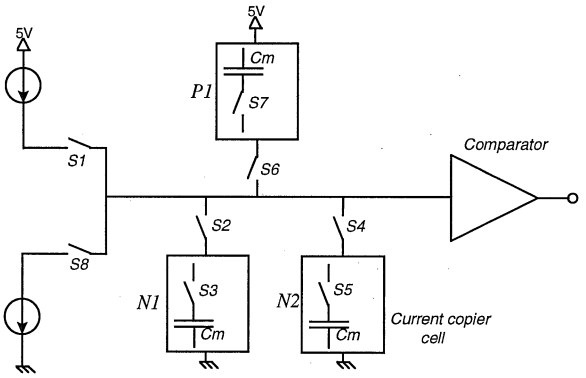

Figure 11. ADC implementation

TOP DESIGN. The final chip design was completed with 22 bondpads as we see in figure 12 where a layout print is showed. The final chip area is 26,2 mm^2.

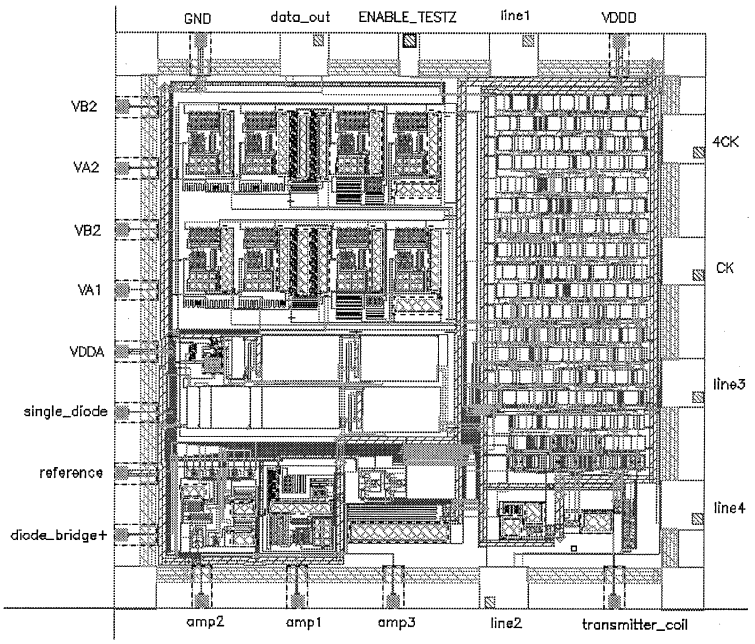

Figure 12. Layout of ITUBRv2.0 chip

DFWII of CADENCE has been the Cadtool used for the design. The Placement has been achieved in a semi-automatic way. The macroCells and pads placement has been done manually to optimize routing. The standardCells regions have been splitted in two: one for the fast logic circuitry (30MHz) and the other for the rest. The reason of this splitting is due to minimize the line capacitances of the fast circuitry because HBIMOS technology only guaranties a maximum frequency of 20MHz for the standardCells. The simulation of the 30MHz critical part has been done electrically, not logically. The routing has been implemented completely in an automatic way..

CONCLUSIONS. A new chip including Telemetry and Conditioning circuitry has been designed for a high bit-rate, batteryless implantable telemetry system which monitors EMG signals. Compactness due to the use of an ASIC will permit to obtain an implantable package non-exceeding $1cm^3$. Chip performances are expected to be available for the Iberchip Workshop. It is important to point out that the system architecture has been designed to permit an easy adaptation to several recording purposes: only the Conditioning Circuitry must be re-designed depending on the application, thus the telemetry system remain independent on the particular activity. This work shows the increasing interest of the biomedical instrumentation field in using microelectronics for implantable devices. The IC here presented is a product obtained within an european funded project (ITUBR) which involves latin-american and

european research institutes and a company. This project was set up taking profit of MicroMed[4].

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[4] MicroMed is a network on microelectronics medical applications funded by CYTED