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# A LARGE VLSI HOPFIELD NETWORK FOR PATTERN RECOGNITION PROBLEMS.

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Several designs have been proposed in recent papers ([1], [2]) to implement VLSI Hopfield neural networks. The first realized networks were just resistor coupling nets by analogy with theoretical models in which synapses are represented by resistors whose values determine the strength of the connection. In order to allow positive and negative values for the connections, the neurons are designed to have complementary (i.e. inverting and non inverting) outputs to which resistors can be connected. Although this circuit corresponds exactly to the Hopfield model, it does not allow changes in the resistor values. Another important problem comes from the difficulty to design large regular arrays of multi-valued resistive elements in VLSI technology.

Most recent implementations use an architecture more adapted to VLSI design. In such circuits, each synapse is an active element which sources or sinks current to the input line of the connected neuron (fig.1). The problem is the required matching between the P-type and N-type current sources, which is difficult to obtain because of the mobility differences between the two types of charges. Since the errors due to this non ideal matching are summed when increasing the number of synapses, the size of the network is very strongly limited. This is incompatible with pattern recognition problems wherein a large number of neurons is needed.

In our solution, sourced and sunk currents are summed separately on two different lines ($I^+$ and $I^-$) making irrelevant the problem of matching between excitatory and inhibitory connections. Each synapse sources or sinks current according to the result of a XOR function between the connected neuron output value and the sign of the connection weight (the connection weight is a two-bit value allowing the connection to be excitatory, inhibitory or non existent) (fig.2). In order to sum the different currents correctly, the conductances of transistors T1 and T2 have to be independent of the number of synapses connected to the lines $I^+$ and $I^-$. The voltages V+ and V- have thus to be fixed; this is obtained by means of a negative feedback loop (fig.3) allowing each synapse to sink the same current independently from the number of other synapses already connected to the same line (without feedback, the individual synaptic current would decrease when increasing the number of active synapses). Finally, the global excitatory and inhibitory currents are compared in a two stage high-gain current reflector which produces a logic output voltage (0 or 5 V) which is the neuron output value. This voltage is then fed back into the circuit.

This circuit allows the implementation of a large number of neurons on a single chip.

[1] Howard R. & al. An associative memory based on an electronic neural network architecture, IEEE transactions on electron device, July 1987.

[2] Graf H., De Vegvar P. A CMOS associative memory chip based on neural networks, ISSCC 1987.

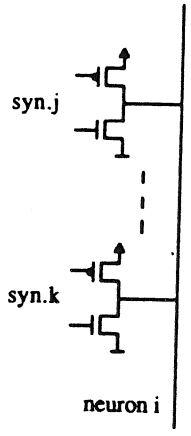


fig. 1

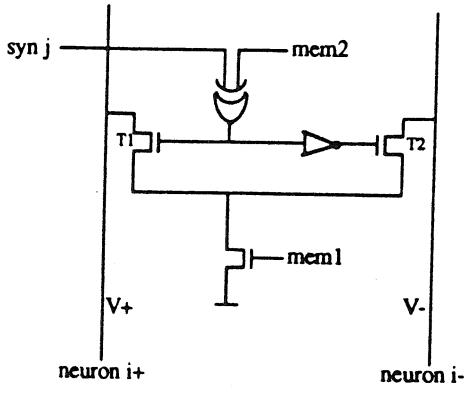


fig.2

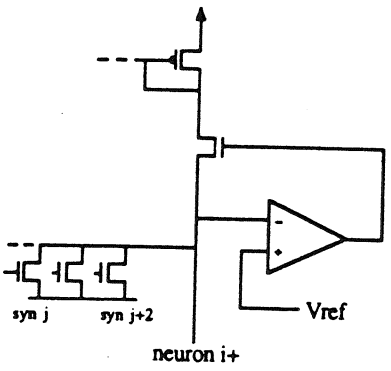


fig.3

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