A LOW-POWER SILICON-ON-INSULATOR PWM DISCRIMINATOR FOR BIOMEDICAL APPLICATIONS

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ABSTRACT

A CMOS/SOI circuit to decode PWM signals is presented as part of a body-implanted neurostimulator for visual prosthesis. Since encoded data is the sole input to the circuit, the decoding technique is based on a double-integration concept and does not require dc filtering. Non-overlapping control phases are internally derived from the incoming pulses and a fast-settling comparator ensures good discrimination accuracy in the megahertz range. The circuit was integrated on a 2mm single-metal SOI fabrication process and has an effective area of 2mm^2. Typically, the measured resolution of encoding parameter α was better than 10% at 6MHz and V_{DD}=3.3V. Stand-by consumption is around 340mW. Pulses with frequencies up to 15MHz and α =10% can be discriminated for V_{DD} spanning from 2.3V to 3.3V. Such an excellent immunity to V_{DD} deviations meets a design specification with respect to inherent coupling losses on transmitting data and power by means of a transcutaneous link.

I. INTRODUCTION

With the perspective of providing quasi-ideal three-terminal transistors, the CMOS Silicon-on-Insulator technology has increasingly become more attractive as compared to its bulk counterpart on designing integrated circuits with superior performance on temperature and radiation hardness, packing density, frequency operation, power consumption, latch-up hazards and others [1]. Very-low leakage currents make CMOS/SOI suitable for micropower applications such as battery-powered and human-implanted devices.

A SOI circuit to discriminate PWM-encoded data has been designed as part of a neurostimulator for a visual prosthesis project [2] whose block diagram is displayed in Figure 1. The complete system consists of external and body-implanted parts, coupled by means of a transcutaneous link. The artificial eye corresponds to a two-dimensional array of pixels containing photo-detectors and processing units mimicking the neural networks of the retina with real-time, parallel massive computation capabilities. A processor containing a switching matrix, PWM encoding circuit and a transmitter transposes signals from the retina into coded data to be transmitted to neurostimulator. RF transmission of both data and power is based on a technology developed for cochlear implants. Two flat coils, fixed to each side of the skin, act as transmitting and receiving antennas. A receiver, a single-input PWM decoder and a current-driving circuit make up the implanted neurostimulator. Discriminated data acts on current sources and define the appropriate stimuli to electrodes placed around the optic nerve.

Usually, PWM encoding and decoding techniques for data transmission are well known and easily accomplished. Discrimination is simplified when a clocking signal, locked-up to the main high-frequency encoding clock, is made available at the local receiver, as commonly happens in network communication. In such cases, chip complexity or low-power consumption does not necessarily represent a major design constraint, however. Data can also be decoded by using the PWM signal to control the charge of an integrator with a reference applied to its input and taking the dc component of the resulting truncated ramp [3]. Nevertheless, low-pass filtering would demand large on-chip RC values.

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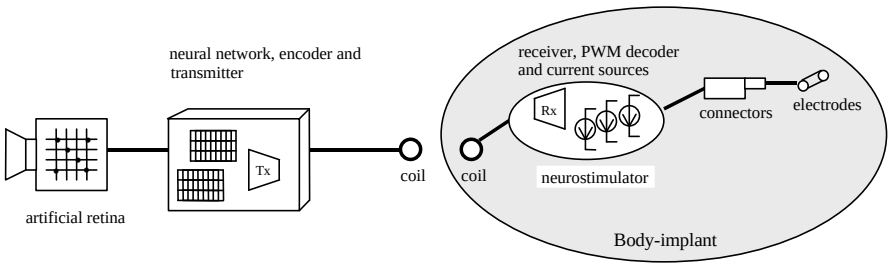

Figure 1. Visual prosthesis system

This paper introduces an accurate discrimination technique that handles the requisite of a unique input to the PWM decoder. Owing to inherent coupling losses in the transcutaneous link, it features good immunity to variations on power supply and input-data level. Furthermore, it can operate in the megahertz range while keeping power consumption at acceptable levels.

In Section II, the PWM decoder is described. Design procedures and simulated data are also discussed. Experimental results are presented in Section III. Discussion and concluding remarks are summarized in Section IV.

II. PWM DECODER DESCRIPTION

Figure 2 shows the decoder single input, a sequence of pulses D_{in} with a fixed frequency $f_{in} = 1/T_{in}$. Encoded by pulse-width modulation, the incoming information is expressed in terms of α, whose value is referenced to a duty-cycle of 50%. A coded "0" corresponds to a pulse shorter than $\frac{1}{2}T_{in}$ and is represented by $\alpha < 0$. Conversely, a logic "1" implies $\alpha > 0$. As no clock nor synchronizing signal is available, the arbitration condition (α=0) has to be internally generated.

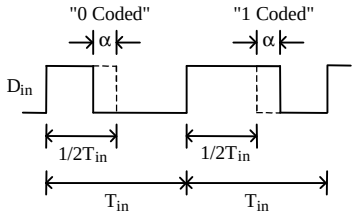

Figure 2. Incoming PWM data

The double-integration concept of the PWM discrimination is illustrated in Figure 3. Lossless capacitors C_1 and C_2 are charged by an ideal current source I_{REF}. Four non-overlapping phases are established to achieve full discrimination: *precharge (F1)*, *sampling (F2)*, *comparison (F3)*, and *reset (F4)*. All phases remain high during a period T_{in} with exception of sampling that coincides with D_{in} and has therefore duration of ($\frac{1}{2}T_{in}$+/-α). During precharge, capacitor C_1 is charged to a reference voltage V_{REF}. Similarly, capacitor C_2 is charged during sampling. By setting $C_1 = 2C_2$, V_{REF} would ideally correspond to the reference condition α=0. By neglecting any meaningful leakage effect on the stored charges due to non-ideal switches, comparison between V_{REF} and V_{C2}, carried out during Φ_3, assigns the digital value to the encoded α parameter. Upon reset phase Φ_4, the comparator output is latched and capacitors discharged.

The decoder block diagram is illustrated in Figure 4. It comprises an edge-detector with schmitt-trigger input (ST/ED), a phase-generator (PG) and integrator-comparator (INT/CMP) blocks. Input clock to the phase-generator is derived by detecting the positive transitions of incoming data. Since no external reset signal is present, hazardous phase generation upon powering-up is avoided by turning unstable spurious states in the PG finite-state machine. As four phases are required to accomplish a bit discrimination, the same number of integrator-comparator sets are needed. Continuous and sequential decoding of D_{in} is ensured by rotating their control phases as indicated. For instance, Φ_1 generated by the PG block is connected as input Φ_1, Φ_2, Φ_3 and Φ_4 to INT_1/CMP_1, INT_2/CMP_2, INT_3/CMP_3 and INT_4/CMP_4, respectively. In this case, when precharge occurs in INT_1/CMP_1, sampling comparison and reset are respectively carried out in INT_2/CMP_2, INT_3/CMP_3 and INT_4/CMP_4.

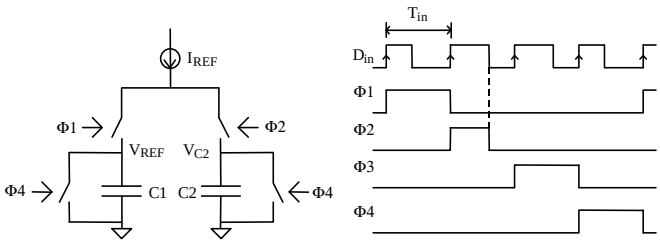

Figure 3. Discrimination basic concept (C_1=$2C_2$)

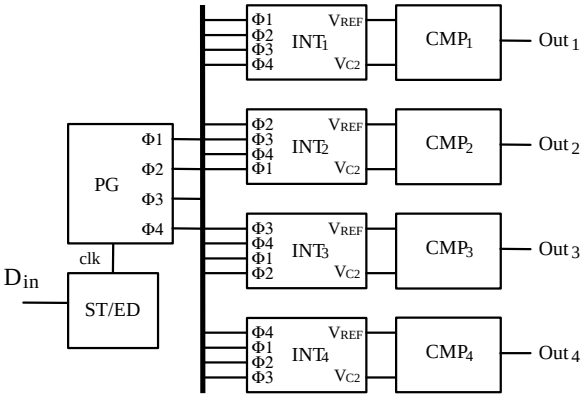

Figure 4. Decoder block diagram

The simplified schematic of a fast-settling voltage comparator is presented in Figure 5. It comprises a differential-input transconductance stage (M_1-M_{14}) in conjunction with a current subtractor (M_{15}-M_{18}) and a digital inverter (M_{19}-M_{22}). Gate capacitance C_G is initially discharged and inverter output OUT_N preset. Assuming ideal transistor matching, $V_{REF} > V_{C2}$ implies $I_B > I_A$ and $I_D = I_C = I_B - I_A > 0$ so that C_G begins to be charged. As C_L discharges through M_{14}, M_{12} turns on and reinforces the charge of C_G, knocking down OUT_N. Comparison is considerably sped up by such a positive feedback. Upon negation of Φ_3, C_G is discharged. Reversely, $V_{REF} < V_{C2}$ yields $I_B < I_A$ and $I_D = I_C = 0$. In this case, C_G remains uncharged and the inverter output preset. Clocked by Φ_3, a latch holds the comparison result over the four subsequent phases.

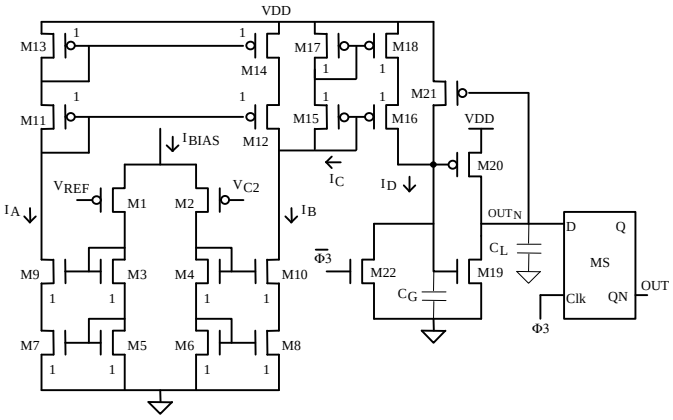

Figure 5. Comparator simplified schematic

In order to meet design specifications, the circuit has to decode data at f_{in} = 6MHz for α within +/-10% of $\frac{1}{2}T_{in}$. A single 3.3V-power supply is adopted. The PWM decoder was sized according to design parameters of a low-voltage, 2μm single-metal SOI fabrication process. N- and P-type transistors correspond to fully-depleted and accumulation-mode devices [1], respectively. Typical large-geometry, low-fields parameters correspond to V_{THN}=0.4V, V_{THP}=-0.4V, T_{ox}=30nm , μ_n=467cm^2/Vs and μ_p=142cm^2/Vs.

Since discrimination accuracy relies on good matching C_1/C_2=2 in the integrators, stray capacitances associated with input devices of comparator and interconnections should be carefully considered. Adopted values are C_1=4.1056pF and C_2=2.0528pF. As V_{C2} reaches its maximum value for $\alpha = \frac{1}{2}T_{in}$, I_{REF} is evaluated @V_{C2max}=3.3V and corresponds to 40μA. As C_1 and C_2 are only charged on Φ_1 and Φ_2, respectively, a single current source I_{REF} is time-shared between two INT blocks to reduce consumption. The comparator sizing is listed in Table 1 for I_{BIAS} = 5μA. Its input common-mode range (CMR) is [0.73V, 2.72V].

At nominal specifications, simulated results from ELDO revealed that data with the encoding parameter α within interval $3.2\% \le |\alpha| \le 52.8\%$ can be correctly discriminated. For these α values, $0.87V \le V_{C2} \le 2.66V$, so that the sampling voltage across C_2 is kept inside the comparator CMR. Figure 6 displays the waveforms at nodes OUT_1 – OUT_4 for data with different α's.

	M_{1-2}	M_{3-18}	M_{19}	M_{20}	M_{21}	M_{22}
W (μm)	30.0	8.0	12.0	6.0	3.0	12.0
L (μm)	3.0	4.0	2.0	2.0	2.0	2.0

Table1. Drawn sizing of comparator transistors

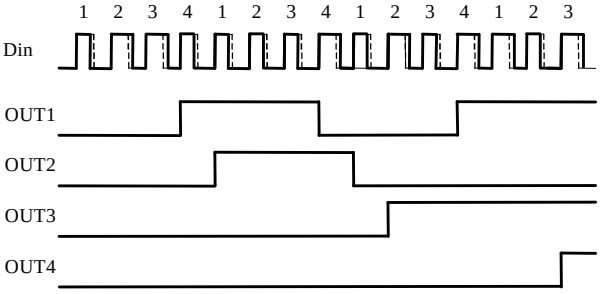

Figure 6. Simulated output waveforms

III. EXPERIMENTAL RESULTS

The circuit was integrated at Microelectronics Laboratory, Catholic University of Louvain, Louvain-la-Neuve. The PWM decoder effective area is 2mm^2 and its microphotograph is displayed in Figure 7. Typically, minimum recognizable parameter α was below 10% at 6MHz and V_{DD}=3.3V. As attested by process

characterization, important transistor mismatching limits the comparator resolution to roughly 7mV and degrades the α resolution, therefore. Figure 8 shows the highest operating frequency as function of power supply. Pulses with frequencies up to 15MHz and α=10% can be discriminated for V_{DD} spanning from 2.3V to 3.3V. Such a result represents a satisfactory immunity to power supply variations. Stand-by consumption is nearly 340μW. Waveforms of incoming and decoded data @6MHz and 3.3V are shown in Figures 9a and 9b for α=-10% and α=+7%, respectively.

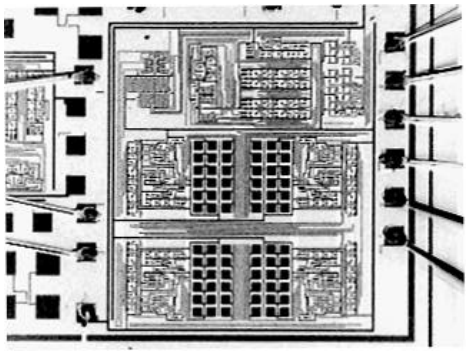

Figure 7. Die microphotograph

IV. CONCLUSION

A CMOS/SOI PWM discriminator intended for low-power biomedical applications was designed. Based on a double integration, the presented decoding technique meets the design restriction of having the incoming data as the only available signal to the decoder. Furthermore, it provides good discrimination accuracy while keeping circuit complexity and power consumption at acceptable levels. For a 2μm single-metal SOI fabrication process, the chip size is $2mm^2$. Minimum recognizable encoding parameter α was typically below 10% @6MHz and 3.3V, for a stand-by consumption of 340μW. As compared to simulated results, experimental resolution is degraded by significant transistor mismatches in the comparator, as indicated by process characterization. The decoder is capable to attain operating frequencies as high as 15MHz. Excellent immunity to power supply variations is achieved since pulses are discriminated for V_{DD} ranging from 2.3V to 3.3V.

V. ACKNOWLEDGEMENS

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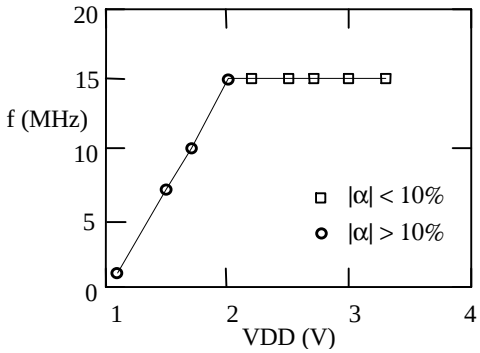

Figure 8. Maximum frequency against supply voltage

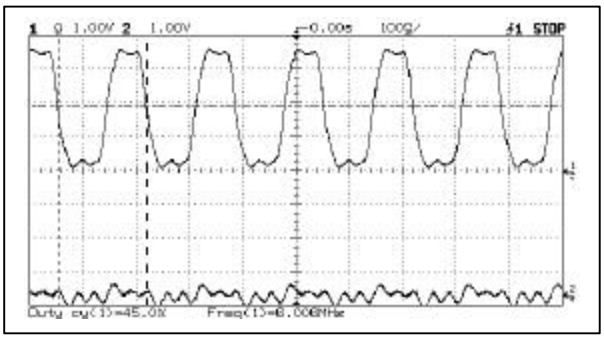

Figure 9a. Discriminator response to α=-10% @f= 6MHz

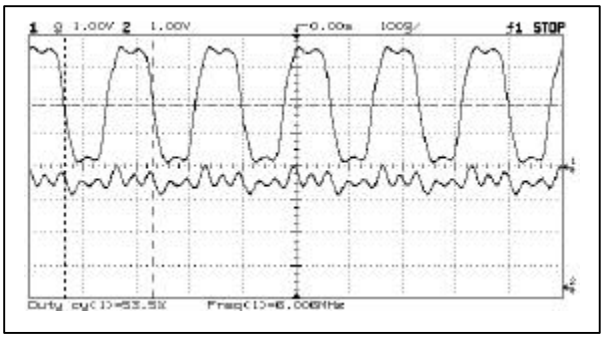

Figure 9b. Discriminator response to α=+7% @f= 6MHz