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Matching properties of CMOS SOI transistors

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Abstract

Analog implementations of neural networks have shown promising results; the main drawback of such techniques is the limited accuracy available in standard analog technologies. A test circuit composed of 256 *N-channel and P-channel transistors has been designed in a SOI (Silicon-On-Insulator) CMOS* 3 μm *technology and tested. This paper describes the matching properties of these current sources. We present results about mismatching depending on proximity and operating conditions. We also propose a method to compute the matching behavior of multiple current mirrors.*

1 Introduction

Neural networks algorithms have proved their usefulness in many situations but the large number of 'simple' computations and the parallelism of such structures are not well adapted to classical computers and tend to limit industrial applications. Analog implementation is well adapted to solve some problems and presents a good solution for these neural structures. Indeed, low accuracy computations (6 to 8 bits) like sums of products, non-linear functions and winner-take-all can easily be implemented by analog cells. However, the design of precise analog circuits requires a thorough understanding of the matching behavior of components available in any given technology.

The Silicon-On-Insulator technology is appeared ten years ago and makes every day substantial progress. This increases the popularity of this technology in comparison to other ones and to the most largely used: the CMOS bulk silicon process. We think that SOI is a reliable workhorse: it can cope with standard bulk technology, and shows interesting behaviors in presence of high temperatures or radiations; furthermore the SOI technology seems to have good matching properties [1] which will be exploited in the analog realizations of neural networks. Indeed, the SOI technology is attractive because it is simpler than bulk CMOS one on design and technology point-of-view (no well to integrate complementary transistor, full dielectric isolation on the devices,...) and it suppresses some yield hazard factors present in bulk CMOS.

In this paper, we focus our study on the matching behavior of MOS transistors, since this is a critical phenomenon which has to be taken into account for the analog VLSI implementation of neural networks.

After a short description of the circuit used for all the measurements, we will comment the results and will show the dependency of transistors mismatching on the distance separating them. At the end of this paper, we will propose a method to compute the mismatching for multiple current mirrors.

2 The test chip

To have an idea of mismatching between P-channel and N-channel transistors in a CMOS SOI technology, a test chip has been designed with current sources spread on a regular grid over the whole silicon area. Measuring the currents in the transistors under the same operating conditions will give an evaluation of the systematic and random variations of the characteristics for this technology.

The test chip includes 256 N-channel and 256 P-channel transistors of size of $W/L = 6\mu m/6\mu m$. The area is divided into 16 rows of 16 transistors. The whole area occupied by the transistors is a square of about $2mm$ side. Each matching transistor must be switched on and off sequentially. The solution we used is based on token which goes through all transistors or, more exactly, goes through all the command blocks of the matched transistors and connects the gate of

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the device under test to a constant input signal (here a voltage). In this solution, each command block is near the matched transistor it controls, thus the transistors are not as close each others as permitted by technological rules. The values obtained for the random parameters σ_β and $\sigma_{V_{th}}$ (the standard deviation of the conductance parameter and of the threshold voltage) will probably be greater and more scattered than in a well matched design.

3 Matching properties

In general, there are two kinds of parameter variations to consider in an integrated circuit process. Global variation accounts for the total variation in the value of a component over a wafer or a batch. Local variation or mismatch reflects the variation of a component value with reference to an adjacent component on the same chip. As the design of precise analog circuits is based on component ratios rather than on their absolute values, we will concentrate this paper on the mismatch behavior.

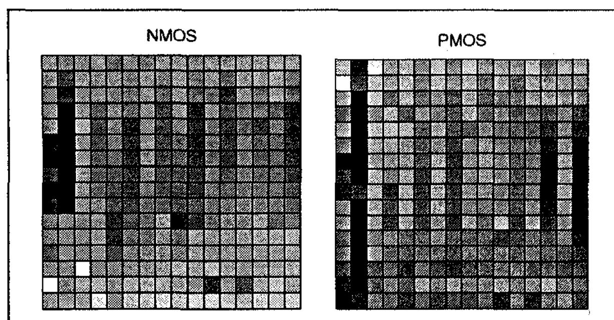

Figure 1: Distribution of currents for N-channel (left) and P-channel (right) transistors all over the chip.

For each transistor, we have measured the drain current with respect to its gate voltage with a constant drain voltage fixed for all tests to 1 Volt. To avoid errors due to temperature effects during the test, we have injected a current in a MOS transistor in diode configuration and which is sequentially connected to gates of matched transistors. The spreading of currents of N-channel transistors is presented on the figure 1, for a gate to source voltage of 2.5 Volts. The current values for NMOS transistors range from darker colors corresponding to a current of about 76 μA to the lighter ones corresponding to a current of 88 μA. The spreading of currents of P-channel transistors is presented on the same figure, for a gate to source voltage of −2.5 Volts. The current values for PMOS transistors range from darker colors corresponding to a current of about 30 μA to the lighter ones corresponding to a current of 37 μA.

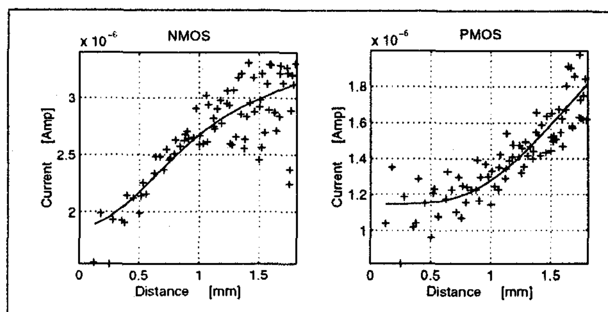

Figure 2: Errors on current function of the distance between transistors involved; the mean current flowing through the transistors is 82 μA for N-channel and 35 μA for P-channel.

As one can see on this figure, there are few jumps of color between two neighbor squares, but some gradients over the whole chip can be observed. By computing the mean differences of currents in function of distance between transistors, illustrated in the figure 2, we find a well-known result: the error grows with the distance between transistors [2].

Other important characteristics of mismatching are the value of β, the conductance parameter and of V_{th}, the threshold voltage. In fact, as we will see in the next section, these parameters will allow us to compute the mismatch in current over a wide range of operating conditions. The values of standard deviation of β and V_{th} given in the table below are not comparable to the results obtained in industry but we must keep in mind that the circuits we have tested come from an university experimental process line.

	$NMOS$	$PMOS$
$\bar{\beta}$	$52.22\ \mu A/V^2$	$18.58\ \mu A/V^2$
$\sigma_\beta/\bar{\beta}$	2.6 %	3.2 %
$\bar{V}_{th}$	$349\ mV$	$-149\ mV$
$\sigma_{V_{th}}/\bar{V}_{th}$	4.5 %	9.8 %

4 Errors on current versus current

During the test, the drain current is measured with a sweep of the gate voltage for all transistors. By this way, the transistor is first put in a saturated mode and then works in linear region.

In the case of saturation region, Lakshmikumar [3] has shown that the mismatching in current can be

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expressed in terms of σ_β and $\sigma_{V_{th}}$:

$$\frac{\sigma_{I_D}}{I_D} = \sqrt{\frac{\sigma_\beta^2}{\beta^2} + \frac{4\sigma_{V_{th}}^2}{(V_{GS} - V_{th})^2}}. \quad (1)$$

In the case of linear region, this equation becomes:

$$\frac{\sigma_{I_D}}{I_D} = \sqrt{\frac{\sigma_\beta^2}{\beta^2} + \frac{\sigma_{V_{th}}^2}{\left(V_G - V_{th} - \frac{\lambda}{2}(V_D + V_S)\right)^2}}. \quad (2)$$

These equations are obsolete when the gate voltage overdrive $(V_{GS} - V_{th})$ is too small and thus when the transistor goes in weak inversion. With these equations, the variance of currents is minimum when an important current flows through the transistor, or when the transistor is in strong inversion. Figure 3 illustrates the decrease of σ_{I_D}/I_D when the gate voltage overdrive (or the current in the figure) increases. The stars come from measurements and the solid and dashed lines come from theoretical computation based on the values of the table above. We have plot in solid lines the equations 1 and 2 when these equations correspond to the operating conditions (the transistors are respectively saturated and in linear region) and in dashed lines for the other situations. As we can see, the measurements are well adapted to theoretical curves. If the operating conditions impose low currents in the transistors, the mismatch in the threshold voltage ($\sigma_{V_{th}}$) will degrade the matching in current. On the other hand, for high current, the error in currents can not decrease with high gate voltage overdrive and tends to stabilize at σ_β/β.

5 Accuracy of multiple current mirrors

Conventional matching between two transistors in a current mirror may be not sufficient for some analog operations, and thus drastically decreases the precision of the computations, especially when the mirror ratio is far from 1. A simple method to increase the precision is to increase the size of both transistors, in order to reduce the border effects (technological variations on widths and lengths of transistors) [4] [3]; however, the centers of the transistors are then moved away, and this increases the influence of the other mismatching problems like circuit-size oxide or doping gradients. It seems obvious that a practical realization of an accurate mirror must be based on the use of identical transistors connected in parallel, for which a reasonable matching is around 2%. The transistors have to be geographically interleaved to compensate for the gradient mismatches.

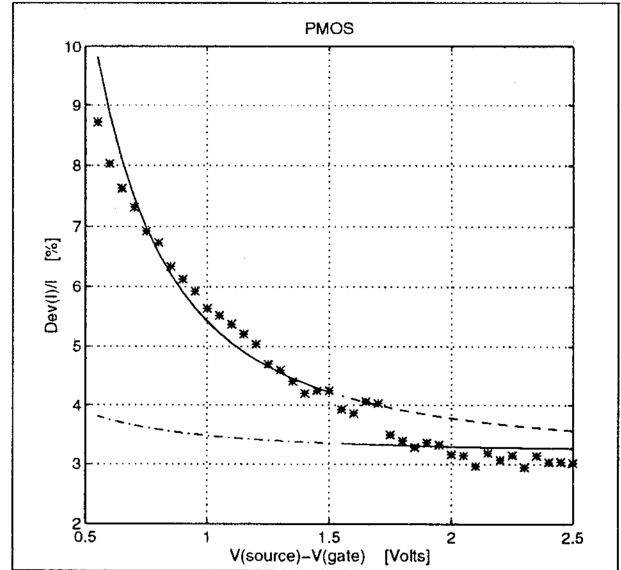

Figure 3: Ratio of the standard deviation of the drain current over this current in function of drain current (stars come from measurements and solid line comes from theoretical computation.

When the ratio between sizes of two transistors in the mirrors cannot be approximated by the ratio between two integers of a reasonable size, a unique supplementary transistor of a different size can be added to reach this ratio, without decreasing too much accuracy.

To evaluate the precision obtained on a ratio α between two groups of transistors, we consider two groups of (respectively x and y) identical transistors connected in parallel, a supplementary transistor with a different size being added to the second group. If the current in each transistor is supposed to be an independent Gaussian variable of mean and standard deviation $\{\bar{I}, \sigma\}$ for the identical transistors and $\{\bar{I}_\epsilon, \sigma_\epsilon\}$ for the last one, we can evaluate the mean and the standard deviation of the ratio α:

$$\bar{\alpha} = \frac{Y + \epsilon}{x},$$

$$\frac{\sigma_\alpha}{\bar{\alpha}} = \sqrt{\frac{1}{x}\left(1 + \frac{1}{\alpha}\left(1 - \frac{\epsilon}{y}\right)\right)\left(\frac{\sigma}{\bar{I}}\right)^2 + \frac{\epsilon}{x^2\bar{\alpha}^2}\left(\frac{\sigma_\epsilon}{\bar{I}_\epsilon}\right)^2},$$

where $\epsilon = \bar{I}_\epsilon/\bar{I}$. If the ratio α may be approximated by the ratio of two integers, this last equation may be simplified to:

$$\frac{\sigma_\alpha}{\bar{\alpha}} = \sqrt{\frac{1}{x}\left(1 + \frac{1}{\alpha}\right)}\frac{\sigma}{\bar{I}}.$$

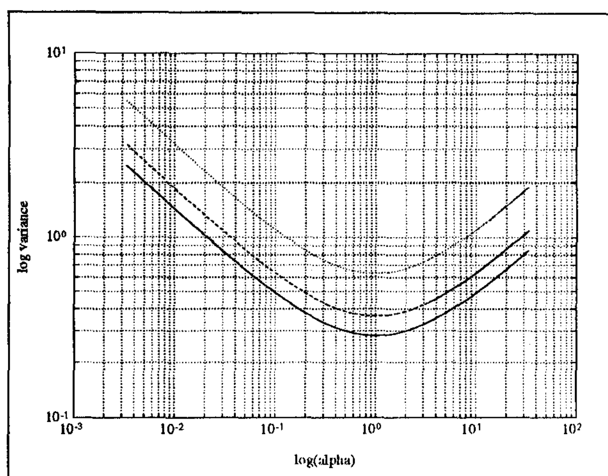

Figure 4: Evolution of $(\sigma_\alpha/\bar{\alpha})/(\sigma/\bar{I})$ with respect to α for $x+y=10$ (upper curve), $x+y=30$ and $x+y=50$ (lower curve).

These two equations show that, for a given silicon area, i.e. for a fixed number $x+y$ of transistors, the error on α increases when the ratio becomes different from 1. Figure 4 illustrates the standard deviation $\sigma_\alpha/\bar{\alpha}$ with respect to $\bar{\alpha}$ for a given number of transistors. The number x was allowed to take real values to obtain continuous curves. This graph gives thus the obtainable precision for ratios being approximated by a rational. One can also observe that, if the total number of transistors is doubled, the standard deviation is reduced by about 30%.

6 Conclusion

It has been shown in this paper that matching components on a VLSI chip is not an easy job even if design precautions are taken to limit the effect of different working conditions applied to two devices (size, proximity, orientation, neighborhood, temperature,...) [5]; technological constraints limit the maximum precision which can be obtained. We have illustrated by chips measurements some well-known results like the influence of proximity on matching of current sources. This study has pointed out that splitting matched pairs of transistors into many smaller ones and interleaving them improves the matching of currents, we have proposed a method to compute the gain we can obtained through by this technique which is, of course, area consuming.

Acknowledgments

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