A CMOS/SOI Continuous-Time Low-Pass g_m-C Filter

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Abstract

This paper describes a preliminary comparative analysis between continuous-time g_m-C filters based on a specific transcondutor but designed according to CMOS/bulk (conventional) and CMOS/SOI fabrication processes. A compensation technique to minimize the phase-error (lead-phase) of the basic integrator owing to the relatively high output-conductance of the adopted transconductor is examined. Such a technique consists of moving the RHP zero frequency closer to the non-dominant LHP pole by adding an extra capacitance along the signal feedforward path.

A 3rd-order low-pass, ladder-type elliptic-filter was designed and integrated on a 2μm CMOS/SOI fabrication process. At nominal bias and V_{DD}=5V, the filter experimental parameters are f_p=4.1MHz, f_s=12MHz, A_{max}<2.47dB and A_{min}>39dB. As no meaningful gain-peaking around the roll-off frequency was found, small phase-error associated with basic integrators can be assumed. The filter linearity is described by a THD of 0.25% for a differential output voltage V_{out}=200mV_{pp}.

I. Introduction

With the perspective of providing quasi-ideal three-terminal transistors, the CMOS Silicon-on-Insulator technology has increasingly become more attractive as compared to its bulk counterpart on designing integrated circuits with superior performance on temperature and radiation hardness, packing density, frequency operation, power consumption, latch-up hazards and others [1]. Very-low leakage currents make CMOS/SOI suitable for micropower applications such as battery-powered and human-implanted devices.

Continuous-time filters successfully process high-speed signals in applications where distortion and noise performance are not too demanding such as many data communications and video circuits. Their lower consumption with respect to switched-capacitor filters makes them thus attractive to low-power applications. Transconductance-C filters can readily be implemented in fully-integrated form, compatible with the remaining, often digital, system in most desired technologies. Besides, electronic-tuning against environmental or processing variations can be made by adjusting the g_m parameter through its dependence on some dc bias voltage or current [2-5]. Owing to smaller stray capacitances, CMOS/SOI filters are expected to feature better performances concerning frequency-range and linearity than their counterparts integrated on conventional CMOS/bulk processes.

This paper is organized as follows. In Section II, a comparison between the frequency characteristic of CMOS/SOI and CMOS/bulk integrators, built around the transconductor-cell proposed by Krummenacher [6], is carried out. By employing a macromodeling of the integrator, the phase-lead at the unity-gain frequency, caused by the transconductor relatively low output-resistance, is compensated by properly adjusting the frequency of the positive zero associated with the signal feedforward path. In Section III, the design of a CMOS/SOI low-pass, 3rd-order Cauer filter is presented. Experimental results of the CMOS/SOI filter are presented in Section IV. Conclusions and final remarks are summarized in Section V.

II. Integrator Modeling and Design

The simplified small-signal model of an inverting g_m-C integrator is shown in Figure 1. Low-frequency transconductance and the finite output-conductance are

represented by g_{mo} and g_o, respectively. C_i and C_o are the stray-capacitances at input and output nodes, respectively, and C_p the coupling capacitance. Assuming $C_i >> C_p$ and defining $C_T = C_L + C_p + C_o$, the integrator transfer-function turns out

$$\frac{V_o(s)}{V_s(s)} = \frac{C_p}{R_s C_i C_T} \frac{s - \frac{g_{mo}}{C_p}}{\left(s + \frac{1}{R_s C_i}\right)\left(s + \frac{g_o}{C_T}\right)} \qquad (1)$$

with a low-frequency gain $-g_{mo}/g_o$. Dominant and secondary poles are respectively $p_1=g_o/C_T$ and $p_2=1/(R_sC_i)$. As expected, the feedforward capacitance C_p gives rise to a zero $z_1=g_{mo}/C_p$ on positive real-axis.

A previously-reported transconductor stage [6] was considered for a comparative analysis between circuits of same functionality integrated on CMOS/bulk and CMOS/SOI. Figure 2 displays the schematic of the adopted fully-differential transconductor. It basically corresponds to a differential-pair, whose linear range is extended by voltage-controlled source-degeneration, and active loads with an embedded common-mode feedback (CMFB) loop. Nominal parameters are g_m = 150µS, g_o = 2µS, C_i = 0.42pF, C_o = 0.22pF and C_p = 20fF. In order to compare the integrator performance in different fabrication processes, an identical g_m was assumed as design specification for the CMOS/SOI version. Transconductor-sizing for both versions is listed in Table 1, for a nominal bias current I_{ref} = 50µA.

Simulation of CMOS/bulk and CMOS/SOI circuits was carried out with PSPICE and ELDO, respectively. Design and process parameters correspond to a standard 0.8µm CMOS and a 2µm CMOS/SOI fabrication processes. A single supply-voltage V_{DD} is assumed. Figure 3 overlays the resulting frequency characteristic of both integrators, for C_L=5pF. The CMOS/bulk version revealed a unity-gain frequency f_t=446kHz, a low-frequency voltage-gain A_V =19dB and a phase-error of 4.5°, whereas its CMOS/SOI counterpart presented f_p=110kHz, A_V =28.1dB and a phase-error of 1.0°. Lead-phase is mainly associated with dominant-pole p_1 due to the transconductor relatively high output-conductance on both versions although the CMOS/SOI one exhibits a lower g_o. As an excessive phase-error may cause gain-peaking in the filter-passband near the roll-off frequency, and consequently distortion [7], its reduction by moving the zero z_1 to frequencies close to p_1 is thus proposed. Such a technique tends to compensate for the original phase-lead since a zero on the RHP acts as a LHP pole, as far as phase-shifting is concerned. In practice, compensation is achieved by adding an extra capacitance C_{ex} along the feedforward path, as depicted in Figure 4. As $g_o/C_T << (1/R_sC_i)$, the secondary pole shouldn't affect the C_{ex} value.

The compensation effect on the phase-error is shown in Figure 5. For C_{ex} = 200fF, the phase error decreases from 4.44° to 3.34° for the CMOS/bulk integrator. Nonetheless, a further improvement occurs for the CMOS/SOI version where the phase-error is lowered from 1.00° to –0.01° (excess phase). As the compensation technique is affected by process random-variations as well as modeling-uncertainties of output-conductances and stray-capacitances, an optimal C_{ex} that would exactly cancel out the phase-error is not therefore proposed. By means of careful layout-extraction and simulation, a range of C_{ex} capacitances can however be found to lower the phase-error (lead or excess) close to one-degree values.

	CMOS	/SOI	CMOS	/Bulk
Transistor	**W [µm]**	**L [µm]**	**W [µm]**	**L [µm]**
M1-M1A	264	6	44	1.6
M2-M2A	15	2	7.6	1.6
M3-M3A	40	10	44	1.6
M4-M4A	26	12	120	1.6
M5-M5A	46	2	21	1.6

Table 1. Drawn-sizing of transconductor-transistors

III. Filter Design

The block diagram and specifications of a balanced 3rd-order low-pass, RLC ladder elliptic-filter with resistive termination using a gyrator-capacitor combination is shown in Figure 6. Filter specifications correspond to a nominal 3dB-cuttof frequency f_p=4.0MHz, a stopband-frequency f_s=12MHz, a passband-attenuation A_{max}<1.0dB and a stopband-attenuation A_{min}>23dB. On-chip capacitors are C_1=2.88pF, C_2=0.7375pF, C_3=2.88pF and C=2.675pF. The simulated frequency characteristic of the CMOS/SOI filter is displayed in Figure 7, for V_{DD}= 5V, resulting f_p=5.75MHz, f_s=19MHz, A_{max}<1.5dB and A_{min}>25.7dB.

IV. Experimental Results

The CMOS/SOI version of the designed filter was integrated at the Microelectronics Laboratory, Catholic University of Louvain, Louvain-la-Neuve, Belgium. Effective area is 2mm^2 and its microphotograph is displayed in Figure 8. The measured frequency response of the filter @V_{DD}=5V is illustrated in Figure 9. As it can be seen, no meaningful gain-peaking near roll-off frequency is found which suggests occurrence of a small phase-error associated with building-part integrators. The filter experimental parameters are f_p=4.1MHz, f_s=12MHz, A_{max}<2.47dB and A_{min}>39dB, which are in good agreement with simulation. The 3dB-cutoff frequency as function of V_{DD} is illustrated in Figure 10. The meaningful difference between simulated and measured data could mostly be attributed

to inaccuracies of the pseudo SOI-transistor model embedded in ELDO that is simply adapted from a standard MOSFET modeling. Moreover, non-ideal effects in metal/poly-Silicon floating and grounded capacitors may also contribute to such deviations.

The filter 3dB-cutoff frequency can be tuned by the bias current I_{ref}, as shown in Figure 11, variations of the bandwidth with the supply voltage could be compensated by adjusting I_{ref} through on-chip auto-tuning systems [8]. The filter linearity corresponds to a total harmonic distortion (THD) of 0.25% for a differential output-voltage V_{out}=200mV_{pp}. The measured THD as function of signal level (peak amplitude) @V_{DD}=4V is shown in Figure 12.

V. Conclusion

A comparative analysis between continuous-time g_m-C filters based on a specific transcondutor but designed according to different fabrication processes was carried out. Simulated data from the frequency response of CMOS/bulk and CMOS/SOI basic integrators confirm a better performance of latter version with respect to low-frequency gain and phase error. In addition, this work proposes a compensation method to cope with the lead-phase due to the relatively high output-conductance of the adopted transconductor. Based on the integrator small-signal macromodeling, the resulting RHP zero is moved towards the non-dominant LHP pole by adding an extra capacitor along the signal feedthrough-path.

A balanced 3rd-order low-pass, RLC ladder-type elliptic-filter was designed and integrated on a 2µm CMOS/SOI fabrication process. At nominal bias and V_{DD}=5V, the filter experimental parameters are f_p=4.1MHz, f_s=12MHz, A_{max}<2.47dB and A_{min}>39dB, which are on good agreement with simulated data. As no meaningful gain-peaking around the roll-off frequency was found, small phase-errors related to building-part integrators are suggested. The filter presents a THD of 0.25% for a differential output voltage V_{out}=200mV_{pp}@V_{DD}=4V. Lack of accurate modeling for SOI transistors in circuit simulators, such as ELDO and PSPICE, precludes from obtaining a closer fitting between simulated and experimental results as observed, for instance, on the filter frequency response as function of the power-supply voltage.

VI. Acknowledgements

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VII. References

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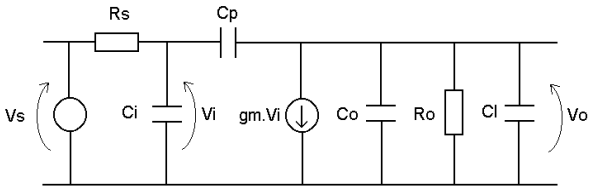


Figure 1. Equivalent small-signal model of gm-C integrator

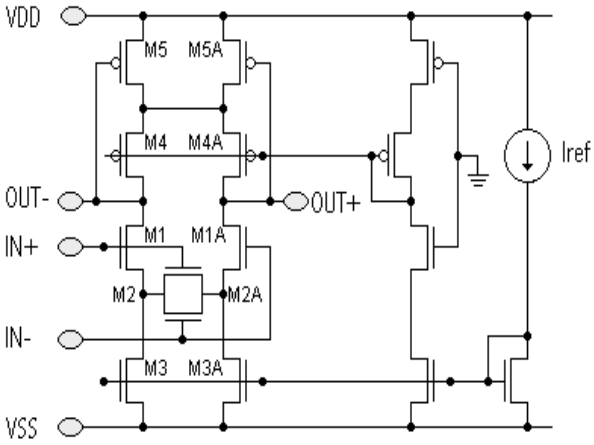
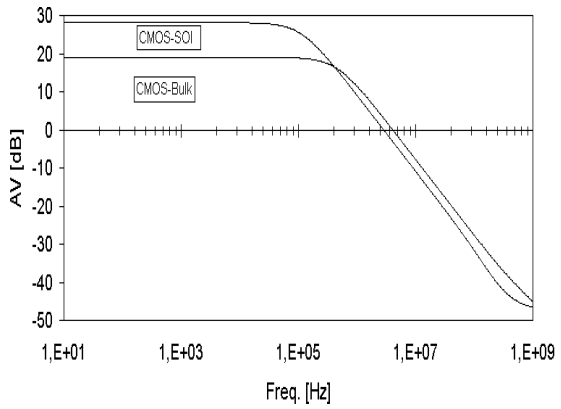
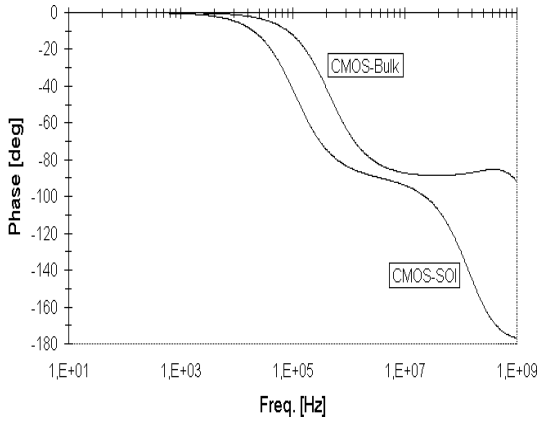


Figure 2. Fully-differential transconductor [6]



(a)



(b)

Figure 3. Simulated frequency response of integrators: (a) gain and (b) phase

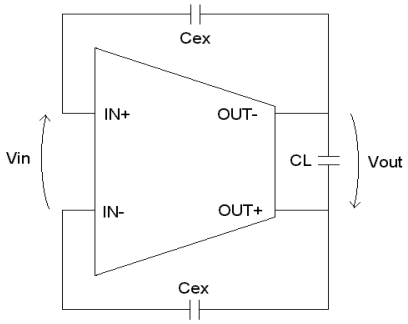


Figure 4. Integrator with compensation capacitors (C_{ex})

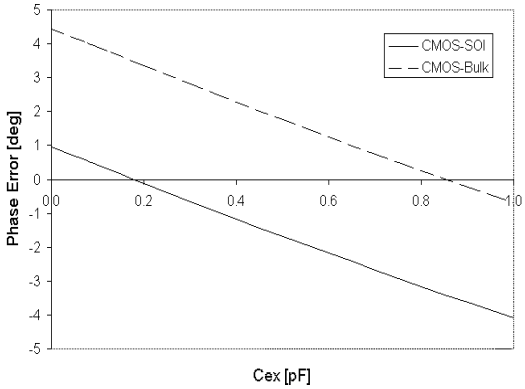


Figure 5. Simulated phase-error of integrators.

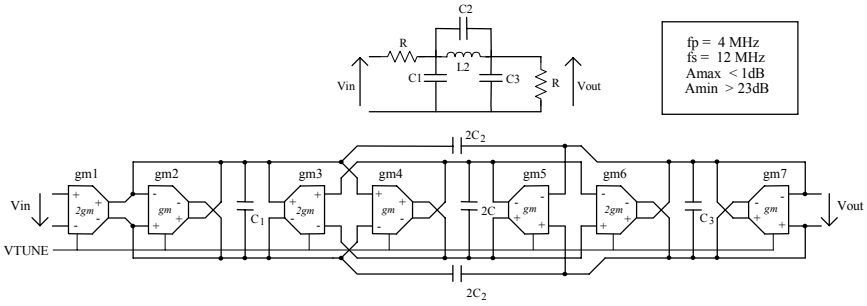
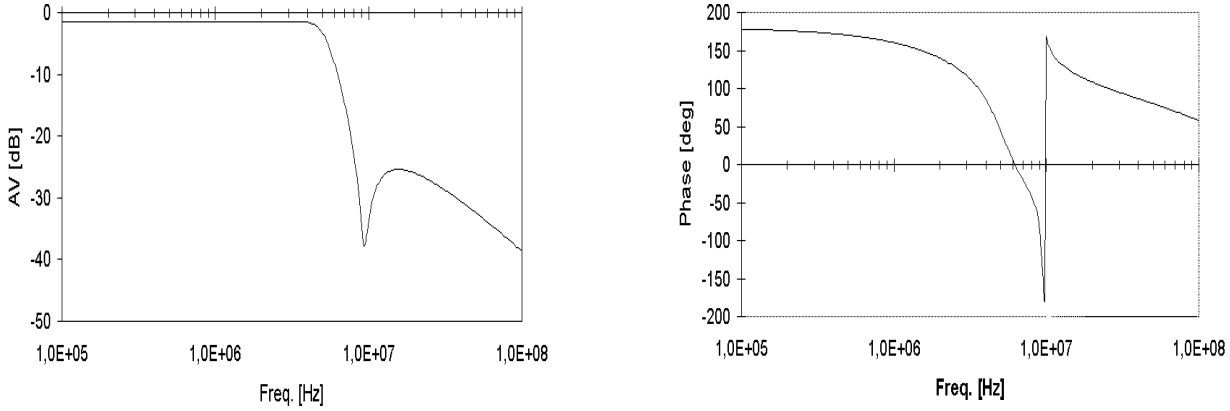


Figure 6. Block diagram of a 3rd-order low-pass Cauer gm-C filter (inset: filter specification)



(a) (b)

Figure 7. Simulated frequency response of SOI filter : (a) gain and (b) phase

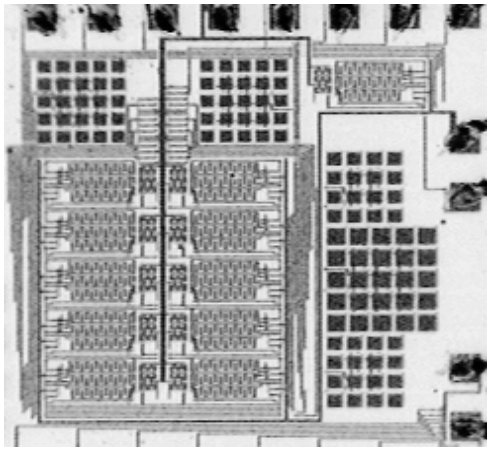


Figure 8. Microphotograph of the SOI filter

Figure 9. Measured frequency response of the SOI filter

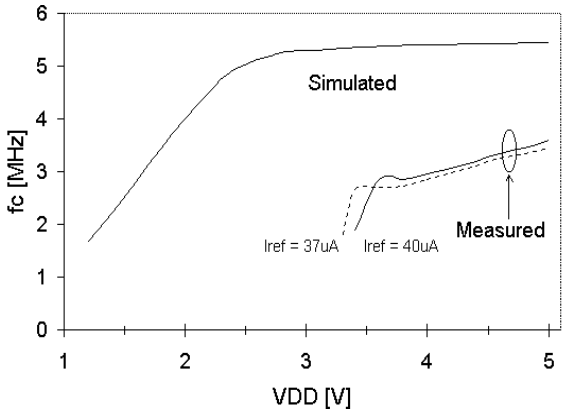


Figure 10. SOI filter characteristic against supply-voltage

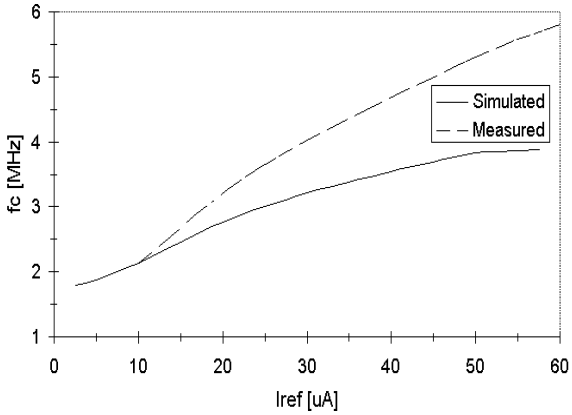


Figure 11. SOI filter bandwidth as function of bias current

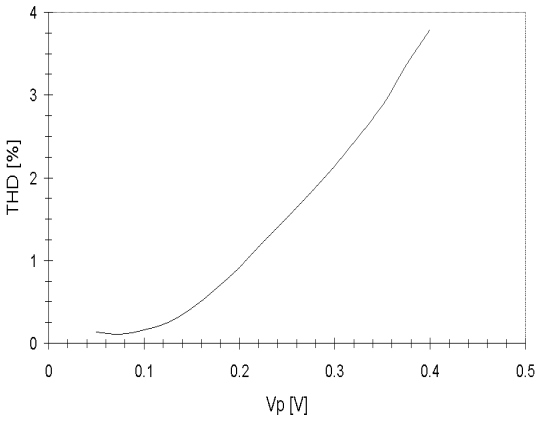


Figure 12. Measured total harmonic distortion of SOI filter @V_{DD} = 4V