Implementing Trojan-Resilient Hardware from (Mostly) Untrusted Components Designed by Colluding Manufacturers

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European Research Council Established by the European Commission





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Introduction

Private Circuits 3

Targeted algorithm

Hardware Design

Conclusion

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- 4. The foundry needs to be trusted.



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Trojan resilience overview: Dziembowski et al (CCS2016)

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- Use redundancy in unstrusted devices.
- Perform trusted majority vote among them.





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No need for non colluding manufacturers thanks to combination of: Passive secure multi-party computation Test amplification

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Reduce the trusted area compared to the unprotected:



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 - 1. First Private Circuit 3 implementation
 - 2. Algorithm: protocol and blockcipher
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 Circuit computes c'_i based on two shares to multiply.



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Can build any functions

- No memory is needed in the master, only rooting and xoring is
- A single element needs to be sent for multiplication

Speed depends on:

Number of rounds

Cipher	# of	Sbox	bits
	rounds	per round	per enc.

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Bottleneck if fed fast enough No restriction on the mini-circuits



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Parallel bus on N bits



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Parallel bus on N bits

- ► Allows to send *N* bits at the time in a full duplex manner ⊘.
- Allows to send 1 bits at the time in a full duplex manner.

Bus	6	AES My			sterion
Throug.	N	Cycles	Through.	Cycles	Through.
[Gbps]	[bit]	[cycle]	[Mbps]	[cycle]	[Mbps]
1.5	1	180	55	96	107
6	4	46	222	24	428



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Parallel bus on N bits

- ► Allows to send *N* bits at the time in a full duplex manner ⊘.
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Parallel bus on N bits

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Serial bus on 1 bits

- Allows to send 1 bits at the time in a full duplex manner.
- ► The master do not need to duplicate XOR gates and routing ⊗ .

		AES	Mys	sterion			
N	Cycles	Through.	Cycles	Through.	☆	1	1
[bit]	[cycle]	[Mbps]	[cycle]	[Mbps]	X	T	Т
1	180	55	96	107	$-\alpha[1]$		
4	46	222	24	428	r[1]		
	N [bit] 1 4	N Cycles [bit] [cycle] 1 180 4 46	AES N Cycles Through. [bit] [cycle] [Mbps] 1 180 55 4 46 222	N Cycles Through. Cycles [bit] [cycle] [Mbps] [cycle] 1 180 55 96 4 46 222 24	AES Mysterion N Cycles Through. Cycles Through. [bit] [cycle] [Mbps] [cycle] [Mbps] 1 180 55 96 107 4 46 222 24 428	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$

The bus used is Serial to have 16[GE] per sub-circuit OThe number of bits to exchange is the critical part for data throughput.

Majority vote

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Majority vote area [GEs]										
λ Bit select. Serial Maj. Tot										
8	44	52	96							
16	77.6	67	144.6							



Methodology:

$$\Pr[M(x) \neq D(x)] = \left(\frac{n}{t}\right)^{\lambda/2} \le 2^{-80}$$

t [days]	n [hite]		AES			Mysterion		
	II [DIIS]	λ	ROB.	Area [GEs]	λ	ROB.	Area [GEs]	
	10 ³	6	2^{-95}	181	5	2^{-81}	144	
1	10 ⁶	8	2^{-86}	224	8	2^{-89}	224	
	109	15	2^{-85}	380	14	2^{-84}	361	
	10 ³	5	2^{-86}	144	5	2^{-88}	144	
7	10 ⁶	7	2^{-86}	202	7	2^{-88}	202	
	109	12	2^{-85}	321	11	2^{-81}	286	

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Changing the blockcipher allows to either:

▶ Reduce λ

t [days]	n [bits]	AES			Mysterion		
		λ	ROB.	Area [GEs]	λ	ROB.	Area [GEs]
1	10 ³	6	2^{-95}	181	5	2^{-81}	144
	10^{6}	8	2^{-86}	224	8	2^{-89}	224
	10 ⁹	15	2^{-85}	380	14	2^{-84}	361
7	10 ³	5	2^{-86}	144	5	2^{-88}	144
	10 ⁶	7	2^{-86}	202	7	2^{-88}	202
	10 ⁹	12	2^{-85}	321	11	2^{-81}	286

Methodology:

- ► Set the testing time *t*
- ► Set the number of runs *n*
- ► Choose λ

$$\Pr[M(x) \neq D(x)] = \left(\frac{n}{t}\right)^{\lambda/2} \le 2^{-80}$$

Changing the blockcipher allows to either:

- ▶ Reduce λ
- Get smaller bound

Mysterion AES t [days] n [bits] λ ROB. Area [GEs] λ ROB. Area [GEs] 2^{-95} 2^{-81} 10^{3} 6 181 5 144 2^{-86} 2^{-89} 10^{6} 1 8 224 8 224 2^{-85} 2^{-84} 10^{9} 15 380 14 361 2^{-86} 2^{-88} 10^{3} 5 144 5 144 2^{-88} 2^{-86} 10^{6} 7 7 7 202 202 2^{-85} 10^{9} 2^{-81} 12 321 11 286

Outline

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Conclusion

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